AN ENERGY-EFFICIENT, HIGH SPEED CLASS-E TRANSMITTER FOR BATTERY-FREE WIRELESS SENSOR NETWORKS

by

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To all the people who stood against my dreams and tried to hold me back.. Thanks, you made me stronger.

Table of Content

List of Tables

List of Figures

Abstract

Energy efficiency and power consumption are increasingly important in wireless communications and especially for wireless sensor networks (WSNs). The limited energy budget in a WSN imposes many constraints on the transmitter side and limits WSN performance especially with the increasing demand for a high data rate in biomedical and imaging applications. In this dissertation, an energy-efficient, high data rate, quadrature phase shift keying (QPSK) class-E transmitter is developed. This transmitter is a promising alternative to conventional phase shift keying (PSK) and direct modulation transmitters. This prototype is fully integrated in CMOS 65 nm technology and has an optimized power consumption and output power to achieve good efficiency and a high data rate. The prototype transmitter employs a class-E power oscillator along with system and circuit level design methodology to maximize the efficiency. The power oscillator is a self-oscillating power amplifier that utilizes a positive feedback system. An efficient new technique for phase modulation (PM) that achieves the 360^o phase shift without the need for an additional circuit is presented. The transmitter operates at 2.4 GHz with a data rate of 69 Mbps and transmitting power of -6.8 dBm with achieved energy/bit of 42 pJ/bit and 2.9 mW power consumption. The transmitter's global efficiency is between 7.7% to 23% under a 0.4 V power supply.

The first class-E power oscillator is tunable between 1.9 and 3.3 GHz. It is robust to $\mp$20% frequency deviation due to PVT variations. The second power oscillator is designed to be suitable for more area-efficient applications to reduce the fabrication cost. It achieves a peak output power of -0.5 dBm and a peak efficiency of 37.5% under a 0.4 V power supply and frequency tuning range of 1.66-2.7 GHz. This oscillator is robust to $\mp$15% frequency deviation from a 2.4 GHz nominal frequency.

Towards the implementation of a battery-free WSN, an autonomous and reconfigurable triple band energy harvester, capable of performing high RF power tracking to maximize the harvested DC power and enhance efficiency, is developed. The harvester has the potential of being deployed along with remote sensor nodes to enhance the nodes' operational life-time. A peak PCEs of 57%, 43% and 33% are achieved at 2.4 GHz, 900 MHz and 1.2 GHz respectively. 30% and 10% increments in the harvested voltage at 900 MHz and 1.2 GHz with a sensitivity of -19 dBm are achieved.

This work emphasizes techniques to improve the energy efficiency of WSN transmitters towards the next generation of WSN. It is anticipated that these solutions will shape future work towards solving many challenging research problems in WSNs.

List of Abbreviations and Symbols Used

ASK Amplitude shift keying.

BER Bit error rate.

CFP Ceramic flat pad.

CMOS Complementary metaloxidesemiconductor.

DAC Digital-to-analog converter.

EIRP Effective isotropic radiated power.

EVM Error vector magnitude.

FCC Federal communication commission.

FF Fast-fast.

FOM Figure-of-merit.

FSK Frequency shift keying.

GBW Gain-bandwidth frequency.

IL Injection locking.

ILRO Injection locking ring oscillator.

ISM Industrial, scientific and industrial.

LC Inductor-capacitor.

LC VCO Inductor-capacitor voltage controlled oscillator.

LO Local oscillator.

MIMCAP Metal-insulator-metal capacitor.

MN Matching network.

MUX Multiplexer.

NMOS N-type metal-oxide-semiconductor.

NMOSFET N-type metal-oxide-semiconductor field effect transistor.

OOK On-off keying.

PA Power amplifier.

PCE Power conversion efficiency.

PLL Phase-locked loop.

PM Phase modulation.

PMU Power management unit.

PRBS Pseudo random bit signal.

PSK Phase shift keying.

PVT Process, temperature variation.

Q Quality factor.

QPSK Quadrature phase shift keying.

REC Rectifier.

RF Radio frequency.

RFIC Radio frequency integrated circuit.

RFID Radio frequency identification.

RLC Resistor-inductor-capacitor.

RMS Root mean square.

RO Ring oscillator.

SNR Signal-to-noise ratio.

SS Slow-slow.

TSMC Taiwan Semiconductor Manufacturing Company.

WBN Wireless body network.

WSN Wireless sensor network.

ZVDS Zero-voltage derivative switching.

ZVS Zero-voltage switching.

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Finally, my love and thanks to my children Sara, Anas and Amal for their support in this journey.

Chapter 1

Introduction

1.1 Introduction

Complementary metaloxidesemiconductor (CMOS) technology dominates the industry for the implementation of inexpensive and ultra-low power remote devices. The continuous scaling of CMOS technology in the last decades helped to reduce the integration cost and led to a new era of portable and miniature devices. Also, the progressive development in wireless technology and the improvement of the sensor integration has allowed the development of wireless body networks (WBN) and wireless sensor network (WSN) [1–5].

WBN/WSN has attracted many researchers in the academia and the industry as an enabler to provide a real-time health monitoring. The recent developments of these nodes have helped to improve the medical diagnoses and have provided better comfort for patients in many applications. WBN/WSN can be used also in fitness applications for athlete's bio-signal monitoring during their training. These networks can also be used in smart fabrics and gaming applications as well as in long-term deployment of outdoor video sensors to monitor wildlife as shown in Fig 1.1(a).

Remote autonomous nodes typically include a radio, controller, a power source and a sensing device as shown in Fig. 1.1 (b). The sensors can measure a wide variety of inputs: temperature, vibration, gas density, tension and so on. For biomedical applications, these WSNs can be implanted inside the human body or worn on the body depending on the type of targeting bio-signal.

Typically, the radiated power in these WSNs is below the 0 dB because sensor nodes communicate over relatively short distances. For nodes that are separated by (10-40) meters, an output power range between (-10-0) dBm is required.

The network architecture for WSN can be classified into two categories: flat architectures and multi-tier architectures. In a flat architecture, each single node sends its data to a personal server or a computer. In a multi-tier network, the data is collected

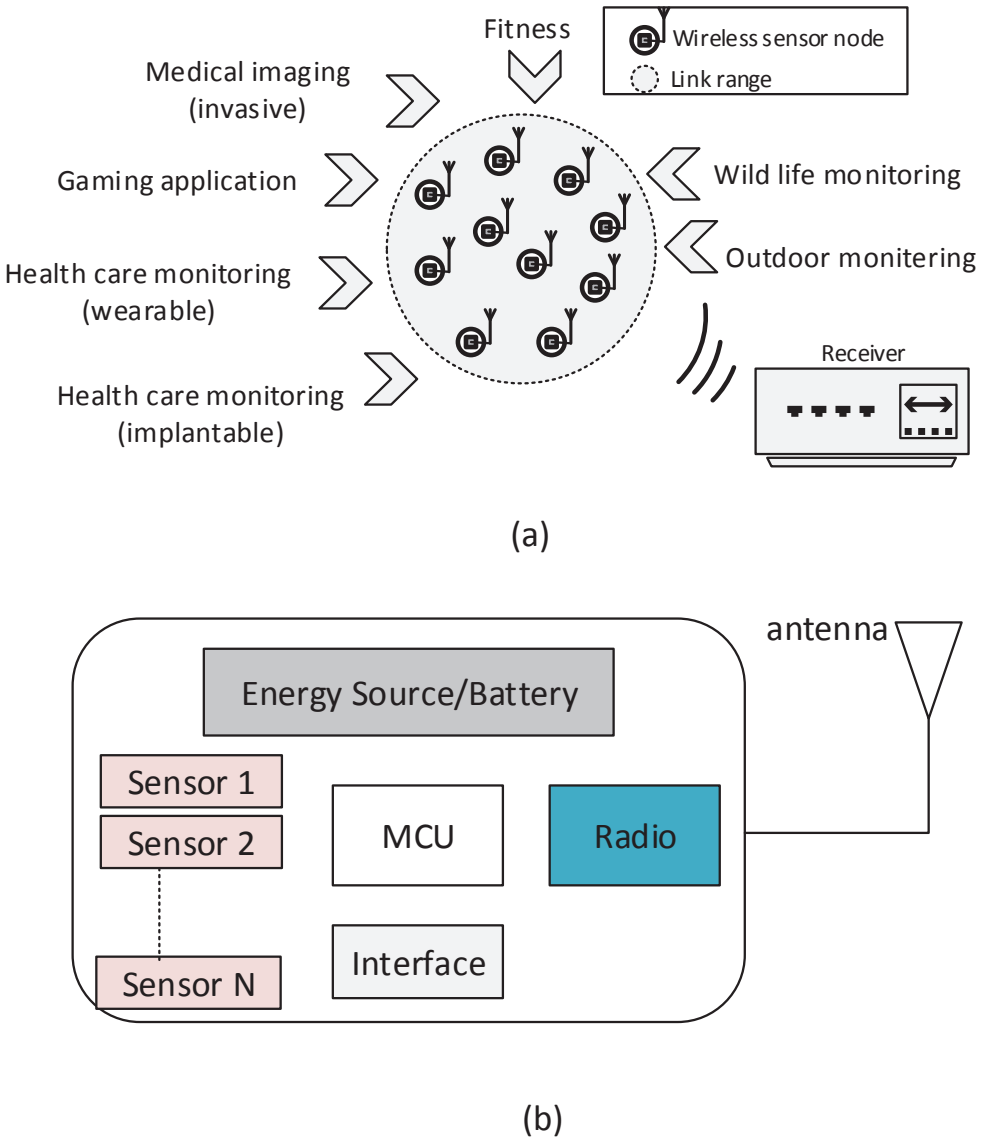


Figure 1.1: Wireless sensor network (a)applications and topologies (b) node architecture.

from multiple sensor nodes and is transmitted to a gateway point over a transmission range between (0.1-2) m. In the second tier link, the gateway acts as an interface between the first and the third tier over a range typically smaller than 10 m. The gateway node can be a smart phone or a computer to connect the local network to the global network. Since the receiver is implemented off the human body, there are no constraints on energy or size.

1.2 Facilitating the next generation of WSN

The limited energy budget in portable WBN/WSN imposes many constraints at the transmitter side, especially with the increasing demand for a high data rate. These constraints are at the resource level and at the performance level. In terms of the node resources, the power supply determines the power consumption, the life time and the size of the node. The RF transmitter is the most power hungry block in the WSN or WBN and it's power consumption dominates the total node's dissipated power. Therefore, the standard heterodyne conversion scheme is not a recommended solution for this kind of wireless link because it includes a mixer, filters and a power amplifier. This increases the design complexity and power consumption while reducing power efficiency. Furthermore, the choice of modulation scheme for these portable WSN has a significant impact on the transmitter architecture and hence the power consumption.

In terms of transmitter performance, metrics like efficiency, output power, transmission range and modulation accuracy are highly impacted by the limited power budget. There is a trade off between the transmitter efficiency, the power consumption and the transmission range. The transmitter efficiency (η_{Tx}) indicates how effectively the transmitter converts the power consumed into radiated power and can be expressed as :

$$\eta_{Tx} = \frac{P_{rad}}{P_{overhead} + \frac{P_{rad}}{\eta_{PA}}} \tag{1.1}$$

where $P_{overhead}$ is the DC power consumption of T_x and η_{PA} is the power amplifier efficiency. For WSN scheme, $P_{overhead}$ should be minimized and η_{PA} should be maximized. In general, energy efficiency can be improved by reducing the losses in the circuit or by minimizing the power consumption. In the literature, there have been

Table 1.1: Performance summary and comparison of the state of the art transmitters

References	Power consump. [mW]	Output power [dBm]	Efficiency %
[9]	0.33	-15	9
[10]	0.938	-15	3.19
[11]	1.3	-15	2.3
[12]	2.6	-8	6

many efforts to avoid the use of mixers by applying direct modulation. For instance, in [6], a direct heterodyne transmitter structure is implemented by using a modulator to mix the data with the carrier frequency. In contrast, in [7, 8], the data is directly applied to the carrier frequency without the need for a modulator.

Energy per bit is a very important figure of merit, which is the average amount of energy required to transmit a single bit of data and is determined by dividing the dissipated power of the transmitter by the bit rate. Minimizing the power budget improves the energy per bit. Yet, this degrades the output power of the transmitter. While the required output power depends on the targeted application, a relatively high output power is required to maintain a good bit error rate (BER) at high data rate. It is worth mention that, the communication system fails if the radiated power is too low. Table 1.1 demonstrates the relationship between power consumption, output power and efficiency. The comparison of the state of the art transmitters reveals that low output power transmitters suffer from poor efficiency.

The modulation scheme is another factor that limits the transmitter efficiency because there is a trade off between bandwidth efficient and energy efficient modulation schemes. For example, the on/off keying (OOK) and the frequency shift keying (FSK) have been used in energy efficient transceivers [13, 14]. However, these transceivers provide relatively low data rate due to the limited bandwidth efficiency in OOK and FSK. For Phase shift keying (PSK), the bits per symbol can be 2,3 or 4 for simple digital modulation. That not only increases the data rate but also improves the energy per bit figure of merit.

Node life time and footprint are critical for WSN. In order to maintain a small foot

Table 1.2: Power density of different types of energy scavenging

Energy source	Power density [W/cm^2]	Efficiency (%)	Integration	Specifications
RF	0.1μ, 1n	50	easy	900 MHz, 2.4 GHz
Solar	100m, 100μ	10-50	possible	indoor, outdoor
Vibration	6μ, 800μ	20-50	difficult	human(Hz), Machine(KHz)
Thermal	6μ, 100μ	0.1,0.3	difficult	Human, industrial

print for the node, the battery size must be reduced to the minimum. For instance, given a battery capacity of 625 mAh at 1.5 V supply with a node consuming on average 100 mW, the node will last only nine and half hours. Therefore, an energy harvesting system that charges or even replaces the battery is essential for autonomous operation.

Energy harvesting is the process in which the energy is collected from the environment. The key to design a battery-free device is to design a node that consumes few milli-watts. Thus, an energy efficient RF link is crucial to enable autonomous operation. The selection of the energy source depends on the environment surrounding the wireless node whether it is inside the human body, on the human body, or deployed outdoor. For example, thermal and vibration harvesting are suitable for inside the human body while harvesting from sun light is a good choice for long term deployed sensors. Also, there are other factors, such as harvesting efficiency, integration capability and available input power that determine the selection of the energy source. Table 1.2 lists different types of energy scavenging sources and their harvested power density, efficiency and ease of integration [15].

The comparison reveals that radio frequency (RF) power is a good solution for energy scavenging because the RF energy is available from different communication services such as TVs, cell phones and radios and is distributed over a frequency range between 900 MHz and 2.4 GHz. Therefore, it is a promising solution to replace or to recharge a battery in WBN/WSN. However, this energy is limited due to the free space attenuation as well as other losses in the wireless channel such as multi-path,

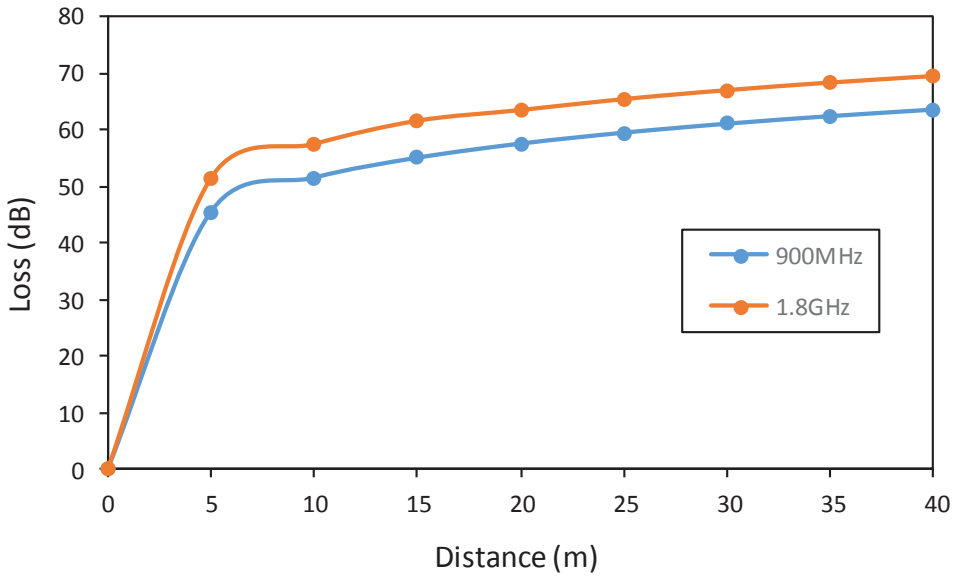


Figure 1.2: Free space loss versus link distance.

fading, reflection and absorption. The free space loss is given by the Friis equation [16] which is a function of the distance between the RF source and a device as shown in Fig. 1.2. These losses reduce the amount of the received power which is already limited by the Federal Communications Commission (FCC) regulations of the effective isotropic radiated power (EIRP) to 4 W [17].

The RF powered devices typically rely on a low bandwidth modulation scheme like OOK, amplitude shift keying (ASK) and backscattering transmitters to reduce the power consumption. Typically, a low data rate is achieved due to the low output power and the limited bandwidth modulation scheme. Table 1.3 lists several recent RF powered WSN. For OOK transmitters low data rate is achieved and even with a spectral efficient modulation [18], the date rate is a few Mbps. It is clear: there is an increasing need to support high data rate in WSNs.

Table 1.3: State of the art RF powered wireless link

Ref	Frequency (MHz)	Min Power(dbm)	Tx power(dbm)	Data Rate	Modulation
[18]	5.8 GHz	-5.9	-28.6	2.5Mb/s	32QAM
[19]	915/2400	-17.1	-12.5	5Mb/s	OOK
[20]	13.55/402	-13	N/A	90kb/s	Back Scatter
[21]	915/2400	-18.4	-2.5	0.5Mb/s	OOK

1.3 System Level Considerations

This section goes through various system level considerations of a wireless link for ingestible camera endoscopy or pill camera.

1.3.1 Frequency Band

The selection of the transmitter frequency band depends on many factors such as propagation, antenna size, required data rate and required signal bandwidth. To integrate a low frequency and a high quality inductor on a chip, it costs more die area and higher losses. In this project, the ISM band is chosen because it gives a good trade-off between antenna size and ease of integration. The corresponding channel bandwidth and channel capacity meet the high data rate requirement for high resolution image transmission. As well this band provides easier integration of the on-chip inductor and it is more area efficient.

1.3.2 Data Rate

Medical imaging requires a high resolution image transmission with a fast frame rate ($>10f/s$). A few Mega-bits per second (Mbps) is not enough to meet the high resolution requirement in a biomedical imaging. For example, in an RGB color scheme with 8 bit/pixel, frame size 640 x 480 with frame rate 6 fps, the required data rate is 44 Mbps. Moreover, for a neural recording system with 256 channels and a sampling rate of 15 KS/s and 10 bit resolution, the required data rate is 38 Mbps. The high

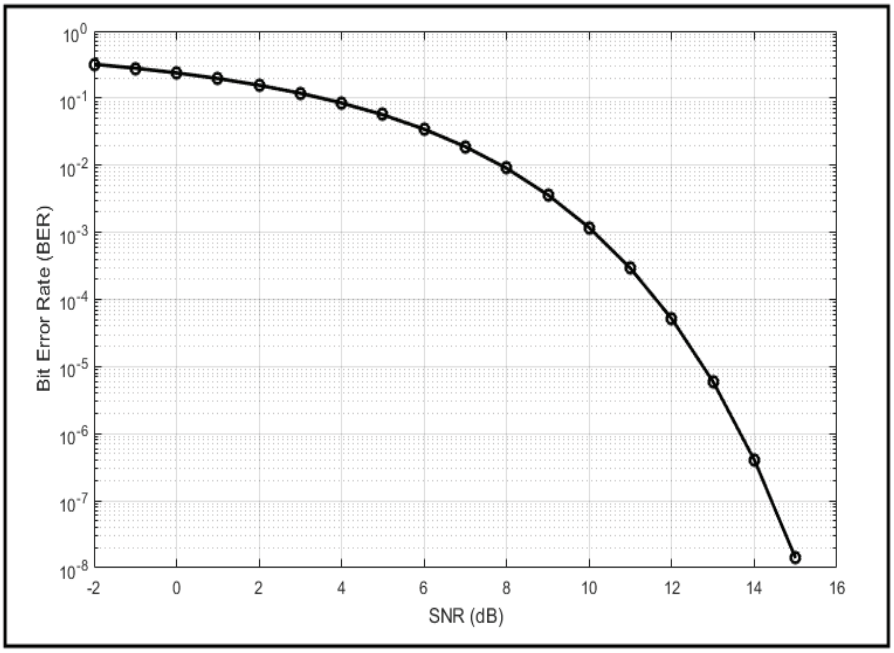


Figure 1.3: Simulated SNR vs required BER plot of a QPSK modulation

resolution and the fast frame requirement need a high data rate, therefore in this dissertation the targeted data rate is > 50 Mbps.

1.3.3 Modulation Scheme

The modulation scheme determines the circuit architecture and that limits the power consumption. As explained previously, in low power budget applications OOK and FSK modulation schemes are typically applied [13, 14]. However, a low data rate is achieved due to the limited bandwidth modulation scheme. To achieve a data rate more than 50 Mbps, a spectrally efficient modulation scheme is required. Therefore, the QPSK scheme is selected in this dissertation.

Although PSK transmitter requires a coherent receiver, the receiver is usually implemented off the human body since there are no constraints on energy or size.

1.3.4 Power Budget

Typically, the high data rate consumes more power, but the size constraints ($in\ mm^2$) limit the capacity of the battery and impose more constraints on the power budget. Especially when the devices are required to operate for six continuous hours once

Table 1.4: Targeting system level design specifications

Specifications	Target
Data rate	$>$ 50 Mbps
Frequency Band	2.4 GHz
Modulation scheme	QPSK
Power Consumption	$< 7mW$
Required EVM	< 23 %
Channel capacity	101 Mbps
Channel Bandwidth	83.5 MHz
Required SNR	$>$ 12 dB

ingested.

The camera endoscopy typically includes a LED, an image sensor and a transmitter. For a rough estimate of power consumption, if two batteries with capacity 83.7 mWh (Energizer no.399) are used, this means 27.9 mW/h for 6 hours duration. The image sensor and LED can consume up to 20 mW. Therefore, the designed transmitter and digital baseband circuitry should consume less than 7.9 mW in total. To satisfy the requirement of bit error rate (BER) $<10^{-4}$, the corresponding signal-to-noise ratio (SNR) should be more than 12 dB as shown in Fig. 1.3, which means a reasonable output power is needed to meet the required SNR. Table 5.1 summarizes the radio design requirements such as SNR, frequency, data rates, and power consumption of the target application.

1.4 Thesis Contributions

The main focus in this dissertation is the development of design techniques, system and circuit design, implementation and validation of an energy-efficient and a high data rate QPSK transmitter for a WSN/WBN and portable biomedical applications. The contributions of this dissertation are summarized here:

- Design methodology, analysis and implementation of a highly efficient class-E power oscillator was accepted in the journal " Analog Integrated Circuit and Signal Processing", titled "An energy-efficient and ultra-low voltage power oscillator in CMOS 65 nm", 2018 [22]. This work is reported in Chapter3.

- A new phase modulation technique for direct modulation is developed and demonstrated along with the digital circuit design to synthesize short pulses that are needed for phase modulation.

- The design and fully integrate a 69 Mbps QPSK transmitter in CMOS 65 nm technology for wireless sensor network applications. This includes both RF and digital components in the same chip. The proposed architecture with simulation results was published in ISCAS conference 2017 titled " A 69-Mbps Dual Tuning 8PSK/QPSK Transmitter using Injection Locking and RF Phase Modulation" [23]. This work is included in Chapter 4.

- The measurement and the evaluation of a QPSK prototype transmitter which achieves a relatively good efficiency and a low power consumption when compared to the other state of the art transmitters. These results were submitted to "IEEE Transactions on Very Large Scale Integration (VLSI) Systems " titled "An Energy-Efficient High-Speed Class-E Transmitter", 2018 [24]. This work is included in Chapter 4.

- To facilitate the next generation of a WSN, a battery-free transmitter is needed. Therefore, the design and the implementation of the triple RF bands energy harvester are presented in this research. The harvester enables a battery-free, autonomous and reconfigurable operation for a WSN. The initial results were published in ICECE conference titled as "Analysis and Design of Simultaneous Dual Band Harvesting System with Enhanced Efficiency", 2016 [25]. The extended analyses and characterization of the RF harvester were published in " Analog Integrated Circuit and Signal Processing" titled "A reconfigurable and instantaneous triple RF bands energy harvester using internal control loop", 2018 [26]. This work is presented in Chapter 5.

1.5 Organization of the Thesis

This dissertation presents the design of an energy efficient transmitter for a battery-free WSN. In Chapter 2, the transmitter's architectures are reviewed and compared. A technical overview of the low-power RF transmitter for WSN and medical applications is presented. The chapter focuses on phase modulation techniques and discusses the design and characterization of QPSK transmitter architecture.

Chapter 3 provides a design methodology and an efficiency analysis of a class-E power oscillator. The proposed oscillator is implemented using TSMC 65 nm technology. A novel energy efficient oscillator is presented. The final layout of the oscillator is also presented.

In Chapter 4, a new efficient technique for phase modulation is introduced and the corresponding mathematical equations are presented. The proposed transmitter architecture of an energy efficiency of 42 pJ/bit and 69 Mbps QPSK transmitter is presented. The measurement results and a discussion are included. The achieved performance of the proposed prototype design is compared with the state-of-the-art transmitter designs showing the improvement in power consumption, data rate, figure of merit (FOM) and efficiency.

Chapter 5 presents the design of an autonomous energy harvester that performs a high RF power tracking to maximize the harvested DC power and to enhance the efficiency. A model for a dual band harvester is derived. The design of a control loop to provide an autonomous operation of the RF tracking. The circuit design and the post layout simulations results are included. The achieved performance of the proposed harvester is compared with the state-of-the-art designs showing improvement in the efficiency and reconfigurable operation.

The summary and the conclusion of this dissertation are made in Chapter 6, where the contributions of the overall work are outlined and benefits of this work are discussed. Possible future work is discussed and a few related circuits are recommended for design and implementation.

Chapter 2

A Review of Transmitter Architectures

This chapter discusses the architectures of the RF transmitters with an emphasis on PM techniques and the relationships between power consumption, data rate, radiated power and efficiency. It describes the circuit design of directly modulated PSK transmitters. Finally, it lists and summarizes the performance parameters of recently published WSN transmitters.

This chapter is organized as follows: Section 2.1 presents the PSK modulation characteristics and accuracy. A review of transmitter architectures is discussed in Section 2.2. A list of recent WSN transmitters and their technical characteristics are included in Section 2.3. A summary of the chapter is presented in Section 2.4.

2.1 Phase Shift Keying Modulation Scheme

The transmitter modulates a message with a carrier and transmits it into the air through the antenna. In a conventional QPSK system, the phase of the carrier is modulated by multiplying the base band signal with the carrier using a quadrature mixer. The carrier phase is adjusted in increments of 90°. Four symbols are defined corresponding to four different phases: the first symbol "00" is defined at 0° and the phase is advanced by an additional 90° for the other three symbols as shown in Fig. 2.1.

For the i-th symbol, the equivalent phase is ϕ_i. The transmitter output voltage is simply expressed as a sinusoidal signal with an instantaneous phase shift such that:

$$V_{out} = V_m \cos(\omega_0 t + \phi_i) \tag{2.1}$$

Here, V_m is the peak amplitude at the output of the transmitter and ω_0 is the carrier frequency in radians.

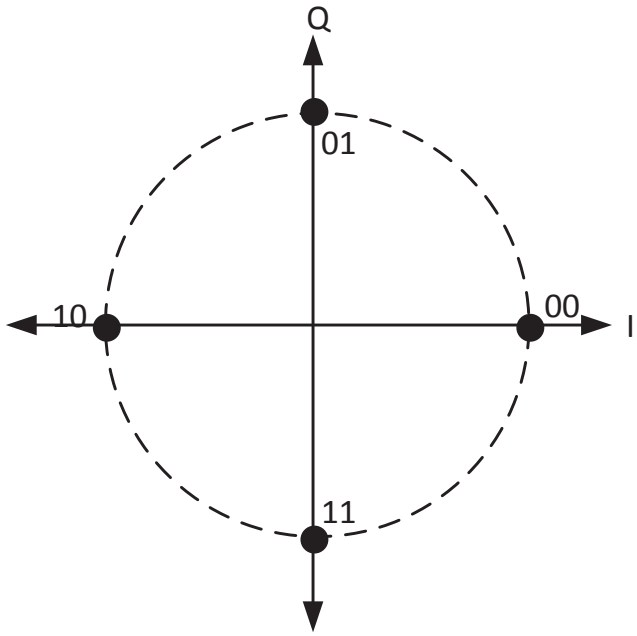


Figure 2.1: The constellation diagram of a QPSK modulation.

2.1.1 Modulation Accuracy

The PSK transmitter performance is characterized by the quality of the modulation. The figures of merit are the error vector magnitude (EVM) and the constellation map that shows the I,Q phasors. Vector signal analyzer(VSA) and vector signal generator (VSG) are usually used to perform the EVM testing. To achieve a row BER better than 10^{-4}, a typical QPSK transmitter requires an EVM better than 23%. EVM is the ratio of the measured output power(P_{error}) divided by reference power(P_{ref}) as found in (2.2).

$$EVM(\%) = \sqrt{[\frac{P_{error}}{P_{ref}}]} * 100 \tag{2.2}$$

To estimate the EVM, the vector plot shown in Fig.2.2 is used. It should be noted that the focus of our EVM analysis is on the systematic constellation error. In this plot, the vector CR is the reference vector, the vector CT is the measured vector,

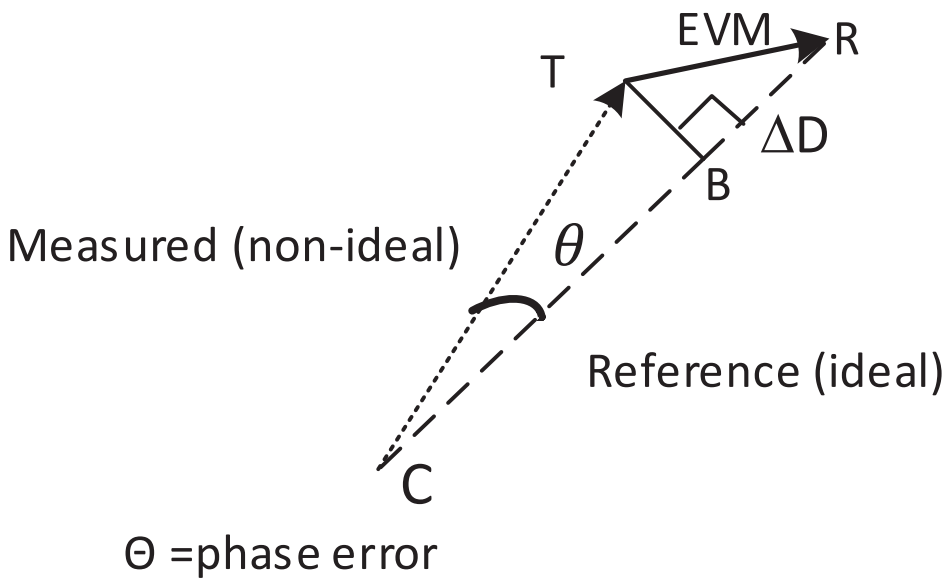


Figure 2.2: The graphical representation of EVM estimation.

the vector TR is the EVM and Θ is the phase error. If the phase error is very small, a right angle triangle is formed between ΔD and BT, the EVM can be obtained as follows:

$$EVM_{rms} = \sqrt{(TB)^2 + (\Delta D)^2} \ * 100\% \tag{2.3}$$

Where TB equals to $CT sin\ \theta$

$$EVM_{rms} = \sqrt{(\frac{\Delta D}{CT})^2 + (sin\ \theta)^2} \ * 100\% \tag{2.4}$$

Assuming both the magnitude error and the phase error contribute equally to the EVM and in order to meet the BER requirements, this result in the following error constraints:

$$\frac{\Delta D}{CT} < 0.16 \tag{2.5}$$

$$\theta < 9.3^o \tag{2.6}$$

The phase error constraint helps to determine the oscillator and frequency accuracy.

Another figure of merit thats helps to estimate the EVM is the SNR. If the SNR is high, the displacement of the measured vector from the reference vector due to noise and distortion effects would be very small and the EVM would approach zero. If SNR is poor, the displacement of the measured vector from the reference vector would be large and EVM would also be large.

$$EVM_{rms} = \sqrt{\frac{1}{10^{\mathrm{SNR(db)}/10}}} * 100\% \tag{2.7}$$

2.2 The Transmitter Architectures

This section reviews the architectures of the two-step conversion and direct conversion transmitter. It discusses the design parameters related to high power efficiency. The main focus is on direct PM for ultra-low-energy transmitter design.

2.2.1 Up-Conversion Transmitter

The phase modulation is realized by mixing the baseband information with the carrier frequency. The frequency up-conversion can be categorized into two architectures: the heterodyne frequency up-conversion and the homodyne frequency up-conversion.

The heterodyne frequency up-conversion architecture is shown in Fig. 2.3. It shows the block diagram of the two-step transmitter architecture. The output of the transmitter can be found as :

$$V_{out} = I(t)\cos(\omega_c t) + Q(t)sin(\omega_c t) \tag{2.8}$$

It employs filters, two sets of mixers, digital-to-analog converters (DACs) and a PA. The baseband I and Q quadrature modulation are at the intermediate frequency ω_1 and the mixer converts it to the RF frequency $\omega_1 + \omega_2$. The band pass filter after the second mixing rejects the LO leakage and unwanted image signal and this is very difficult to be integrated in a single chip. The RF signal is then amplified by the PA before transmitting the output power to an antenna. This architecture is very robust however, it consumes high levels of power and silicon area because it is comprised of many circuit blocks.

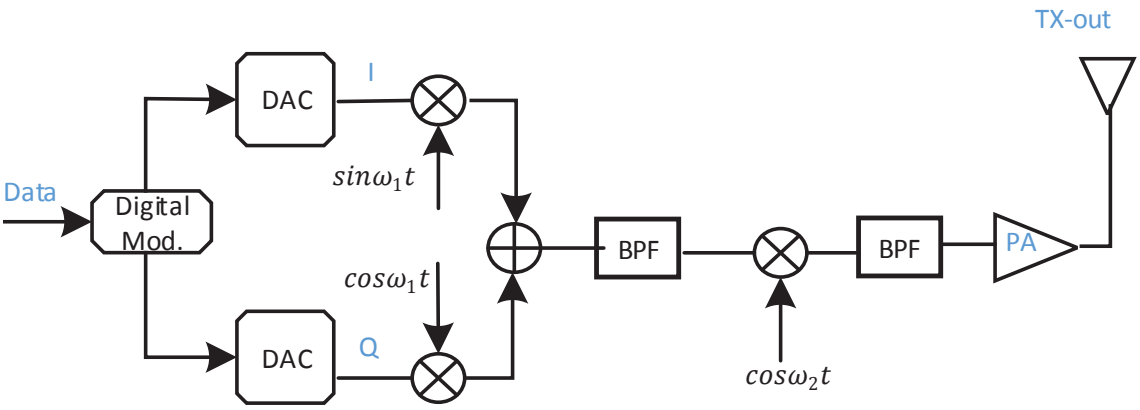


Figure 2.3: Block diagrams of heterodyne RF transmitter architecture.

The homodyne transmitter architecture is depicted in Fig. 2.4. Here, the base-band signal is directly up-converted to the RF signal. It is widely used in many applications due to it's flexibility to adopt any modulation scheme. The power consumption of the homodyne architecture is generally lower than that of the heterodyne architecture due to the elimination of the second mixer and the bandpass filter. However, the power consumption still doesn't meet the WSN power budget. Furthermore, this architecture suffers from injection pulling where the local oscillator (LO) is disturbed by the strong output signal of the PA. In spite of various shielding techniques employed to isolate the LO, the PA output still corrupts the oscillator spectrum.

2.2.2 Phase Locked Loop Transmitter

The Phase Locked Loop (PLL) is a fundamental building block in many modern communication systems. PLLs are widely used in various wireless applications such as frequency synthesis, frequency modulation detection and data detection.

A PLL is a nonlinear feedback control system which can be used to control the phase/frequency of the LO. The block diagram of PLL design is depicted in Fig. 2.5. It consists of a phase detector, a loop filter and a voltage-controlled oscillator (VCO). By synchronizing the VCO to an input reference, the VCO phase is more stable. The feedback system compares the VCO phase with the reference phase. The PLL generates an error signal which adjusts the VCO frequency to maintain constant

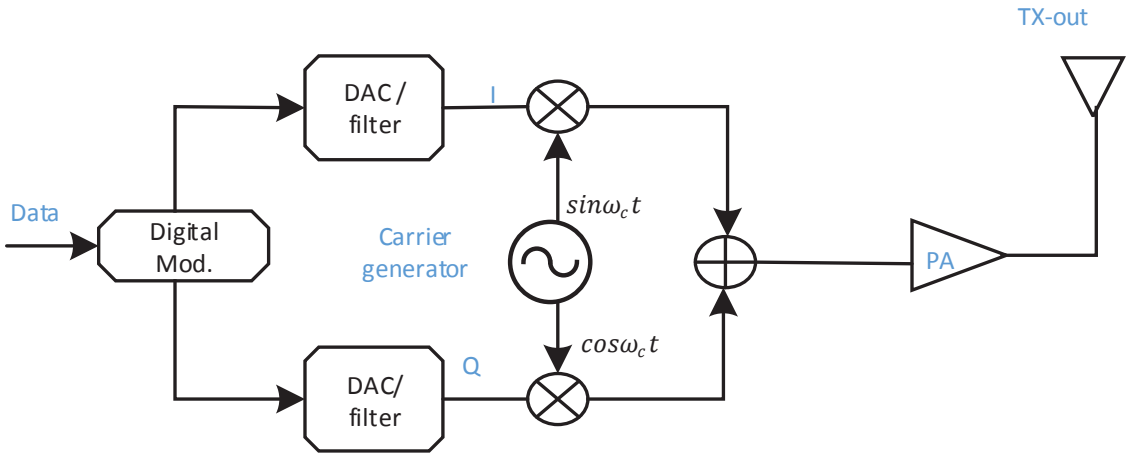


Figure 2.4: Block diagram of homodyne RF transmitter architecture.

phase with respect to input reference. The mismatch between I and Q paths limits the quality of the modulated signal.

Although PLL based transmitters are more hardware efficient than mixer-based transmitters and are often used in low power applications, the data rate is limited by the loop bandwidth. Using a bandwidth extension to increase the data rate leads to a gain mismatch and this degrades the transmitter performance and calibration is usually required.

2.2.3 Direct Modulation Transmitter

Direct modulation scheme is usually adopted to reduce power consumption and silicon area. In this implementation, the data is modulated to the RF directly without the use of a mixer. This architecture is simpler and supports simple modulation schemes like OOK, FSK and PSK. The following list summarizes all the directly modulated PSK transmitter architectures.

- Frequency Injection Locking Transmitter

  Injection locking (IL) is the synchronization of an oscillating system with an external signal as shown in Fig. 2.6(a). IL has gained substantial attention in

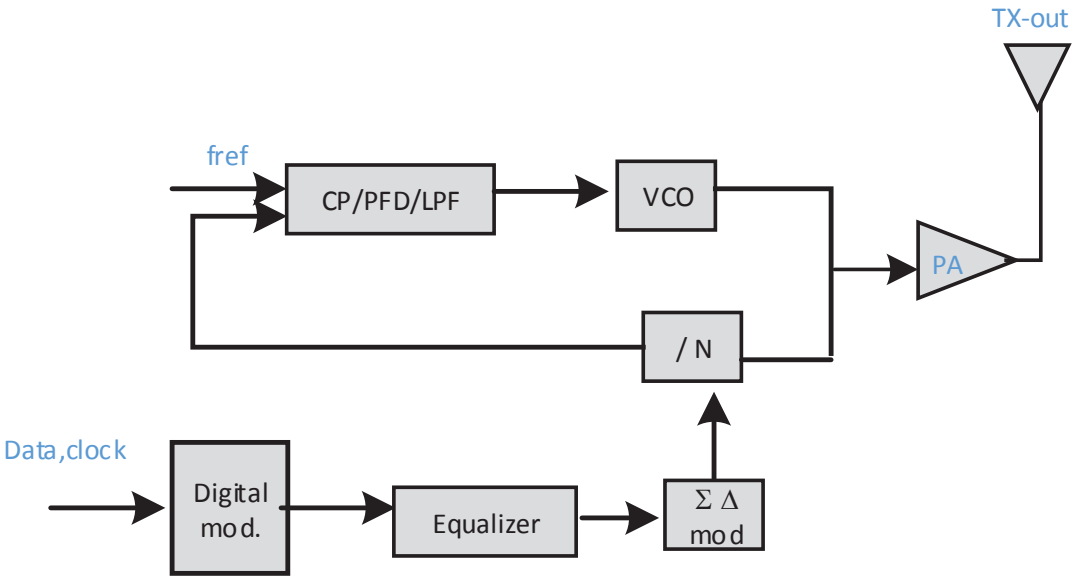


Figure 2.5: Block diagrams of PLL-based transmitter.

the communication system and this phenomena has been studied extensively in [27, 28]. Two key parameters in the design of a PSK transmitter are 1) the phase tuning range and 2) the power efficiency. Fig. 2.6(b) shows the phaser diagram of the injected signal and the output signal where θ is the phase between the injected signal and the output signal .

Fig. 2.7 illustrates the frequency injection locking mechanism. When the injection frequency $\omega_{inj} > |\omega_{inj} - \omega_{osc}|$, the oscillation frequency converges towards the injection frequency. However, if $|\omega_{inj} - \omega_{osc}| > \omega_{inj}$, the oscillator output remains unlocked. The phase θ and locking range ω_L are defined in [28] as the following:

$$\sin\theta \approx \frac{2Q}{\omega_{osc}} \frac{V_{osc}}{V_{inj}} (\omega_{osc} - \omega_{inj}) \tag{2.9}$$

$$\omega_L = \frac{\omega_{osc}}{2Q} \frac{V_{inj}}{V_{out}} \frac{1}{\sqrt{1 - \left(\frac{V_{inj}}{V_{out}}\right)^2}} \tag{2.10}$$

where Q is the tank equivalent quality factor.

As can be seen in (2.9) and (2.10), there are two factors that can be used to control θ: 1) the injected signal amplitude V_{inj} or the ratio $(\frac{V_{osc}}{V_{inj}})$ 2) the tank

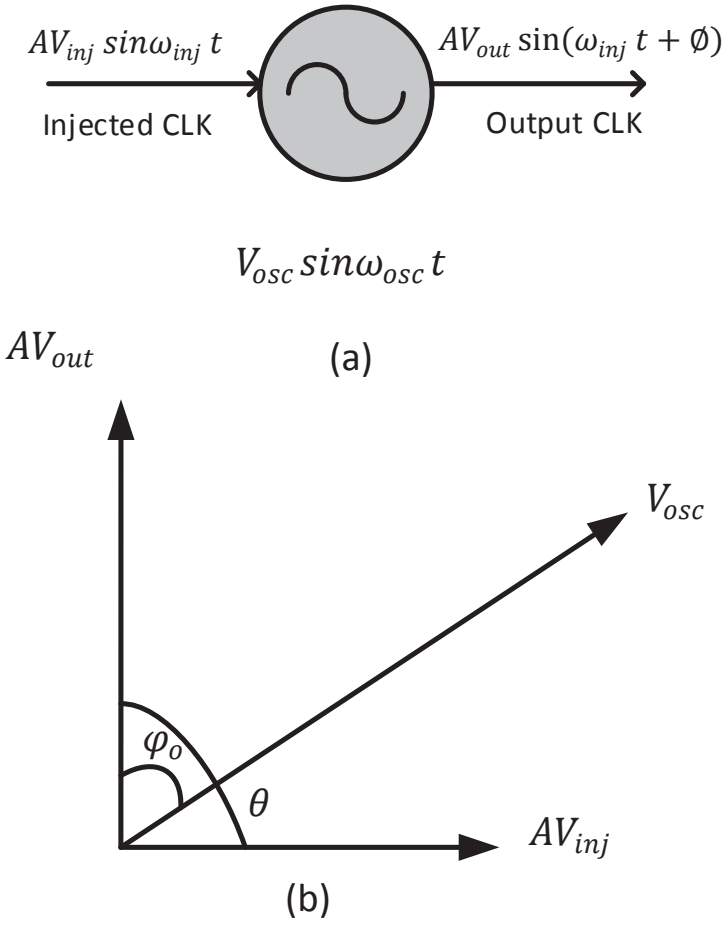


Figure 2.6: Injection locking process (a) conceptual diagram (b) phasor diagram of injected and output signal.

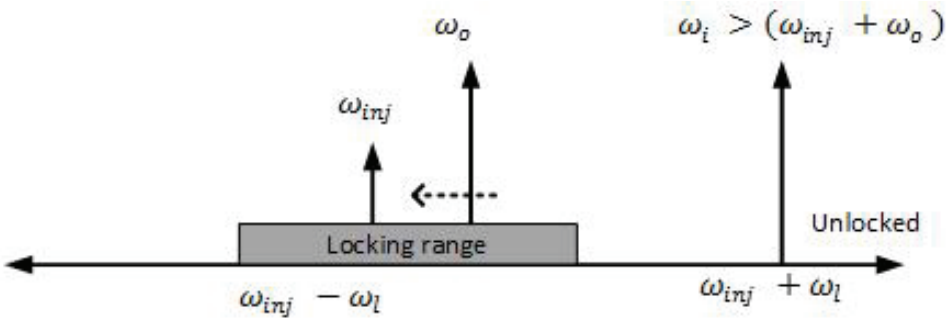


Figure 2.7: Th representation of the injection locking range.

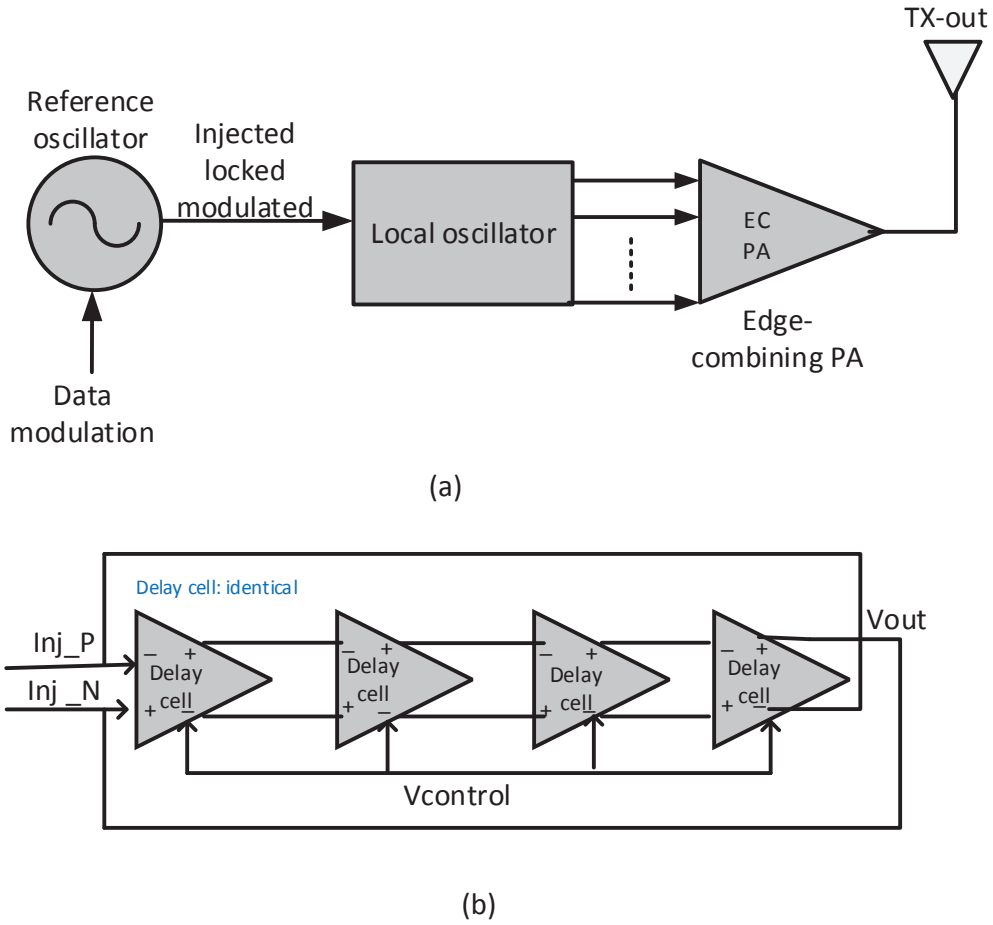


Figure 2.8: IL transmitter architectures (a) multi-phase injection locking and frequency multiplication (b) ILRO .

frequency ω_{osc}. The locking range increases with the ratio of (V_{inj}/V_{osc}). It also decreases with the quality factor Q. As can be seen in (2.11), a wide locking range (ω_L) is required to reduce the locking time (T_{Lock}), which means there is a trade-off between speed and power consumption in IL.

$$T_{Lock} = \frac{4}{\omega_L} \tag{2.11}$$

IL has been employed in different modulation schemes to achieve different purposes. In [29], IL was employed in OOK transmitters to provide an accurate

reference carrier, to improve the phase noise performance and the instabilities associated with ring oscillators. Fig. 2.8(a) shows the reported designs in [10, 30]. Injection locking ring oscillator (ILRO) was employed to provide PM. Ring oscillator is shown in Fig. 22.8(b), where a multiple delay cell with a positive feedback is used. Due to the nature of the cascaded stages in RO, it readily provides multiple phases without the need for a frequency divider. Typically, utilizing RO as a carrier generator can reduce power consumption but this limits output power and hence efficiency. Power consumption is not only a function of power supply, other factors like operating frequency and data rate are the real definers of the consumed power.

In [10] a very limited power efficiency of 3.36% is achieved despite the sub-milliwatt consumed power due to the low output power of -15 dBm. In [31] a high efficiency of 22% is reported at low data rate due to the low dissipated power of sub-micro watt. Even though the sub-micro watt power consumption sounds attractive, the very important figure of merit for energy/bit is not ultra-low with 0.45 nJ/bit. The reported transmitter in [32], operates at 900 MHz and 50 Mbps data rate while consuming 6 mW under a 1.8 V power supply. This high consumed power results from high power supply, high operating frequency and high data rate.

Employing IL to achieve PM (relying on RO) compromises the accuracy of the modulation. RO suffers from process, voltage and temperature (PVT) variation and sensitivity to mismatch lead to a phase error. This phase error directly impacts the modulation accuracy and results in higher EVM. Therefore, a calibration circuit is usually added to compensate for these effects. For example, in [32], a high EVM of 8.227% occurred without a calibration technique compared to a lower EVM of 3.8% in [10]. However, this circuitry is more complex, consumes extra die area and has a higher power consumption.

In [33, 34], the PM is achieved by using IL with LC-VCO. The difference between the injected signal and the self resonant frequency (SRF) of the LC tank sets the output phase to $\mp 45^o$. LC oscillators are more immune to mismatch, however, this technique has a limited phase tuning range. The other two phase shifts $\mp 135^o$ were still needed, so a polarity sweep circuit was added in both reported

works.

- Phase-Multiplexer-Based Transmitter

  Fig. 2.9 shows the analog phase MUX based transmitter reported in [9, 35]. The phase MUX is an over driven quadrature Gilbert cell for direct PM. The multiphase signals are provided by a carrier generator at an RF frequency. The baseband input selects the corresponding phase signal to the PA. These designs rely on RO as an oscillator. As explained in the previous section, this kind of oscillator it is highly sensitive to PVT variation (see Fig. 2.10), although it is very simple and consumes a low power and area. Furthermore, some non-ideal effects related to Gilbert cell are: quadrature mismatch and the offset of LO leakage that alter the duty cycle of the output signal and affect the modulation accuracy. In [36], the phase multiplexing concept was directly applied to an injection locked ring oscillator. Although a low power ring oscillator was employed, a relatively low data rate and high power consumption were reported due to the use of multiple cascaded digital power amplifiers stages that are used to perform the phase selection.

  Despite many building blocks like DACs and analog filters are eliminated in [35] to reduce power consumption, a 3.5 mW for data rate equals to 17.5 Mbps is reported. Note, the DC power consumption increases exponentially with the power supply and increases linearly with the frequency as expressed in (2.12) [37]. That means a 3.5 mW power consumption at 440 MHz carrier frequency is not as low as it should be. A very poor efficiencies of less than 5% in [35] and less than 10% in [9] were reported.

$$P_{DC} = C.V_{DD}^2.f \tag{2.12}$$

2.3 Recently Published WSN Transmitters

This section summarizes the recently published state of the art WSN transmitters. These transmitters are classified by the architectures described in the previous sections. Table 2.1 shows the key performance parameters of frequency up-conversion

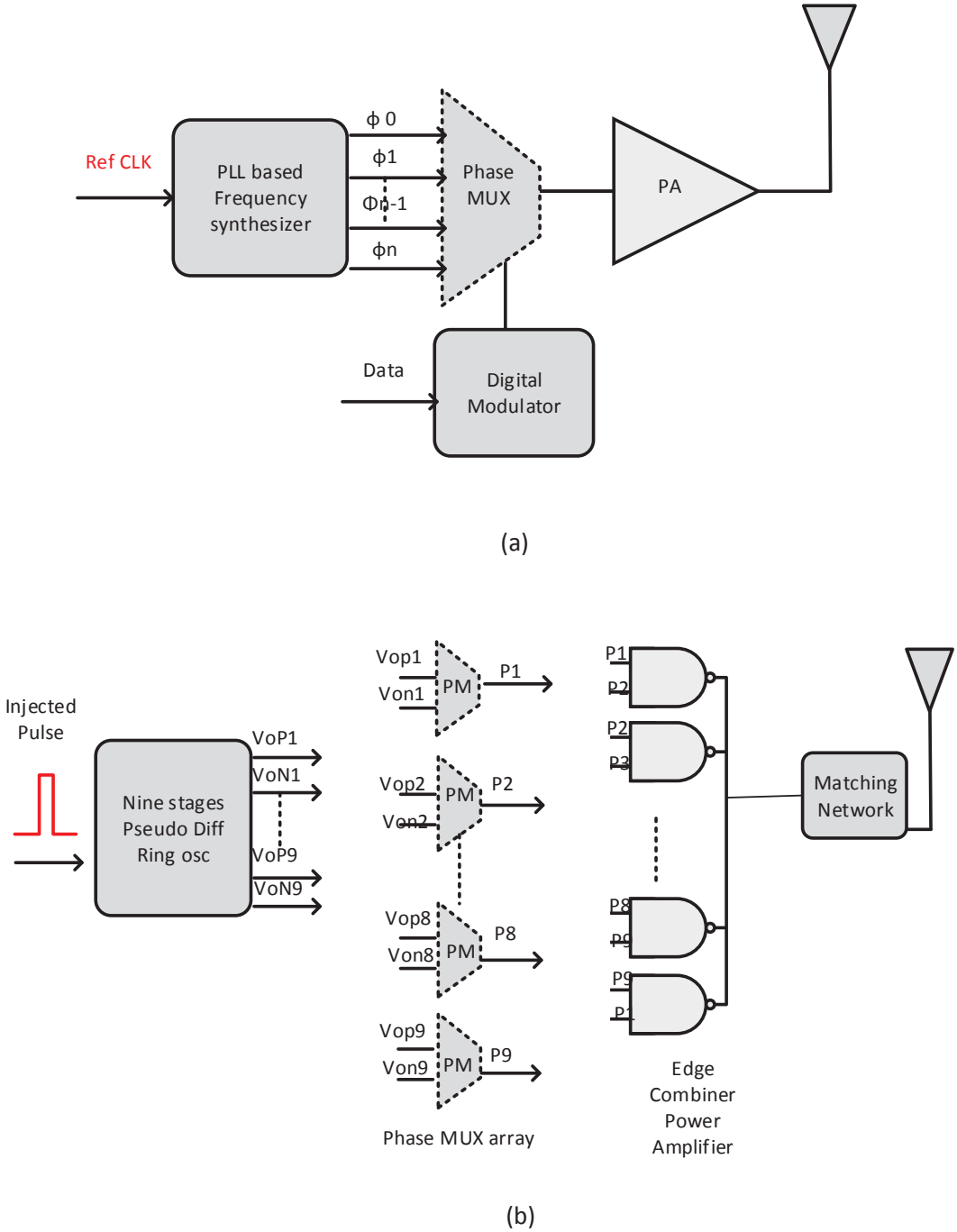


Figure 2.9: Block diagrams of MUX-based PSK transmitters (a) QPSK design (b) binary phase shift keying (BPSK) design.

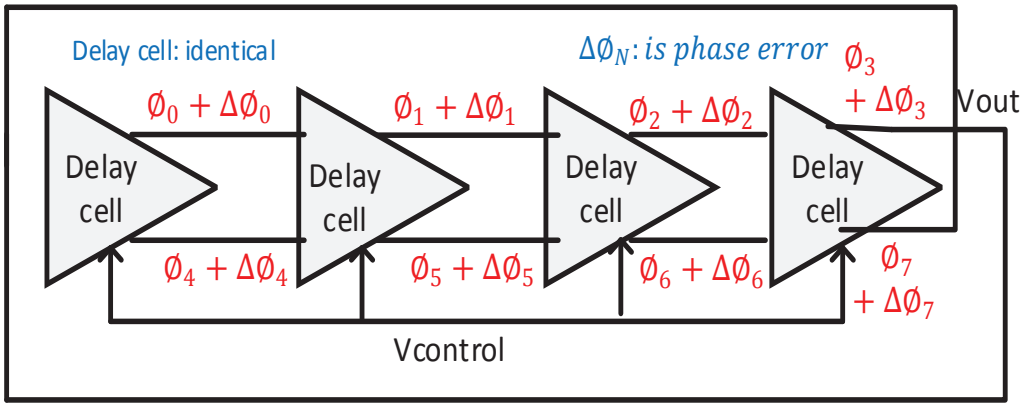


Figure 2.10: Block diagram of four-stages differential ring oscillator showing the phase shift and phase error.

WSN transmitters while Table 2.2 presents the same parameters for the direct modulation WSN transmitters.

The heterodyne transmitters consume more power than the direct modulation transmitters because of the extra circuit blocks as explained in the previous sections. The transmitters with radiated power below 0 dBm have an efficiency lower than 10%. The transmitters with a low radiated power have poor efficiency because they have a relatively high dissipated power.

For the direct modulation transmitters listed in Table 2.2 where the data rate is extremely low, the transmitters consume less power (sub-milliwatt), the efficiency is more than 10% in [30]. For a high radiated power more than 0 dBm, a high efficiency is achieved even with a high data rate. The direct modulation transmitters have less than 10% power efficiency when the radiated power is less than -3 dBm. Note, for an extremely low radiated power, the efficiency degrades even when the data rate is low and the transmitter consumes low power.

Table 2.1: Performance summary of recently published frequency up-conversion WSN transmitters.

Ref	Technology	Frequency	Power consump	Radiated power	Efficiency (%)
[38]	0.18μm	405 MHz	1.87 mW	-12 dBm	3.34
[39]	0.13μm	915 MHz	2.7 mW	-6 dBm	9.26
[40]	0.18μm	400 MHz	11.7 mW	3 dBm	17
[41]	65 nm	5.8 GHz	2.86 mW	-31	0.027
[42]	0.13μm	2.4 GHz	18.2 mW	-8.7	0.6

Table 2.2: Performance summary of recently published direct modulation WSN transmitters.

Ref	Technology	Frequency	Power consump	Radiated power	Data rate	Efficiency (%)
[30]	0.13μm	400 MHz	0.09 mW	-16.9 dBm	200 Kbps	22
[9]	0.18μm	400 MHz	0.33 mW	-15	20 Mbps	9
[10]	65 nm	915 MHz	0.93 mW	-15 dBm	55 Mbps	3.2
[12]	0.18μm	400 MHz	2.6 mW	-8 dBm	4 Mbps	5.7
[32]	0.18μm	915 MHz	5.9 mW	N/A	50 Mbps	N/A
[33]	0.18μm	915 MHz	5.88 mW	-3.3 dBm	50 Mbps	7.8
[43]	0.13μm	2.4 GHz	8.9 mW	1.9 dBm	1 Mbps	16.8
[44]	0.18μm	400-406	0.425	-10.8	0.06	19.3

2.4 Summary

Different RF transmitter's architectures were reviewed. Performance specifications were discussed. Focusing on direct phase modulation, the architectures were described. The drawbacks of these architectures were discussed. Previous state of the art transmitter designs were listed and compared. These comparisons revealed that low power budget transmitters typically had a limited power efficiency.

Chapter 3

A 2.4 GHz Energy-Efficient CMOS Power Oscillator (Methodology and Circuit Design)

This chapter introduces and develops an alternative design for a class-E power oscillator circuit. In this work two types of power oscillators were developed, the first oscillator is presented in this chapter. The second oscillator is part of a QPSK transmitter which is presented in Chapter 4. This chapter presents a new energy-efficient power-oscillator in 65nm CMOS technology under an ultra-low power supply at a 2.4 GHz. This work is developed in [22]. The oscillator is tunable between 1.66 GHz to 2.78 GHz using dual varactors under a 0.4 V power supply and 2.4 mW power consumption. The oscillator is robust to $\mp 15\%$ frequency deviation from a 2.44 GHz nominal frequency due to PVT variation. The proposed oscillator demonstrates a maximum output power of -0.45 dBm, a peak efficiency of 37.5% and a phase noise of -108 dBc/Hz at 1 MHz offset frequency.

This chapter is organized as: Section 3.1 presents an overview of the VCO design, Section 3.2 describes the class-E power amplifier circuit design. The high efficiency requirements in power amplifiers design are discussed in Section 3.3. Section 3.4 introduces the power oscillator concept and methodology. Section 3.5 presents the circuit design of a class-E power oscillator. The simulation results are demonstrated in Section 3.6. Finally, Section 3.7 draws a summary.

3.1 Introduction

The VCO is a very important building block in communication systems. It is used in different applications either as a carrier frequency generator or as a clock for the digital circuits. The VCO's characteristics limit the transmitter performance in a direct modulation scheme. This is clearer in limited power budget applications. An energy efficient and a high-power oscillator is increasingly required.

The power oscillator is a self oscillating power amplifier (PA). Several power oscillators in CMOS technology were reported in the literature [45–47]. In [45], a relatively good efficiency is achieved, however it consumes a high power. While in [48, 49], a very limited tuning range is achieved to maintain a high output power since the frequency tuning is limited by the loop gain of the circuit.

Note, the PA is categorized to several classes depending on the voltage and the current waveform at the drain. These classes are: A,B,C,D,E and F. In classes A,B and C, the output voltage and the current are sinusoidal and that limits the efficiency. Classes A and B (the transconductance amplifier) are linear but they have low efficiency due to overlapping between the voltage and the current. While for the switching amplifiers (Classes D, E and F) in theory the efficiency reaches 100%.

The switching PAs are preferred in many applications due to their high efficiencies, specifically a class-E PA due to its simple circuit. Indeed, the efficiency and the output power are the most important key design parameters in PAs. In low power budget applications, the output power is critical to maintain a reasonable transmission range and to achieve a low bit error rate. The transmitter total operation time (t_{op}) is limited by the PA efficiency (η_{PA}).

$$t_{op} = \eta_{PA} \frac{E_{ava}}{P_{DC}} \tag{3.1}$$

Where E_{ava} is the available transmitted energy and P_{DC} is the total consumed power. An energy efficient class-E power oscillator with reasonable output power and a wide tuning range that is suitable for direct modulation is targeted in this dissertation.

3.2 Class-E Power Amplifier

The class E-PA was first introduced by Sokals in 1975 [50], with ideal efficiency 100%. Fig. 3.1(a) shows a class-E PA circuit. It includes a single NMOS transistor M_1 which acts as a switch and a series resonant filter composed of L_{res} and C_{res} that passes the fundamental sinusoidal to the load. The RF choke inductor L_{choke} connects the DC voltage supply with M1 to allow a DC current to flow. C_p is the parasitic capacitance of M_1 and the antenna is modeled with a 50 Ω load resistance R.

When the switch is closed as depicted in Fig. 3.1(b), the current flows from the power supply (VDD) through L_{choke} and through the switch to the ground. When the switch is open as shown in Fig. 3.1(c), the current continues to flow from the stored energy in the inductor to C_p and R. In operation, the switch will be toggled between on and off.

Sokal made two assumptions or conditions to minimize the power dissipation by the switch. The first condition is the zero voltage switching (ZVS) condition, where the voltage across the MOS switch should be minimized when the current flows. The current should be minimized whenever non zero voltage occurs across the switch. The second condition is the zero voltage derivative switching, (ZVDS) condition where the switching time when the voltage and the current are on, has to be minimized. The non overlapping drain current and voltage waveforms are demonstrated in Fig. 3.1(d). When the switch is turned off, all the switch current will be transferred to the shunt capacitor and this will result in a high peak drain voltage theoretically equal to (3 VDD) [50]. A single transistor class-E PA under a 1.1 V power supply can exhibit a 3.8 V drain swing. This is much higher than the oxide breakdown voltage in CMOS technology. The low breakdown voltage in the nanometer technology is a challenging issue in designing CMOS PAs.

The CMOS technology and the limited power budget usually result in poor efficiency compared to other technologies. For example, PAs with an output power of the order of 1 watt have high efficiency around 65% [51, 52] in which power MOSFET is used in the PAs design. However, for PAs with milli-watt output power level, low efficiency around 10% is usually reported [53–55]. In [56, 57] a class-E PA is implemented in a GaAs technology. The higher break-down voltage in a GaAs helps to use high power supply and this results in higher efficiency.

3.3 High Efficiency Class-E PA Design

The design of the PA starts by selecting the MOS size depending on the power supply and the power consumption requirements. Although the MOSFET transistor in a class-E PA is modeled as an ideal switch, in reality there is no ideal switch. Therefore, using MOSFET results in some associated on-resistance (r_{on}) that degrades the efficiency.

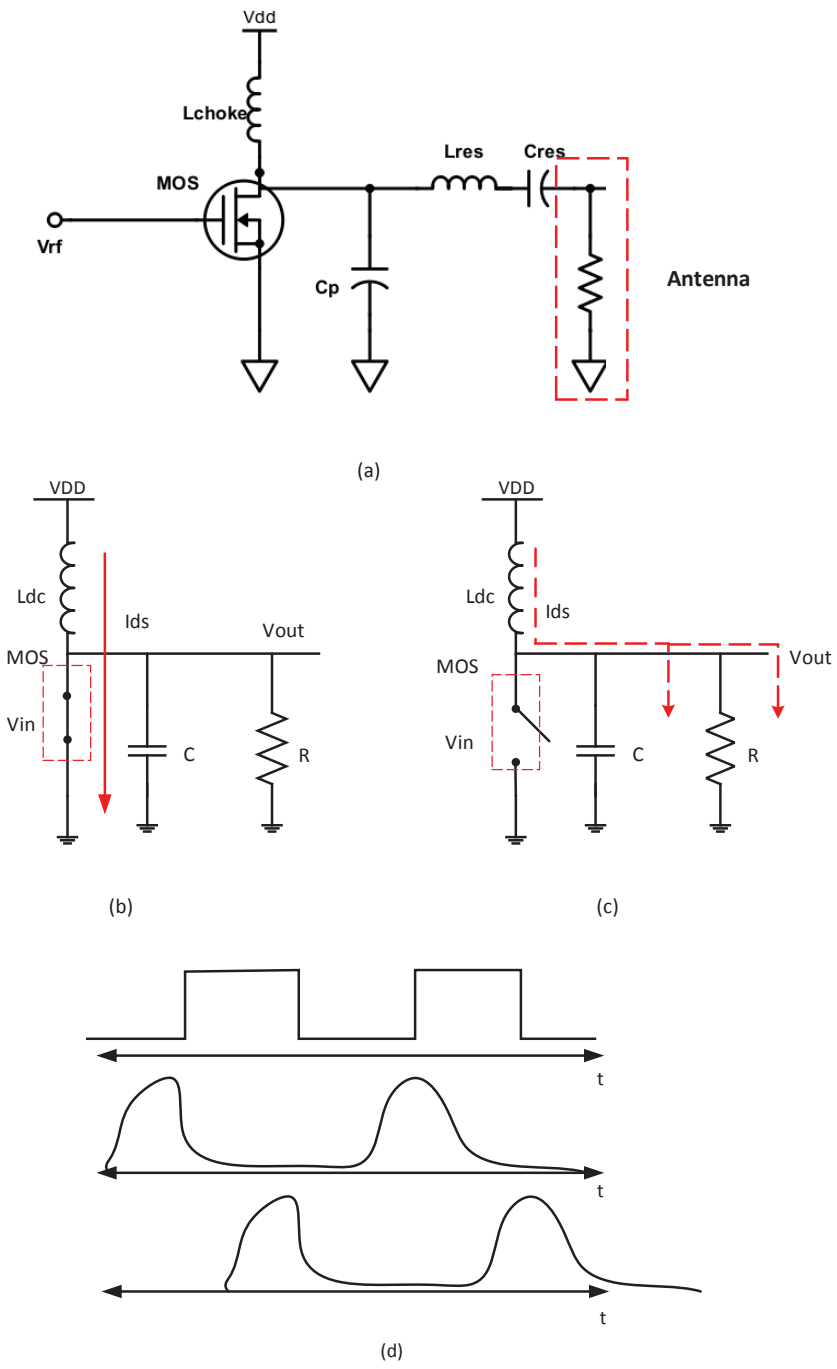


Figure 3.1: Class-E PA (a) circuit design (b) when the MOS switch is closed (c) when the MOS switch is open (d) the input RF, voltage and current waveforms plot.

$$r_{on} = \frac{L}{\mu_n C_{ox} W (V_{gs} - V_{th})^2} \tag{3.2}$$

Where L is the channel length, μ_n is mobility of N-FET $cm^2/(Vs)$, C_{ox} is the oxide capacitance per unit gate area (F/m^2) and V_{th} is the threshold voltage. The losses associated with r_{on} are studied by Sokals and Raab and can be found as:

$$P_{loses-ron} = 1.3365 \ \frac{r_{on}}{R} \ P_o \tag{3.3}$$

where P_o is the output power and R is the load impedance.

To increase the PA output power, enlarging the MOS size is the most intuitive approach. However, MOS size can not be increased unlimitedly. Fig. 3.2(a) shows the output power and the efficiency of a class-E PA as a function of the transistor width. As expected, the output power increases almost linearly with the MOS size. The efficiency increases linearly due to the reduced r_{on} and to the improved ratio of (r_{on}/R) as expressed in (3.4). However, after the 80 μm size, the efficiency starts to decline. Fig. 3.2(b) demonstrates the relation between the power consumption (P_{dc}) of a class-E PA and the dimension of the device with respect to Vdd. It shows that the power consumption directly rises with larger devices and a higher Vdd. However, the increment in the dissipated power for a higher Vdd is significantly more than the dissipated power in larger devices. For instance, there is a 0.3 mW increment in P_{dc} for every 10 μm increment in the MOS width under a 0.5 V supply, while a 2 mW increment in P_{dc} occurs under a 1.2 V power supply and the same MOS size.

$$\eta_{PA} = \frac{1}{1 + 1.4(r_{on}/R_L)} \tag{3.4}$$

Increasing the MOS width improves the transconductance (g_m) to increase the gain. Fig. 3.3 shows the relation between g_m and r_{on} for varying MOS width. Note that the optimum MOS width for a high g_m has the lowest r_{on}.

On the other hand, larger devices increase the associated parasitic capacitances seen at the gate, as can be found in (3.5). The large MOS devices limit the maximum operating frequency and increase the required power to drive the PA as can be seen in (3.6), and this leads to more power consumption. Therefore, selecting the optimum

dimension for the transistors is critical due to constraints imposed by the resources and by the CMOS technology.

$$f_{max} = 0.0798 \frac{P_{out}}{C_{drain} V dd^2} \tag{3.5}$$

$$P_{drive} = f.C_G.V_{gs} \tag{3.6}$$

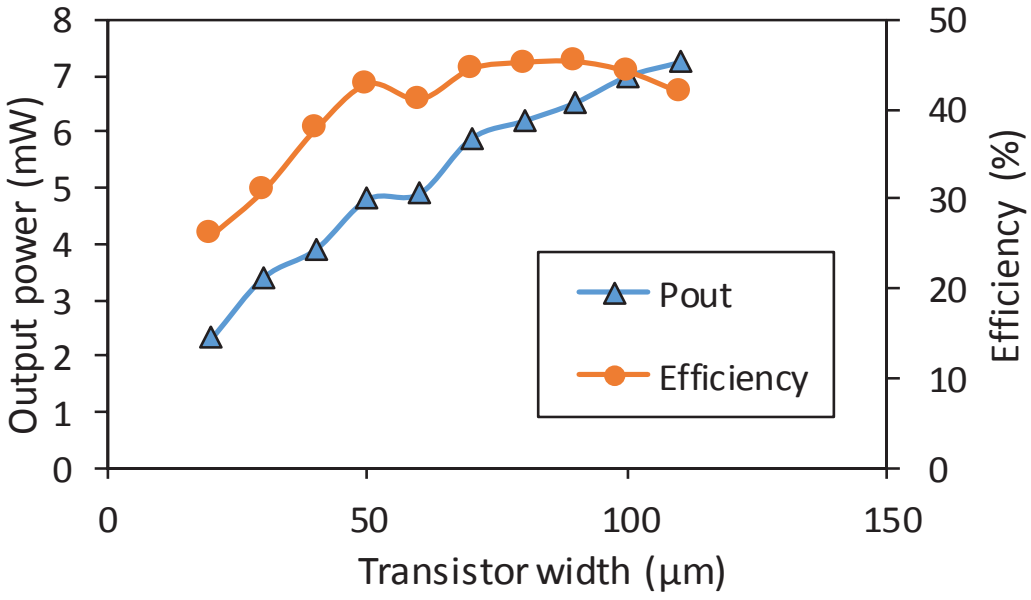
Where f is the operating frequency, C_G is the total capacitance seen at the gate, V_{gs} is the gate voltage of the PA transistor and C_{drain} is the total capacitance seen at the drain.

The high drain voltage swing is critical in PAs and it must be well controlled in CMOS devices. Fig. 3.4 represents the drain voltage swing in a class-E PA for a varying MOS width, multiple Vdd and a varying gate voltage (V_{gs}). As shown in Fig. 3.4 (a), the drain voltage increases as the MOS width and Vdd increase. Note, the drain swing becomes more prominent in larger transistors under a high power supply. For example, for a 50 μm MOS width and a 0.6 V power supply, the drain swing is 1.1 V, while for a MOS width equal to 100 μm and 1.2 V power supply, the drain swing is 2.6 V.

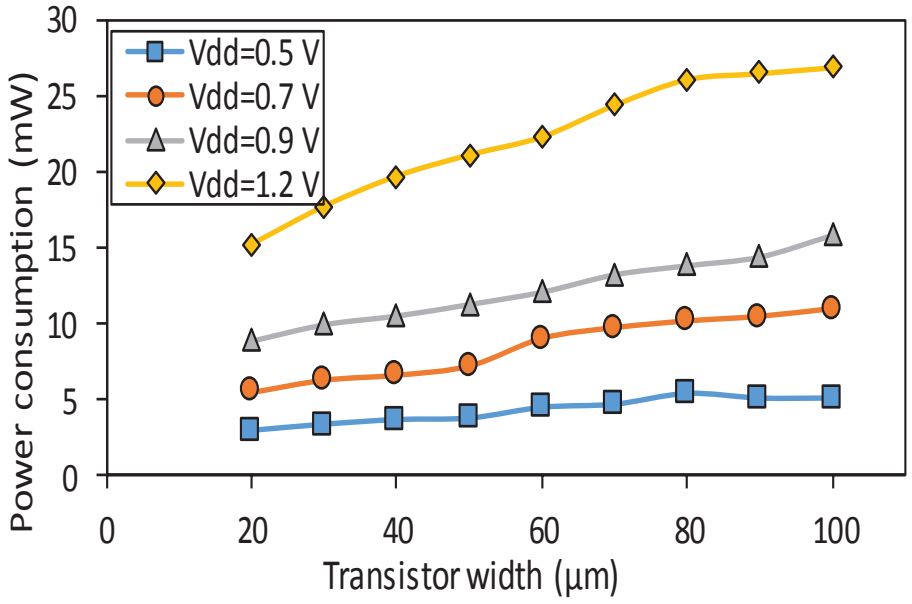
Fig. 3.4 (b) demonstrates the relationship between the gate voltage and the drain swing for 50 μm MOS width and Vdd varies between 0.9 V and 1.1 V. Although there wasn't much change in the drain swing for a higher Vdd, the drain voltage increased linearly as V_{gs} increased from 0.5 V to 1 V.

The load impedance R_L is determined by the output power requirement as can be seen in (3.7). The efficiency can be improved by increasing R_L. However, this increment can not be unlimited. Fig. 3.5 demonstrates the relationship between the load impedance with the output power and the efficiency. Note that the output power and the efficiency increase with high load impedance below 50 Ω however, there is no reasonable increment after 50 Ω.

$$R_L = 0.577 \frac{V_{dd}^2}{P_{out}} \tag{3.7}$$



(a)



(b)

Figure 3.2: The class-E PA (a) output power and efficiency versus MOS dimension under 0.9 V power supply and 50Ω load impedance (b) DC power consumption of PA versus MOS dimension and Vdd.

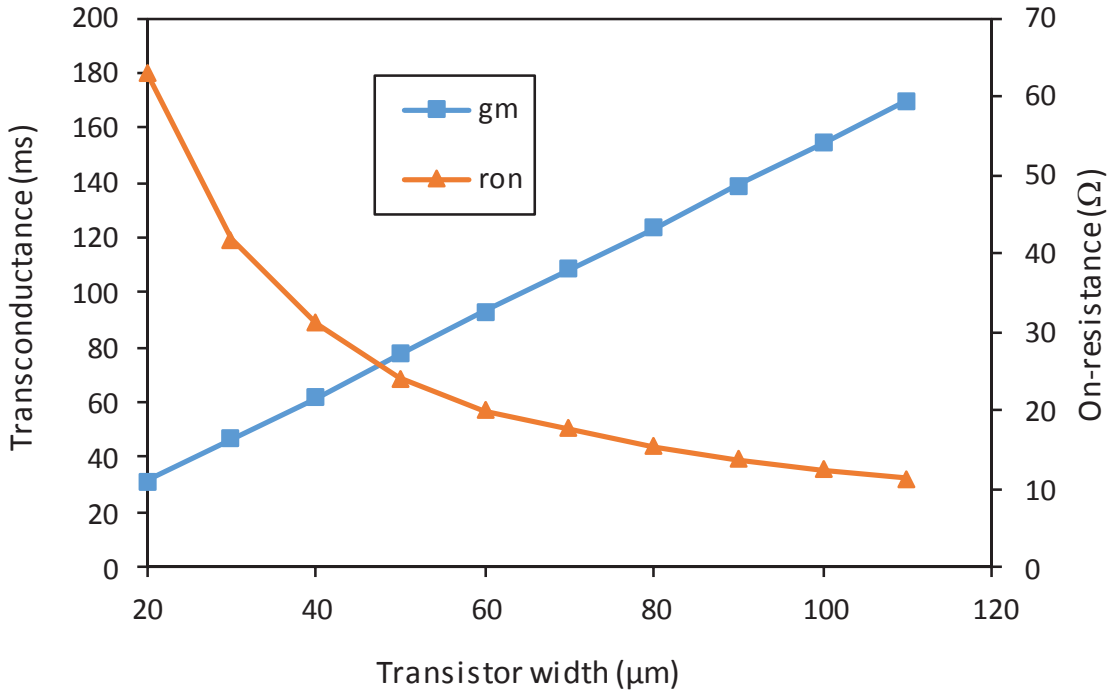


Figure 3.3: The PA transconductance and on-resistance relationship with MOS width.

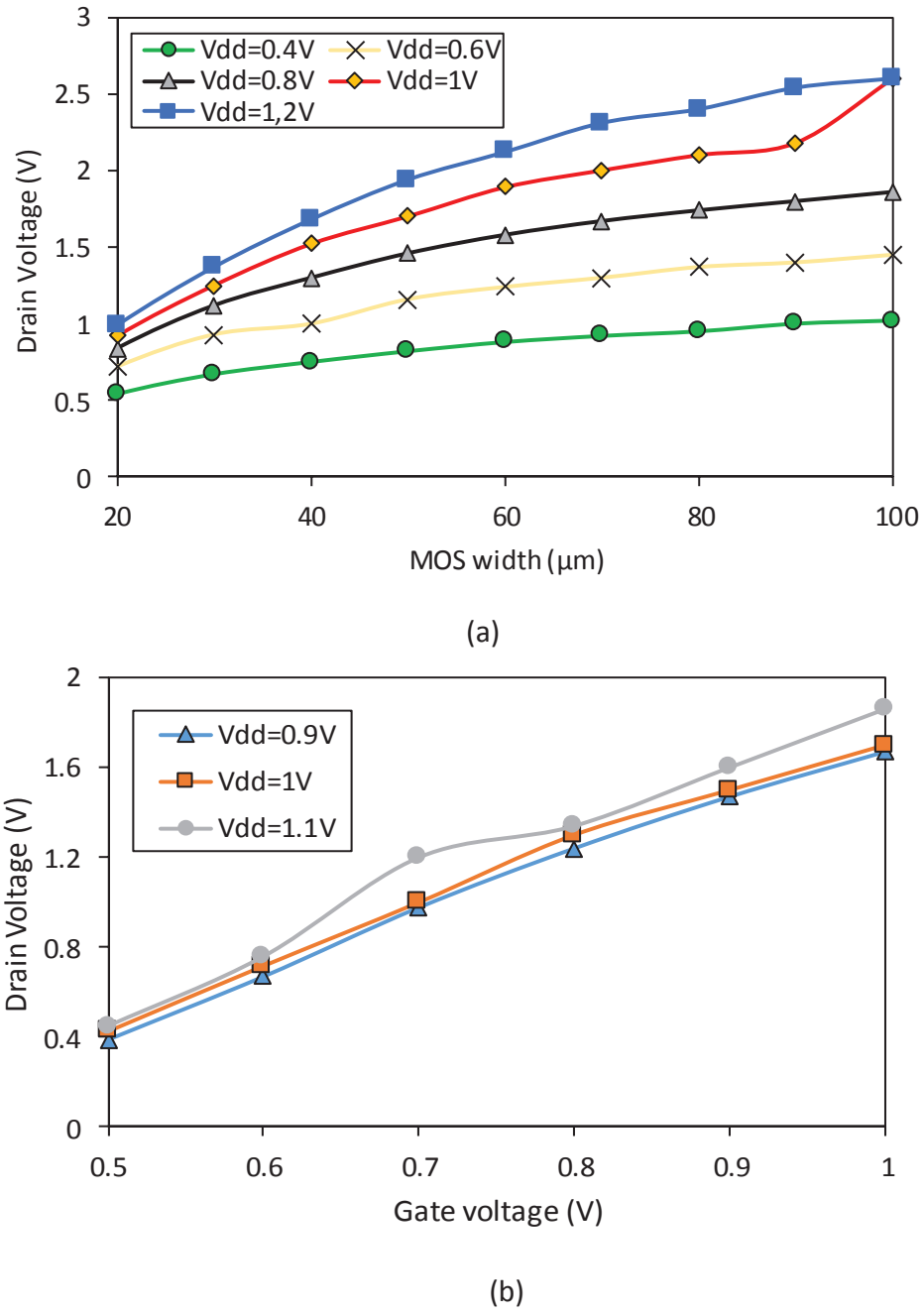


Figure 3.4: The class-E PA drain swing for Vgs voltage equals to 1 V (a) versus MOS dimension and Vdd, Vgs= 1 V (b) versus gate voltage and Vdd.

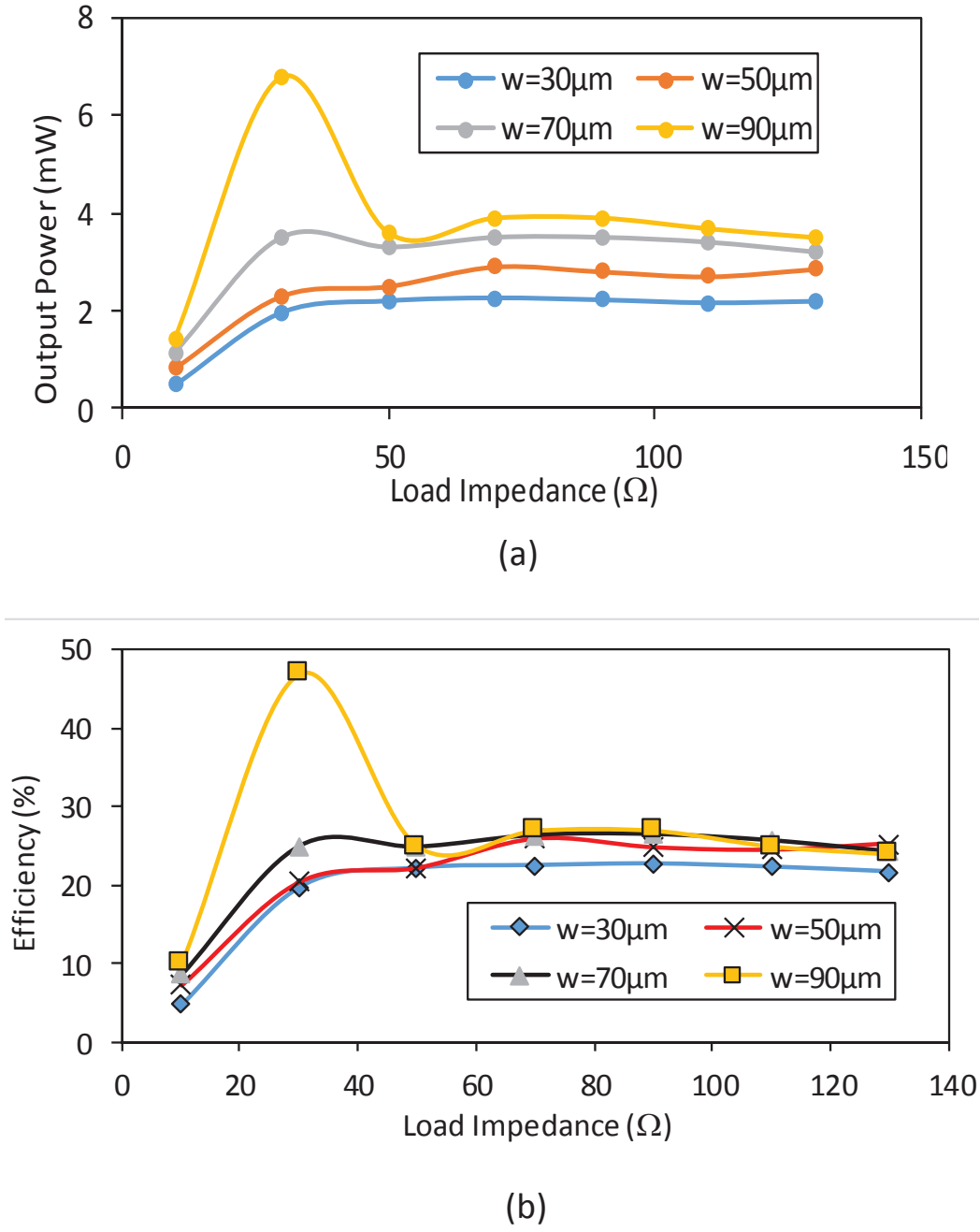


Figure 3.5: The oscillator output power and efficiency versus the load impedance for different transistor widths.

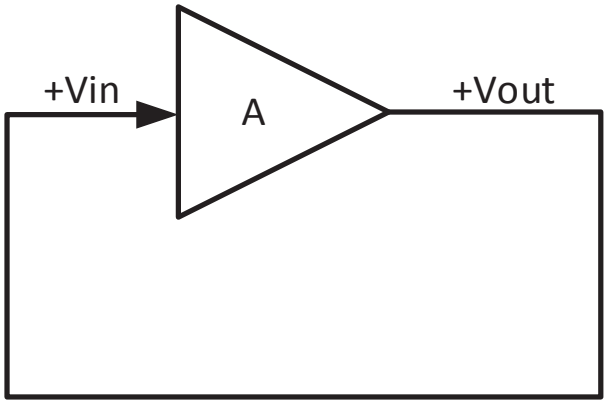


Figure 3.6: The proposed oscillator block diagram.

3.4 Design Methodology

The oscillator is a closed-loop system that sustains a periodic output signal due to a positive feedback. The power oscillator is a self oscillating PA that amplifies its own noise and oscillates at ω_o. Recall that any closed-loop system with a positive feedback where A is the forward gain and β is the feedback gain can be represented by the following transfer function:

$$H(s) = \frac{A}{1 - A\beta} \tag{3.8}$$

The Barkhausen criterion states two conditions for stable sustained oscillation:

$$magnitude = |A\beta| \ > \ 1 \tag{3.9}$$

$$phase = \angle A\beta = 2.n.\pi \tag{3.10}$$

where n is any integer.

The proposed closed-loop system of a class-E power oscillator is shown in Fig. 3.6. The network A includes two stages: the class-E PA and a pre-amplifier stage this is necessary to provide the required $(2\pi n)$ phase shift to sustain the oscillation and to

maintain enough gain for the oscillation during frequency tuning, while maintaining low dissipated power. Two choices are available to serve this purpose: 1) the use of an inverter as a pre-amplifier stage which will be discussed in this chapter, 2) the use of a common source amplifier as a pre-amplifier stage (this will be discussed in detail in the following chapter). The network β is a unity.

Fig. 3.7 depicts the model of the closed- loop system where a class-E PA is modeled as a transconductance ($-G_m$) amplifier and a series RLC circuit with an equivalent impedance ($Z(s)$). The inverter stage is modeled as a gain stage -1. The series RLC circuit can be expressed as:

$$Z(s) = \frac{R}{L_{res}} \frac{s}{s^2 + (R/L_{res})s + 1/LC_{res}} \tag{3.11}$$

The loop gain is:

$$G_{loop}(s) = G_m \frac{R}{L_{res}} \frac{s}{s^2 + (R/L_{res})s + 1/LC_{res}} \tag{3.12}$$

The closed-loop transfer function is:

$$\frac{vout(s)}{vin(s)} = \frac{G_m \frac{R}{L_{res}} \frac{s}{s^2+(R/L_{res})s+1/LC_{res}}}{1 - G_m \frac{R}{L_{res}} \frac{s}{s^2+(R/L_{res})s+1/LC_{res}}} \tag{3.13}$$

$$\frac{vout(s)}{vin(s)} = \frac{G_m \frac{R}{L_{res}} s}{s^2 + (1 - G_m)\frac{R}{L_{res}} s + \frac{1}{LC_{res}}} \tag{3.14}$$

The closed-loop complex-conjugate poles are:

$$S_{1,2} = \frac{-(\frac{R}{L_{res}})(1 - G_m) \mp \sqrt[2]{((1 - G_m)(\frac{R}{L_{res}}))^2 - \frac{4}{LC_{res}}}}{2} \tag{3.15}$$

Figure 3.8 demonstrates the oscillation process and the relationship between the poles location and the transient response. When the poles are located on the left half of the s-plane, the system is stable. When the poles are located on the right half of the s-plane the system is not stable and starts to oscillate. When the poles are located on the imaginary axis the system reaches stead-state oscillation. Root locus plot is used to show the trajectory of the closed-loop poles in the complex s-plane as shown in Fig.3.9. When $G_m \frac{R}{L_{res}} > 1$, the poles have positive real part and are located

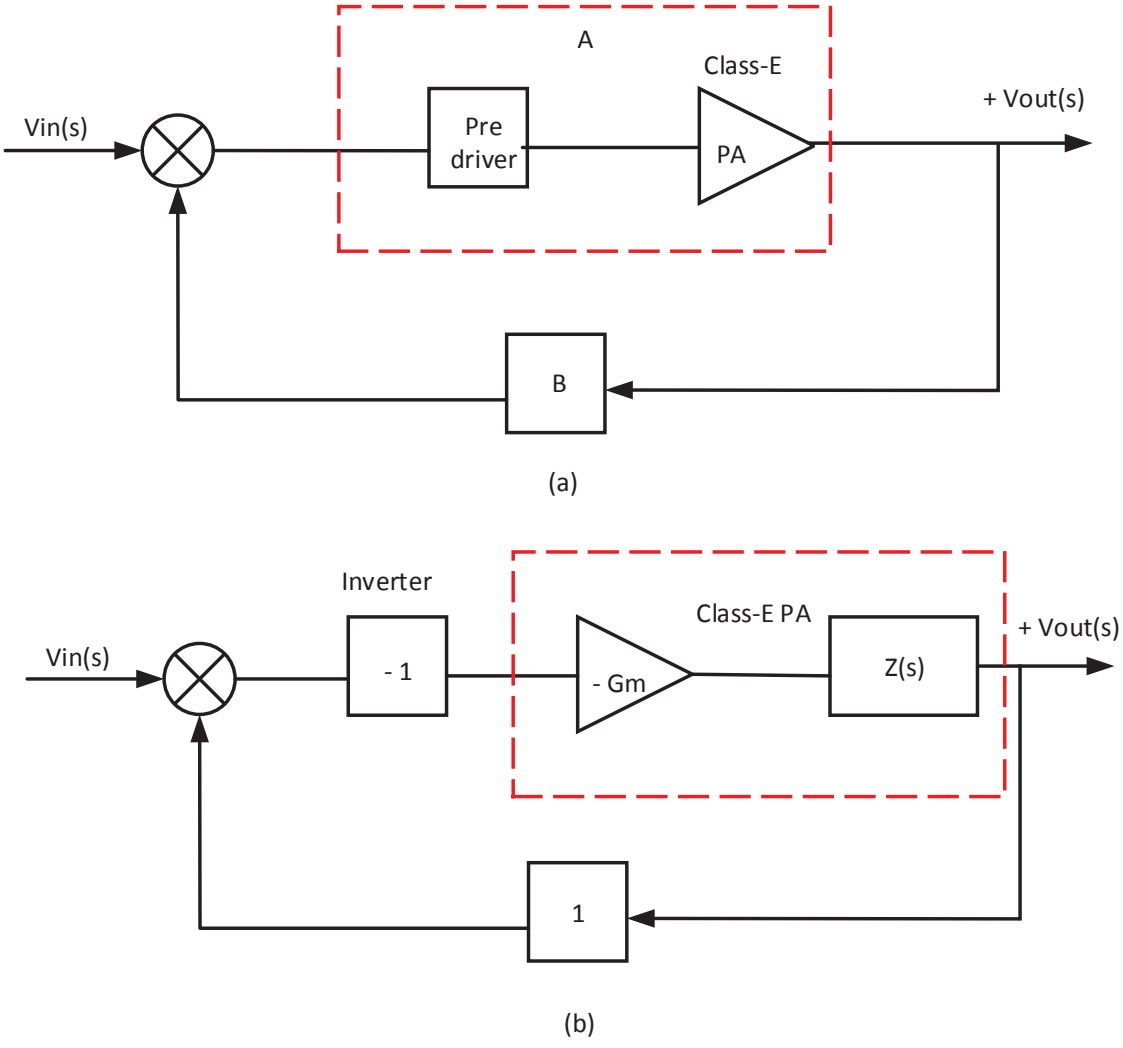


Figure 3.7: The feedback model of a class-E power oscillator (a) the block diagram (b) the detailed closed-loop system.

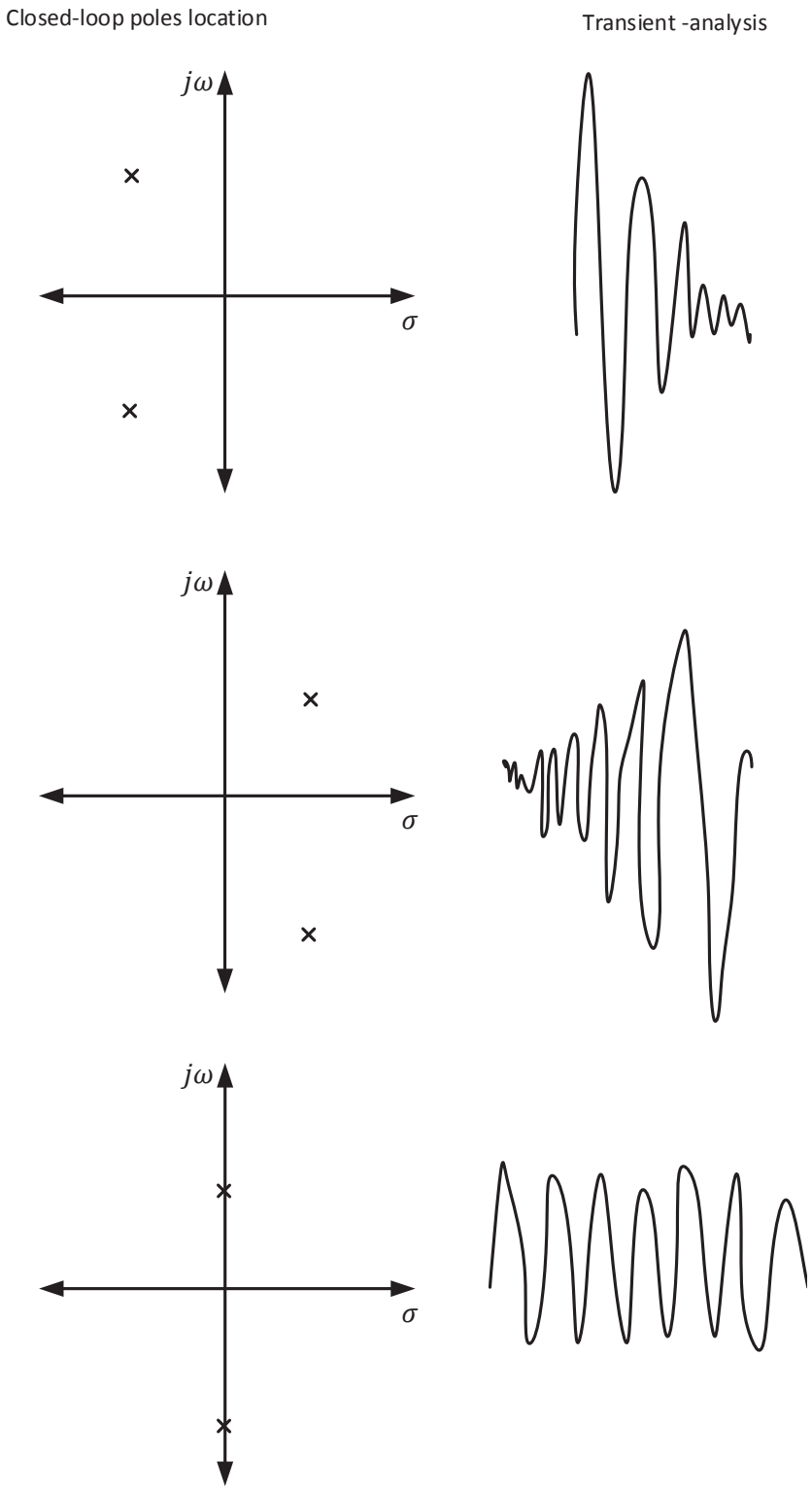


Figure 3.8: The poles' location and transient analysis relationship.

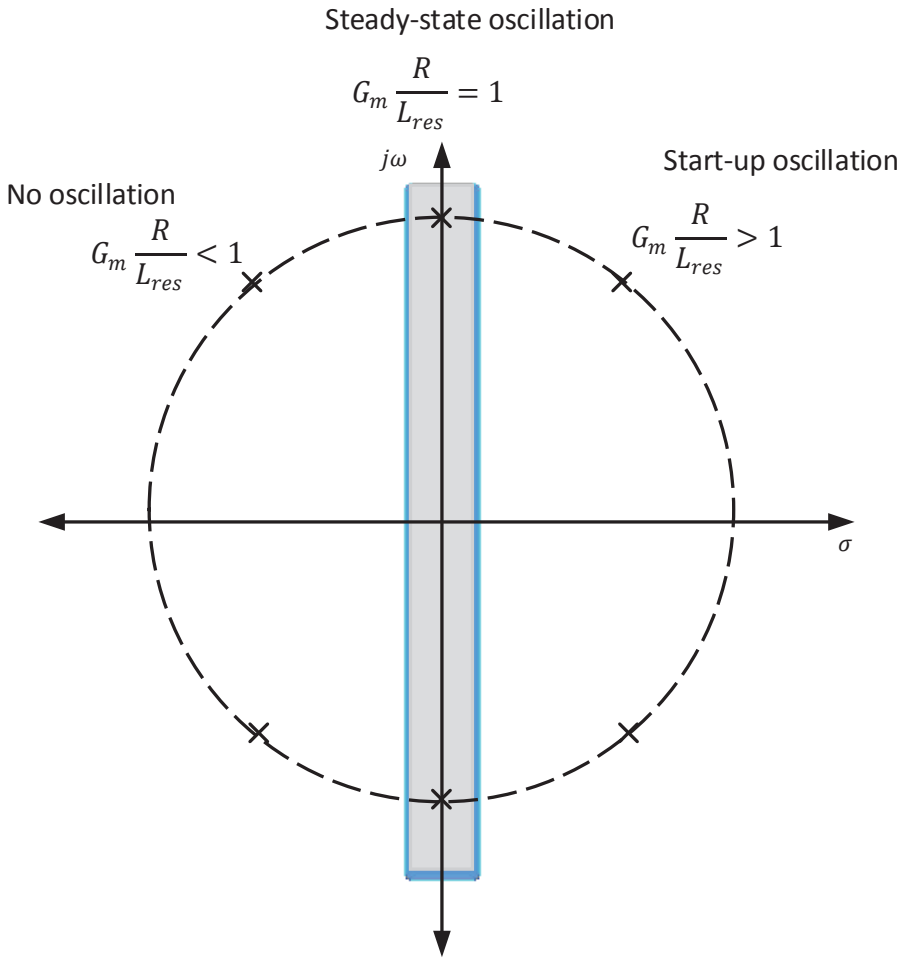


Figure 3.9: The root locus analysis of the closed-loop poles.

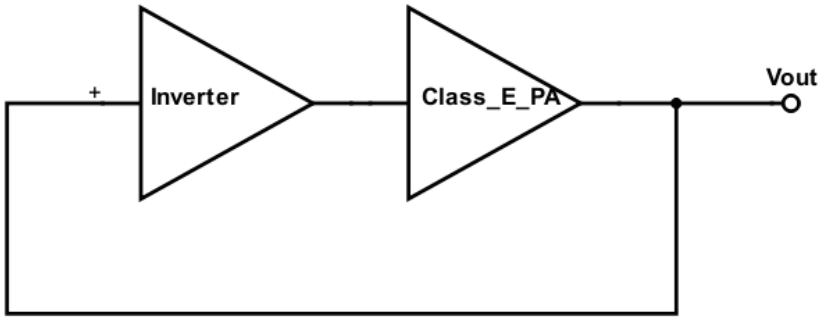


Figure 3.10: The class-E power oscillator block diagram.

on the right half of the s-plane. When $G_m \frac{R}{L_{res}} = 1$, the poles only have an imaginary part and are located exactly on the imaginary axis. When $G_m \frac{R}{L_{res}} < 1$, the poles have a negative real part and are located on the left half of the s-plane. To start the oscillation, $G_m \frac{R}{L_{res}}$ has to be greater than one where the oscillation amplitude starts to grow exponentially. Due to the MOSFET nonlinearities, the poles go back to the imaginary axis and the oscillation reaches a steady-state.

3.5 The Power Oscillator Circuit Design

The self-oscillating PA is depicted in Fig. 3.10. It comprises a class-E PA and a tuning circuit with an inverter as a pre-amplifier. The detailed architecture of the proposed power oscillator is demonstrated in Fig. 3.11. We have considered a single-end structure and made a careful choice of its parameters. The inverter is implemented with the transistors M_2 and M_3 with 15 μm and 10 μm width respectively. A 0.9 V power supply is selected to maintain a minimum power dissipation at the inverter stage.

The two on-chip inductors are: L=4.18 nH and L_{res}=1.1 nH. In our work, the maximum current through the PA is set to a peak value 7 mA. The optimum width for the PA transistor M_1 is 50 μm. A 0.4 V power supply is selected to control the drain swing and minimize power consumption. The load impedance (R_L) is set to be 50 Ω.

The wide frequency tuning is important not only to compensate for PVT variation, but also it is critical for the proposed new modulation technique (this will be explained in the next chapter). The frequency tuning is limited by the loop gain of the circuit. Therefore, a small tuning range is selected to reduce the voltage division ratio. To vary the oscillation frequency in series configuration, a large off-chip inductor L_{bias} that provides a DC bias voltage is used. The frequency tuning is implemented by using a varactor bank. Fig. 3.12 shows the tuning structure of the power oscillator. The varactor bank includes a MIMCAP with the capacitance C_{fix} in parallel with a dual varactor pair C_{var}. C_{fix} maintains an AC path from the input to the output, while the varactor pair provides the frequency tunability. The value of C_{fix} and C_{var} have been chosen properly to allow frequency tunability without degrading the gain.

$$C_{eff} = C_{fix} + \frac{C_{var}}{2} \tag{3.16}$$

The effective capacitance C_{eff} varies with a ratio equal to $C_{max}/C_{min} = 1.7$ to tune the frequency between 1.6 GHz and 2.7 GHz when the control voltage ($V_{control}$) changes between 0 V and 1.5 V, where C_{fix}=0.3 pF, V_{bias}=0.4 V and L_{bias}=100 nH, such that:

$$f = \frac{1}{2\pi\sqrt{L_{res}\ C_{eff}}} \tag{3.17}$$

3.6 Implementations and Results

The proposed oscillator is implemented in CMOS 65 nm. The layout photograph is shown in Fig.3.13. The core of the VCO occupies an active area of about 0.16 mm^2. Fig. 3.14 illustrates the oscillation amplitude at the time domain. The circuit starts to oscillate after 3 ns with peak-peak value equal to 300 mV (at Vcontrol=0 V). The drain voltage swing and the switching behavior of the PA is shown in Fig. 3.15. Table 3.1 summarizes the breakdown of the oscillator power consumption and the total power consumption with a 2.4 mW.

Fig. 3.16(a) represents the simulation results of the tuning range. It is from 1.66 to 2.7 GHz under a tunable control voltage of 0 V to 1.5 V and a supply voltage of

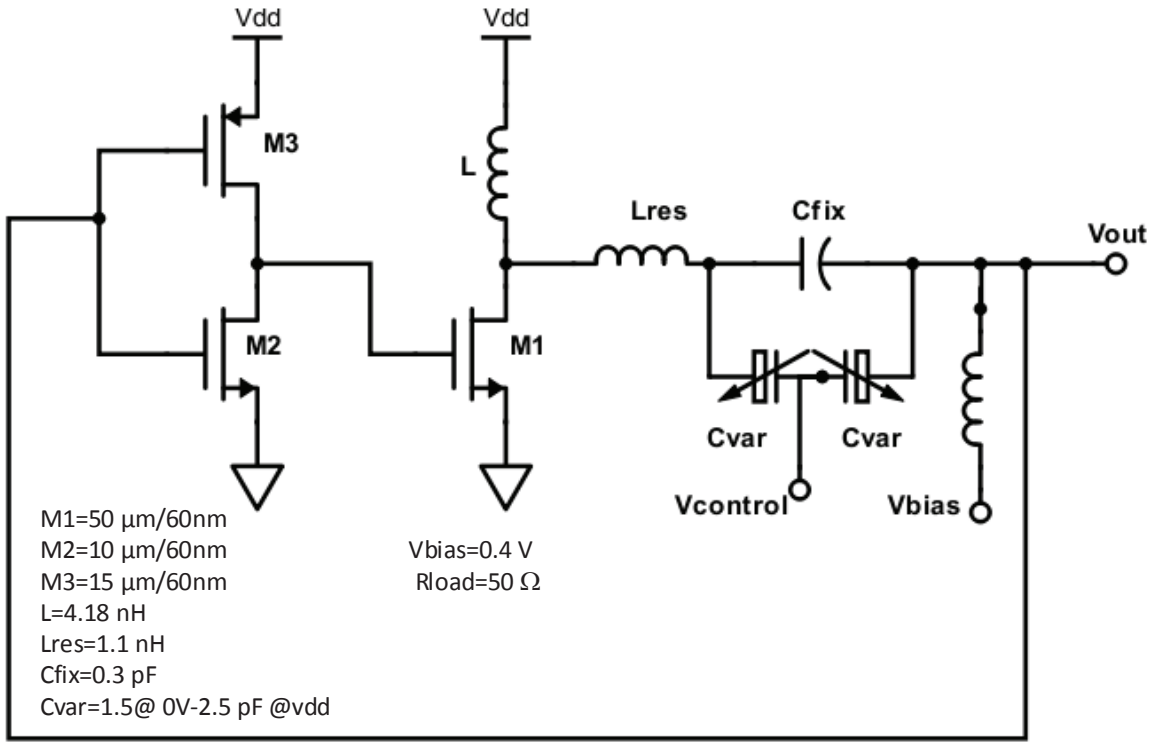


Figure 3.11: The proposed class-E power oscillator circuit design.

Table 3.1: Power consumption breakdown.

Circuit block	power consumption (mW)
Class E power amplifier	1.9, Vdd=0.4V
pre-amplifier	0.5, Vdd=0.9V
Total	2.4

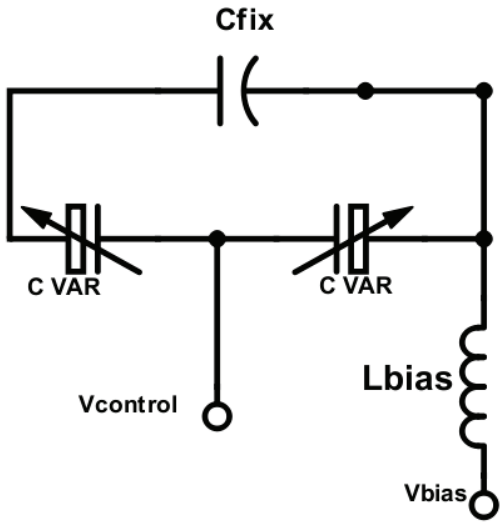


Figure 3.12: Single end tuning structure in the power oscillator.

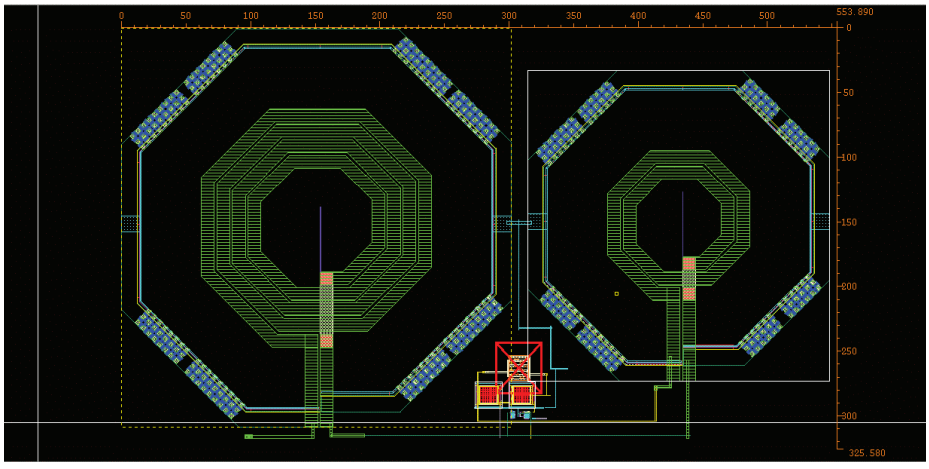


Figure 3.13: Photograph of the proposed oscillator.

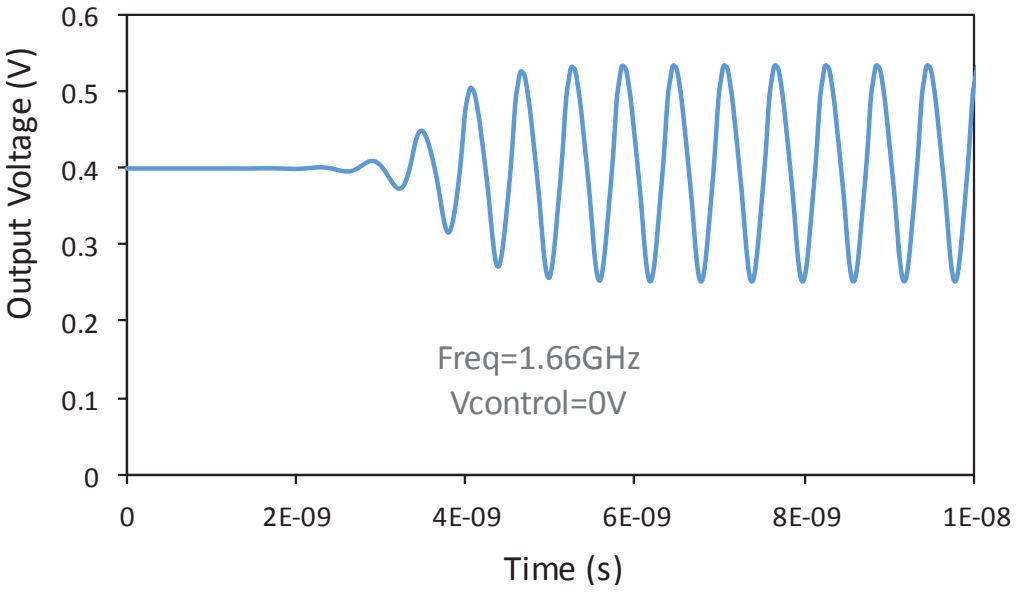


Figure 3.14: The transient analysis of the oscillator output voltage.

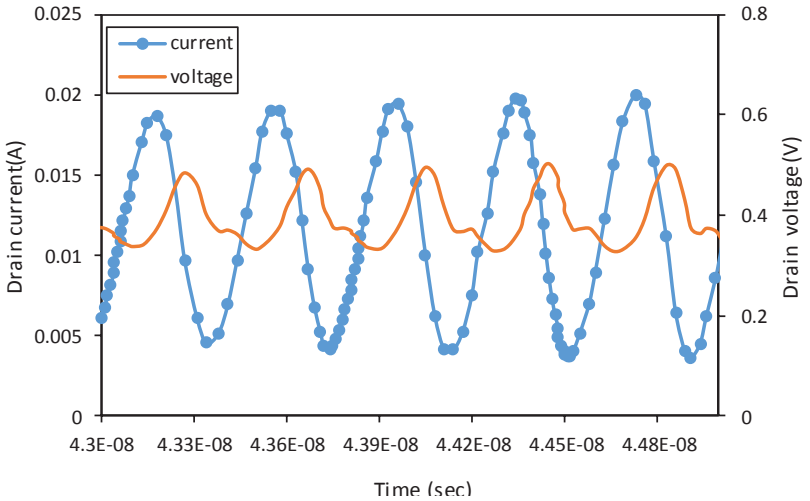


Figure 3.15: The voltage and the current curves of the PA drain.

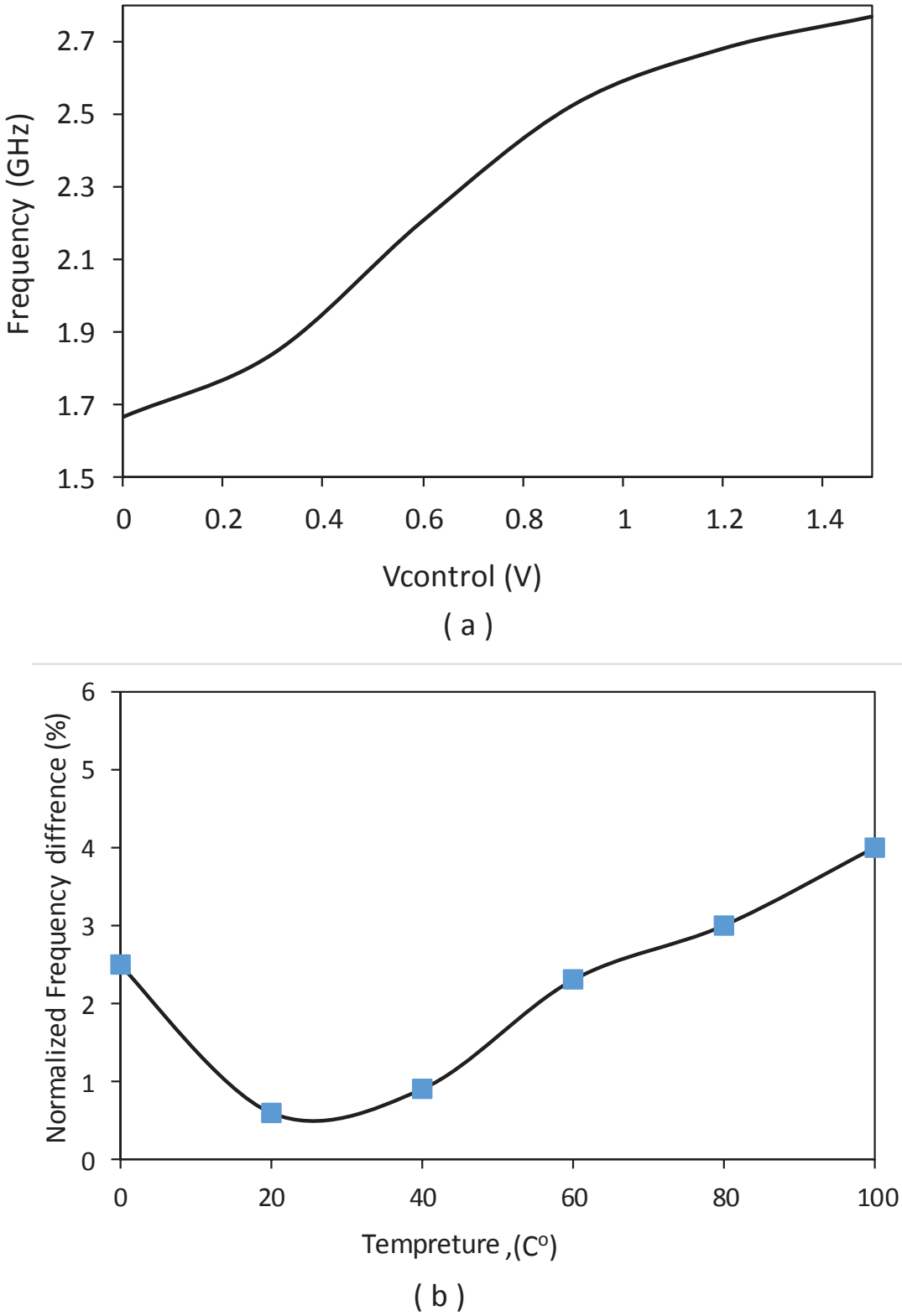
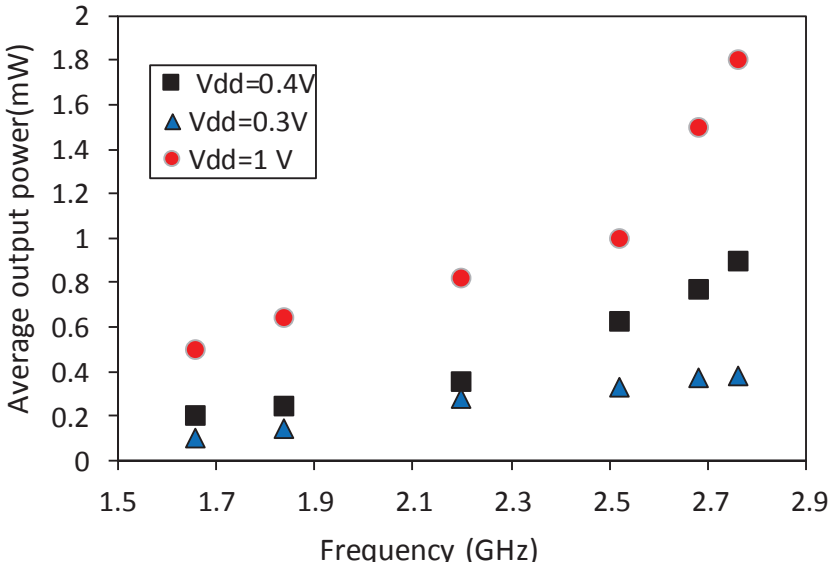
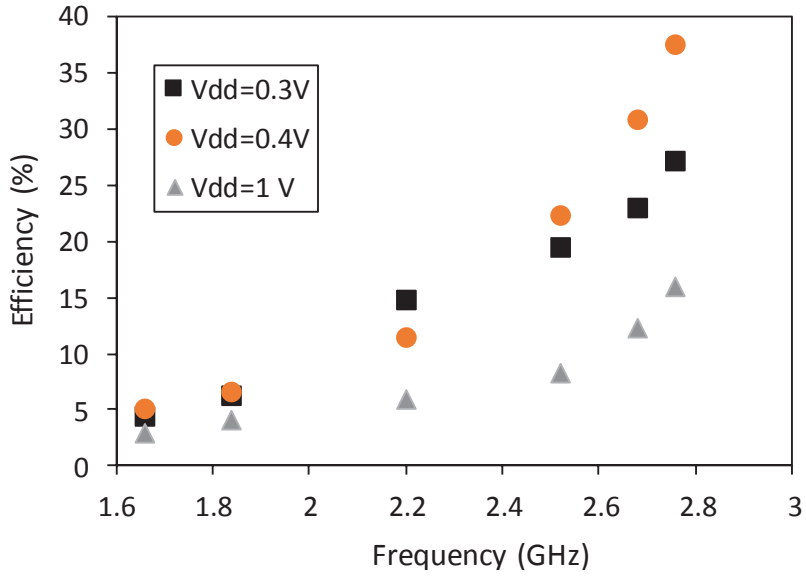


Figure 3.16: The oscillator post layout results (a) oscillation frequency versus control voltage (b) normalized frequency difference versus temperature for nominal frequency 2.4403 GHz at $V_{control}$ equals to 0.8 V.



(a)



(b)

Figure 3.17: The proposed power oscillator performance (a) average output power (b) oscillator efficiency.

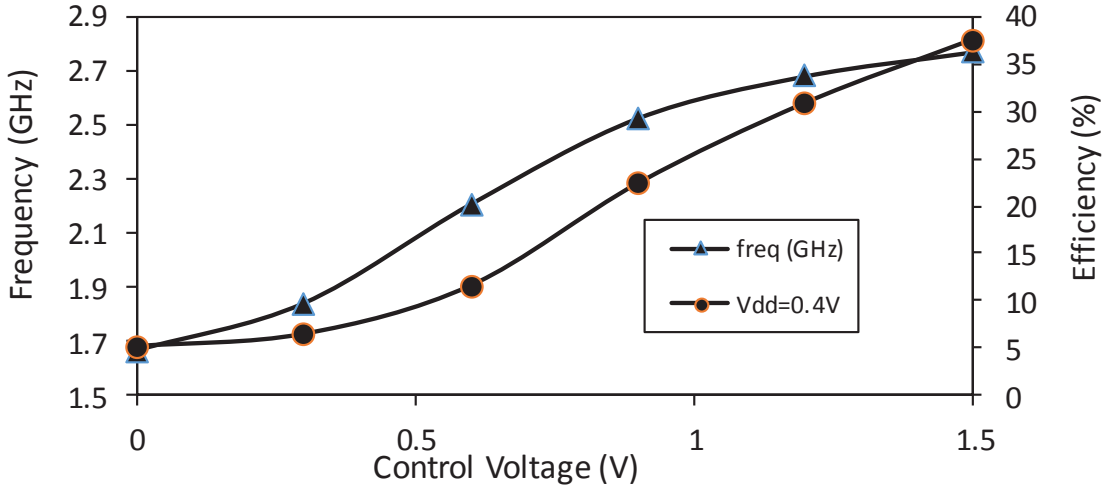


Figure 3.18: The oscillator operating frequency and efficiency as a function of control voltage.

0.4 V. This wide tuning range enables the oscillator to compensate for PVT variation. The oscillator is robust to $\mp 15\%$ frequency deviation from a 2.44 GHz nominal frequency. The PA and the varactor are nonlinear and this reflects on the transmitter spectrum shown in Fig. 3.16(a) where the operating frequency does not increase linearly with the increases of the control voltage that applied to the varactor. The oscillator performance against the temperature variation between 0^oC to 100 ^oC is illustrated in Fig.3.16(b). The results show that less than $\mp 5\%$ frequency deviation occurs over 100 ^oC temperature change.

Fig. 3.17 (a) shows the oscillator output power between 0.1 mW and 2 mW under a supply voltage is between 1.3 V and 1 V and a frequency range of 1.66 to 2.77 GHz respectively. The oscillator efficiency between 5% and 37.5% under a supply voltage is between 1.3 and 1 V as depicted in Fig. 3.17 (b). The results reveal that the efficiency decreases with high Vdd due to the increased power dissipation . A 0.4 V power supply is the optimal due to the achieved 37.5 % efficiency, 0.9 mW output power and 2.4 mW power dissipation as can be seen in Fig. 3.18 .

The VCO achieves a figure of merit (FOM) ranging from -158 to -172 dBc/Hz as described in (3.18) with trade-off parameters that include phase noise ($L(\Delta\ \omega)$),

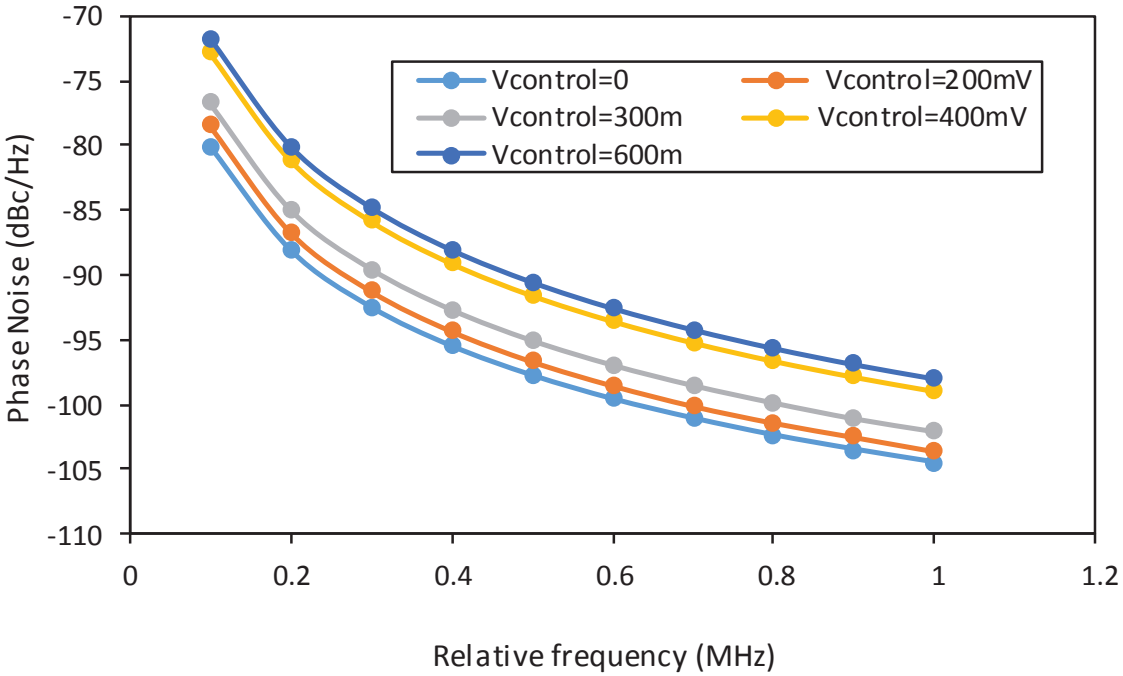


Figure 3.19: The periodic steady state (PSS) analysis as a function of the analog control voltage.

power dissipation (PD), carrier frequency (ω_o) and offset frequency ($\Delta\omega$) . The phase noise of the VCO at 1 MHz offset frequency is ranging between -100 to -110 dBc/Hz as demonstrated in Fig. 3.19.

$$FOM = L(\Delta\ \omega) + 10\log(PD/1mW) - 20\log\omega_o/(\Delta\omega) \tag{3.18}$$

A summary of the results is given in Table 3.2, and the performance comparison with recently reported CMOS VCOs is carried out. The comparison reveals that this work has the lowest power supply and the lowest power consumption while maintaining a high output power, high power efficiency and an excellent frequency tuning range. Moreover, the phase noise and FOM are comparable to other state of the arts.

Table 3.2: Performance comparison with previous state-of-the-art VCO designs.

Specifications	This work	[58]	[46]	[59]	[56]
Process	CMOS 65 nm	CMOS 0.18μm	CMOS 65 nm	CMOS 0.18 μm	GaAs 0.6 μm
Frequency(GHz)	2.4	2.1-2.7	1.95	2.2-2.4	4.4
Tuning range (GHz)	1.1	0.6	0.4	0.2	0.15
Power supply(V)	0.4	0.9	2.5	0.7	0.9
Power dissipation (mW)	2.4	2.7	337	5.18	33.3
Output power (dBm)	-0.45	-5.2	22	-10	1.1
Efficiency, η(%)	37.5	11	N/A	1.96	36
Phase noise (dBc/Hz)	-108	-122	N/A	-125	110
FOM (dBc/Hz)	-172	-186	N/A	-185	-165

3.7 Summary

An overview of the PA classes were presented and a class-E PA design was discussed in detail. The requirements and the trade-off between design parameters were reviewed. A system-level design methodology for a class-E power oscillator was demonstrated.

Finally, a complete circuit design of a low voltage class-E oscillator in CMOS 65nm was presented. The design utilized a class-E PA as the core of the design with a positive feedback. The oscillator achieved a peak output power of -0.5 dBm and a peak efficiency of 37.5% under a 0.4 V power supply and frequency tuning range between 1.66 and 2.7 GHz.

Chapter 4

Design of a 69 Mbps Energy-Efficient Transmitter Based on a Class-E Power Oscillator

In this chapter, an energy efficient QPSK transmitter suitable for high-quality imaging for biomedical applications is presented. In addition, a novel technique to achieve a full phase shift of 360° for phase modulation is proposed and detailed analysis is discussed along with the derivation of the mathematical equations. The transmitter is targeting the 2.4 GHz ISM band. In order to reduce the power consumption and optimize the energy/bit figure of merit, a highly efficient transmitter architecture is proposed, utilizing a class-E PA not only as an amplifier but as a carrier generator and as a modulator.

This chapter is organized as follows: Section 4.1 presents a new PM technique suitable for low-power direct modulation. Section 4.3 describes the circuit design of the QPSK transmitter and the phase modulation digital circuit design. Section 4.4 discusses the quality of the oscillation and the BER requirements. The layout recommendations are discussed in Section 4.5. Test plan and fabrication are described in Section 4.6. In addition, an analysis of the principle of operation is demonstrated. Section 4.7 presents the measurement results and compares them with the existing state-of-the-art WSN transmitters. Finally, a summary and discussion are given in Section 4.8.

4.1 A New Phase Modulation Technique

In a conventional QPSK system, the phase of the carrier is modulated by multiplying the base band signal by the carrier using a quadrature mixer. As explained in Section 2.1, the carrier phase is adjusted in increments of 90° by selecting one of four phase-shifts- $0°, 90°, 180° or 270°$- of the carrier signal to represent the two-bits digital information per symbol. The transmitter output voltage is simply expressed as a

sinusoidal signal with an instantaneous phase shift (ϕ_i) such that:

$$V_{out} = V_m \cos(\omega_0 t + \phi_i) \tag{4.1}$$

Here, V_m is the peak amplitude at the output of the transmitter.

The ability to generate the 360° phase shift is critical in direct modulation transmitters. The up-conversion architecture, although it generates the required phase shift, it is not suitable for limited power budget application due to the high power consumption (as explained in Chapter 2). The IL QPSK/PSK transmitters suffer from limited phase tuning range and usually they need additional circuits to generate the rest of the 360°. Recall (2.9) the maximum phase shift that can be achieved in IL is 90° which occurs at weak injection [28]. In [33], an IL LC-oscillator was used in a QPSK transmitter with a limited phase shift only 90°. An additional circuit (polarity sweep) was added to generate the rest of the required phase shift. The limited phase tuning range results from using IL for phase modulation. In another example [36], sub-harmonic IL pulses were employed to generate phase shift of only 45°. The 90°, 180° and 270° phase shifts were generated from the next three delay cells. As can be seen, there is a need for an alternative solution that replaces these techniques.

The presented new PM is an alternative technique that relies on the instantaneous change in the carrier frequency to rotate the phase 360°. To understand the concept behind this technique, recall the angular frequency (ω) of a periodic system can be represented as the derivative of the phase with respect to time, i.e. $\omega = d\phi/dt$. Thus, we can represent the instantaneous phase at a time t as

$$\phi(t) = \int_0^t \omega(t)dt + \phi_0. \tag{4.2}$$

where ϕ_0 is the initial phase at time 0. By assuming the carrier phase ϕ_0 is known either through synchronization, or by defining a known reference symbol at the beginning of a frame. By assuming a constant instantaneous frequency ω_i, the phase at the end of a transition period T_m is equal to:

$$\phi_i = \omega_i T_m + \phi_0 \tag{4.3}$$

For simplicity, we assume ϕ_0 equals to zero. For the i-th symbol, the equivalent

phase is ϕ_i is given by:

$$\phi_i(rads) = \omega_i T_m = \pm k\frac{\pi}{2} \tag{4.4}$$

Where $\omega_i = 2\pi f_i$ is the instantaneous frequency. The PM can be derived as follows:

$$\phi_i = 2\pi f_i T_m \tag{4.5}$$

As presented in (4.5), there are two degrees of freedom to modulate the phase: the first is by using the instantaneous frequency f_i, the second is by using the transition period T_m. This technique provides flexibility in achieving the phase rotation in terms of the frequency change and the transition time. In the following sections, we will discuss the PM using these two degrees of freedom.

4.1.1 Phase rotation using instantaneous frequency

For a transition period equals to the period of the carrier frequency $T_m = 1/f_c$, the instantaneous phase ϕ_i can be found as:

$$\phi_i = \frac{2\pi f_i}{f_c} \tag{4.6}$$

By rotating the phase in 90^o increment: $(\pm k\pi)/2$, where $k = 1, 5, 9, \cdots$, thee required f_i can be found as:

$$f_i = \frac{1}{4}f_c, \frac{5}{4}f_c, \frac{9}{4}f_c, \cdots \tag{4.7}$$

To achieve a 180^o or $\pm k\pi$ phase shift, the required f_i is:

$$f_i = \frac{1}{2}f_c, \frac{5}{2}f_c, \frac{9}{2}f_c, \cdots \tag{4.8}$$

To achieve a 270^o or $\pm(3k\pi)/2$ phase rotation, the required f_i is:

$$f_i = \frac{3}{4}f_c, \frac{15}{4}f_c, \frac{27}{4}f_c, \cdots \tag{4.9}$$

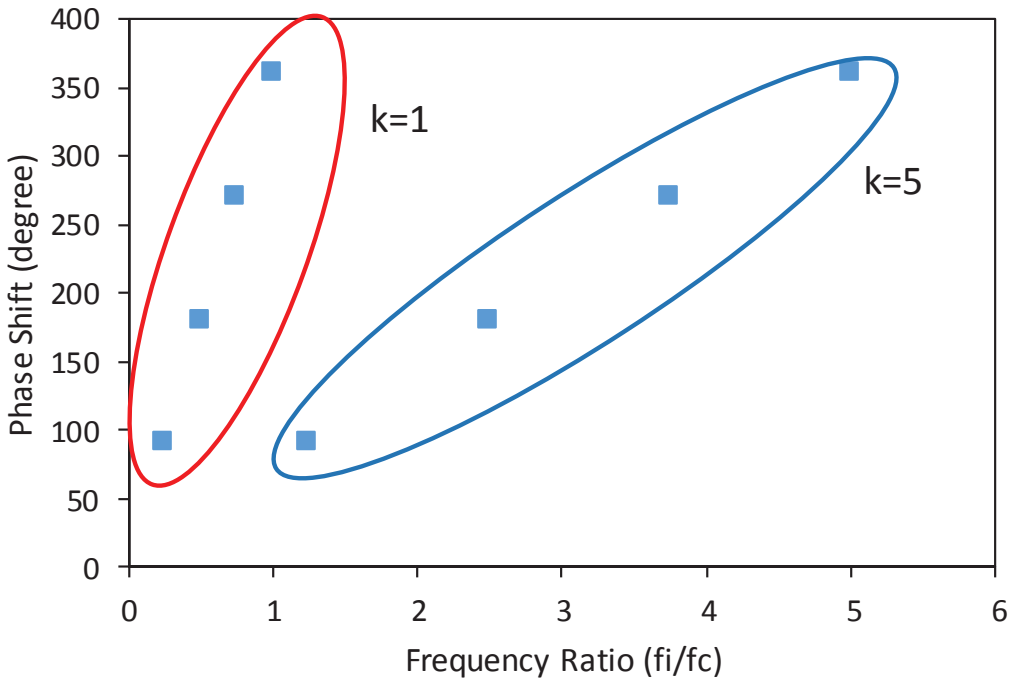


Figure 4.1: The phase rotation as a function of the instantaneous change of frequency ratio (f_i/f_c).

This is demonstrated in Fig. 4.1 which shows the relationship between the instantaneous ratio(f_i/f_c) and the achieved phase shift with respect to k. For a 2.4 GHz nominal frequency, the required instantaneous frequencies to achieve the 360° phase shift as a function of a varactor control voltage is illustrated in Fig. 4.2. As can be seen, the phase shift increases linearly with the control voltage. Note, the ratio f_i/f_c is increasing linearly over a 360° phase range.

4.1.2 Phase rotation using transition period

The transition period T_m is chosen here to rotate the phase. When the transition period equals to one period of the carrier frequency $T_{m1} = 1/f_c$, the required instantaneous frequency to rotate 90° can be found as:

$$f_i = \frac{1}{4}f_c, \frac{5}{4}f_c, \frac{9}{4}f_c, \cdots \tag{4.10}$$

When T_m equals to twice the period of the original clock $T_m = 2T_{m1} = 2/f_c$. The required f_i to achieve a 180° phase shift is found as:

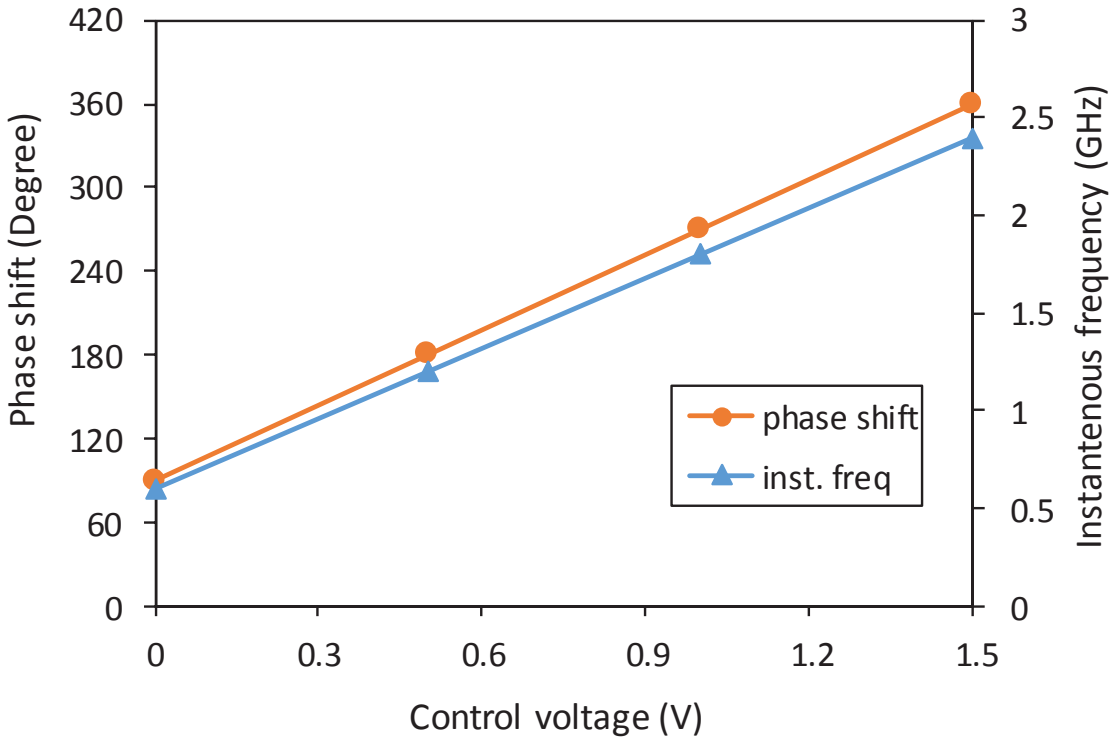


Figure 4.2: The characterization of the frequency and phase shift as a function of a varactor control pulse.

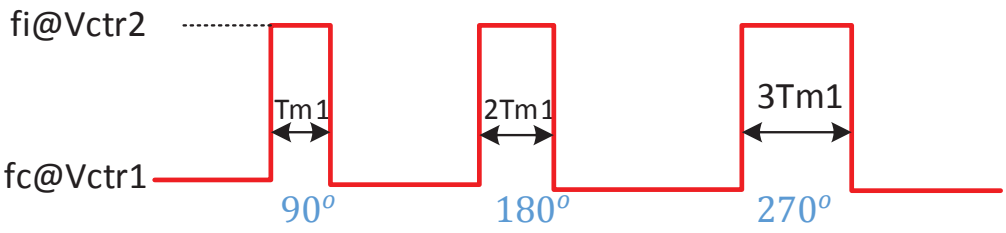


Figure 4.3: The waveform of PM using transition period tuning.

$$f_i = \frac{1}{4}f_c, \frac{5}{4}f_c, \frac{9}{4}f_c, \cdots \tag{4.11}$$

When T_m equals to triple the period of the original clock $T_m = 3T_{m1} = 3/f_c$. The required f_i for 270° phase shift is found as:

$$f_i = \frac{1}{4}f_c, \frac{5}{4}f_c, \frac{9}{4}f_c, \cdots \tag{4.12}$$

Note (4.10), (4.11) and (4.12) require the same f_i for (90°,180° and 270°) phase shift. This is a very interesting characteristic where increasing the PM pulse width will increase the phase shift without increasing f_i. Fig. 4.3 illustrates the time domain representation of the required pulse width. Indeed, this technique maintains small f_i during phase rotation and this is important advantageous at circuit level implementation. Fig. 4.4 demonstrates the phase modulation using the proposed technique and the required instantaneous frequency change f_i/f_c.

In practice, the selection of f_i and T_m are defined by the circuit parameters of the carrier generator. However, a large frequency shift requires a large capacitor bank to be integrated and more die area. We will discuss all the requirement and the consideration to implement the circuit design for PM technique in the following section.

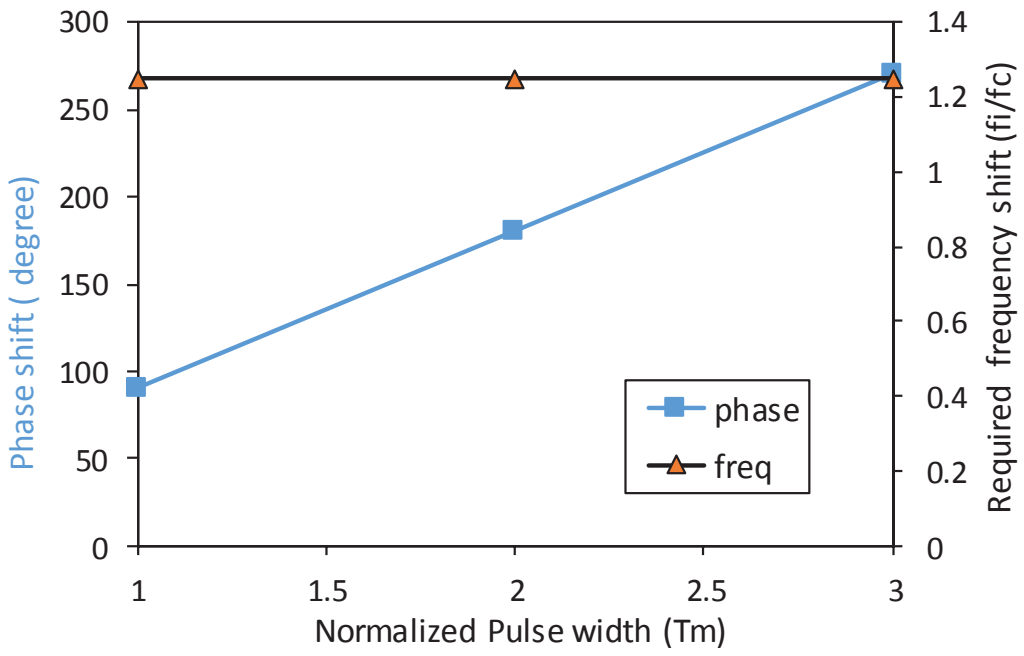


Figure 4.4: The relationship between the phase shift and the frequency ratio(fi/fc) using transition period tuning.

4.2 System Level Consideration for The Transmitter Design

The new PM technique (using T_m control) is applied to the class-E power oscillator for direct modulation. Since the operating frequency is a 2.4 GHz ISM band and from (4.7), we select the f_i/f_c ratio to be 5/4, hence, the required instantaneous frequency f_i is 3 GHz. To adjust the operating frequency of a resonant LC circuit, the resonant capacitor should fluctuate between two values (C_i, C_c) to meet the associated frequencies f_i and f_c that can be found as:

$$f_i = \frac{1}{2\pi\sqrt{L_{res}\ C_i}} \tag{4.13}$$

$$f_c = \frac{1}{2\pi\sqrt{L_{res}\ C_c}} \tag{4.14}$$

Where L_{res} is the resonant inductor, C_c is the value of the capacitance at nominal resonant frequency f_c and C_i is the instantaneous value at the instantaneous frequency f_i. Circuit topology and design requirement determine which degree of freedom (f_i *or* T_m) to be used for PM control. The transition period is selected carefully to keep the capacitor ratio (C_c/C_i) within reasonable range.

To achieve a 90^o phase shift, the required C_c/C_i is:

$$\frac{C_c}{C_i} = \frac{1}{16}, \frac{25}{16}, \frac{81}{16} \tag{4.15}$$

We select the C_c/C_i ratio equal to 25/16 or 1.56 to allow the frequency to vary between 2.4 GHz and 3 GHz. To account for any non-ideal effects and PVT variation, the oscillator tuning range is extended to 1.95 GHz and 3.3 GHz.

Figure 4.5 depicts the required capacitance change ratio C_c/C_i to generate the 360^o phase rotation. It clearly indicates that a very small capacitor change is needed to achieve the required phase shift.

4.3 QPSK Transmitter Design

A prototype of the energy efficient QPSK transmitter is designed, implemented and tested in this research. This transmitter employs direct modulation architecture for low energy consumption.

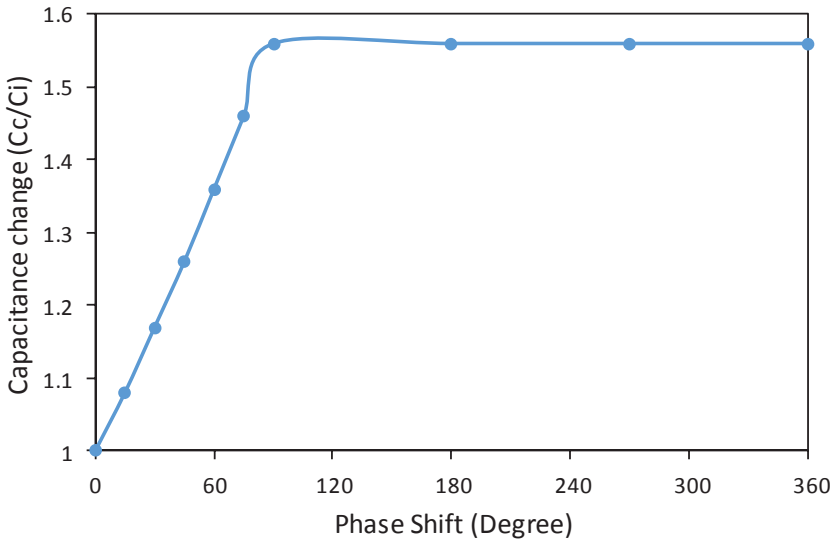


Figure 4.5: The required capacitance ratio for 360° phase shift using the proposed technique (transition period control).

The transmitter block diagram is depicted in Fig. 4.6. The transmitter is synchronized (locked) to the external clock (V_{synch}) of a 2.2 GHz for a very short period of time, in which this refrence is used to generate an accurate symbol clock of 34.4 MHz to meet the 69 Mbps data rate. The synchronization process is enabled/disabled by an external clock ($V_{c,inj}$).

The transmitter circuit consists of a class-E power oscillator and a digital control circuit for PM and synchronization. The class-E power oscillator generates the RF carrier of a 2.4 GHz ISM band. A self oscillating class-E PA is employed to design a class-E power oscillator. The directly modulated power oscillator rotates the phase of the carrier frequency to represent two bits of binary data. The transmitter radiated power is around -6.8 dBm. The digital control circuit manages the PM pulse generation for QPSK modulation and provides data serial interface.

Figure 4.7 represents the simulation results for a QPSK system with a symbol rate equal to T_s and a carrier frequency equal to f_c. Note, to evaluate the transmit symbol sequence, one must sample the carrier phase after the instantaneous change of frequency (indicated by red markers).

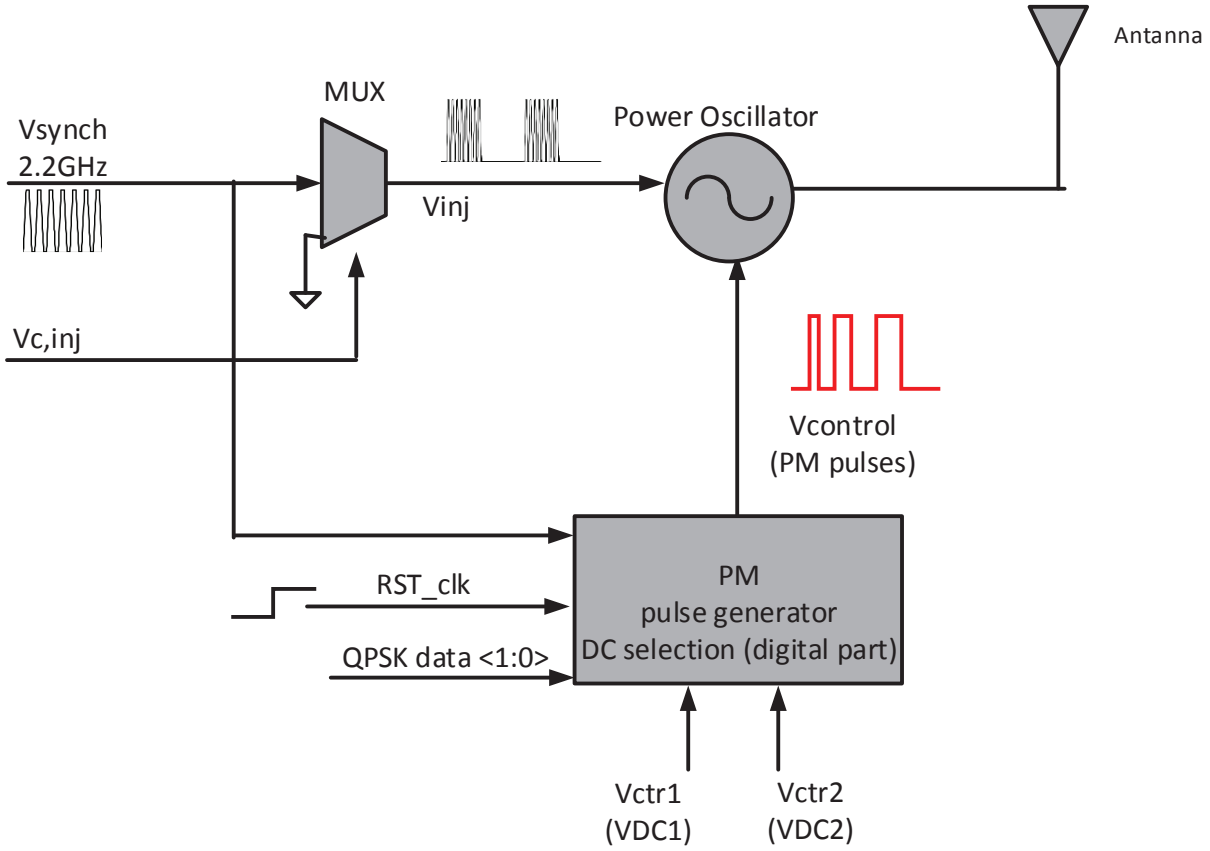


Figure 4.6: The block diagram of the transmitter architecture.

Figure 4.8 shows the relationship between the input two-bits code and the pulse width associated with phase shift for a 2.4 GHz oscillation frequency and a clock period equal to 416 ps. When input data is 01 the PM pule width is 416 ps, for 10 the pulse width is 832 ps and for 11 the pulse width is 1248 ps.

In the following sections, each block of the transmitter design is discussed in detail along with simulation and measurement results.

4.3.1 The Power Oscillator Design

A high frequency tuning range (2.4 GHz to 3 GHz) is required to implement the proposed technique for PM; however, the frequency tuning range is directly related to the gain as explained in Chapter 3. The extended tunability comes at the price of limited gain. To overcome this problem, a class-D driver is used as a pre-amplifier to sustain the oscillation. The block diagram of the proposed oscillator design is

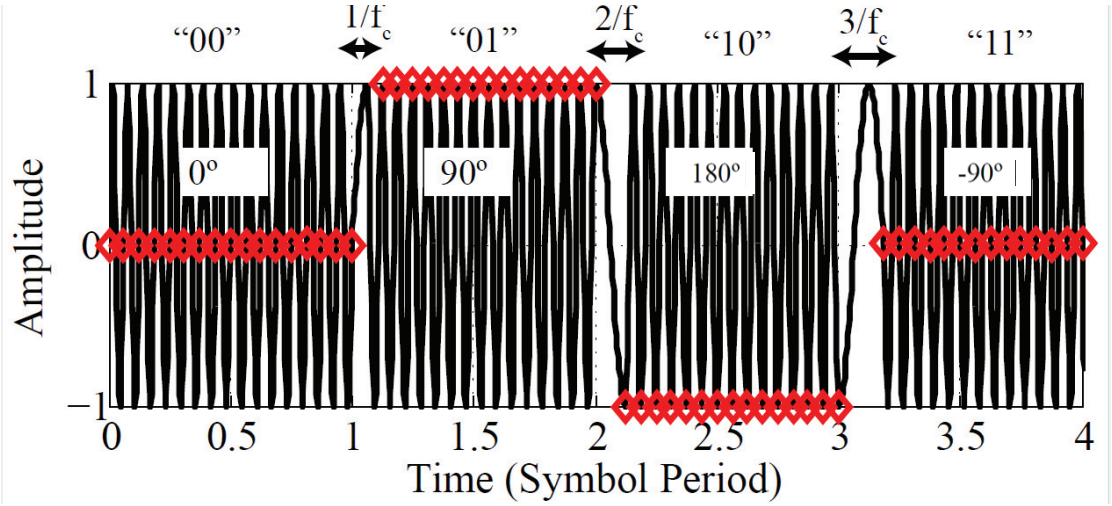


Figure 4.7: System simulation of the transmit waveform for a set of digital symbols.

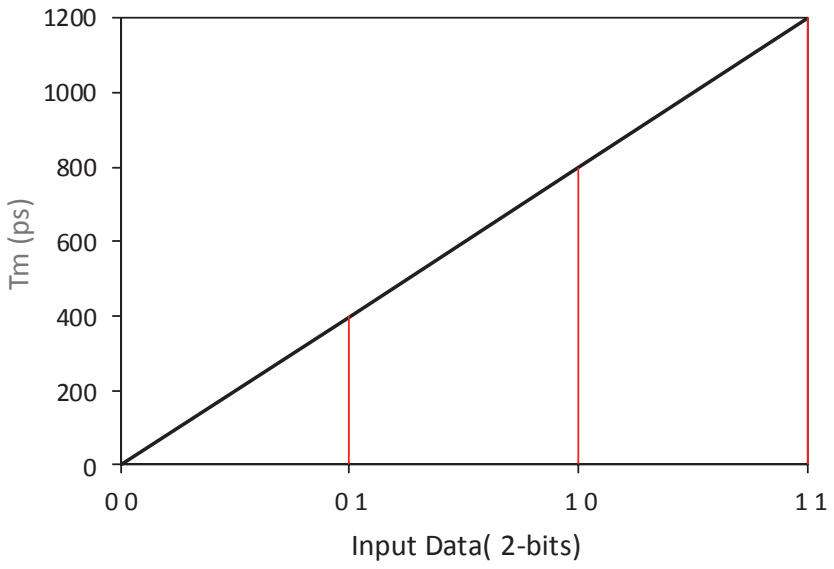


Figure 4.8: The required transition time (T_m) for PM of two-bits input code and the clock period equals to 416 ps.

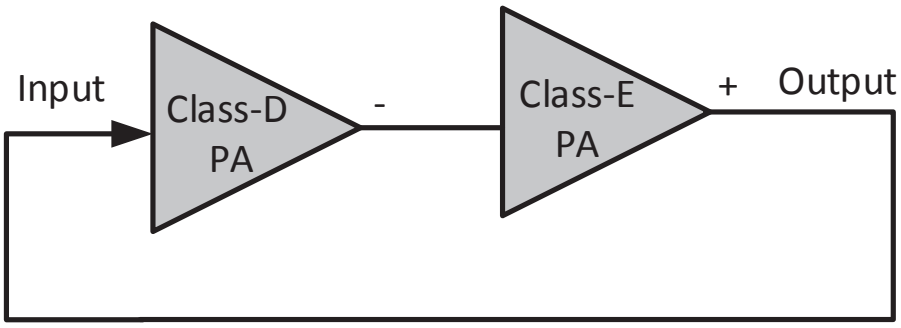


Figure 4.9: The feedback model of class-E power oscillator.

depicted in Fig. 4.9. Network A includes two stages: the class-E PA and a class-D as a pre-amplifier stage which is responsible for providing the required $(2\pi n)$ phase shift to sustain the oscillation. The network β is unity.

Fig. 4.10 shows the closed-loop system of the power oscillator. The class-E PA is modeled as a transconductance $(-G_{m2})$ amplifier and a series RLC circuit with an equivalent impedance $(Z(s))$. The class-D driver is modeled as a $(-G_{m1})$ and the loop gain can be found as:

$$G_{loop}(s) = G_{m1}G_{m2}\frac{R}{L_{res}}\ \frac{s}{s^2 + (R/L_{res})s + 1/(LC)_{res}} \tag{4.16}$$

The closed-loop transfer function is:

$$\frac{vout(s)}{vin(s)} = \frac{G_{m1}G_{m2}\frac{R}{L_{res}}\ \frac{s}{s^2+(R/L_{res})s+1/(LC)_{res}}}{1 - G_{m1}G_{m2}\frac{R}{L_{res}}\ \frac{s}{s^2+(R/L_{res})s+1/(LC)_{res}}} \tag{4.17}$$

$$\frac{vout(s)}{vin(s)} = \frac{G_{m1}G_{m2}\frac{R}{L_{res}}s}{s^2 + (\frac{R}{L_{res}})s[1 - G_{m1}G_{m2}] + \frac{1}{(LC)_{res}}} \tag{4.18}$$

The closed-loop complex-conjugate poles are:

$$S_{1,2} = \frac{-(\frac{R}{L_{res}})(1 - G_{m1}G_{m2}) \pm \sqrt[2]{(\frac{R}{L_{res}}(1 - G_{m1}G_{m2}))^2 - \frac{4}{(LC)_{res}}}}{2} \tag{4.19}$$

The root locus plot is used to show the trajectory of the closed-loop poles in the

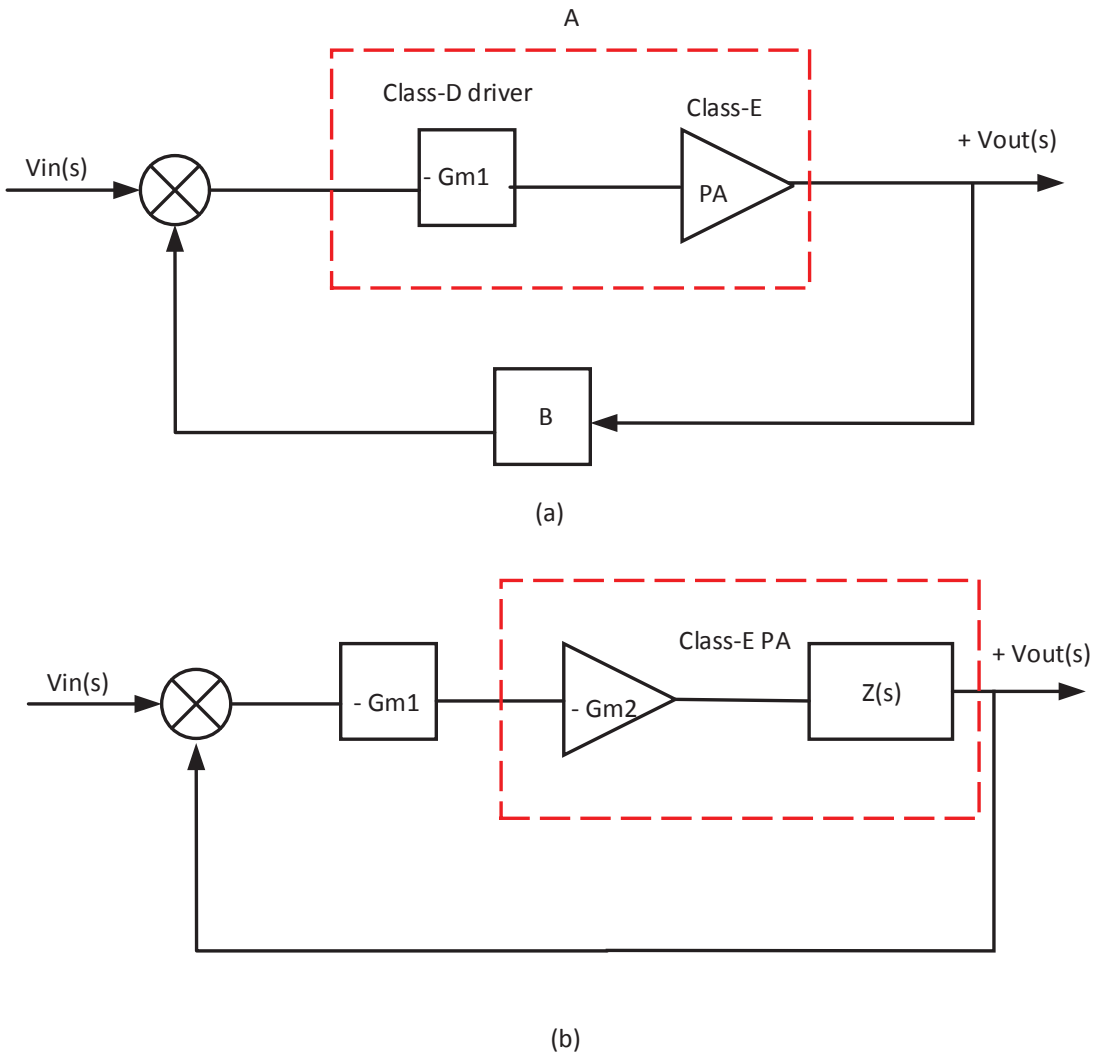


Figure 4.10: The feedback model of a class-E power oscillator (a) the block diagram (b) the detailed closed-loop system.

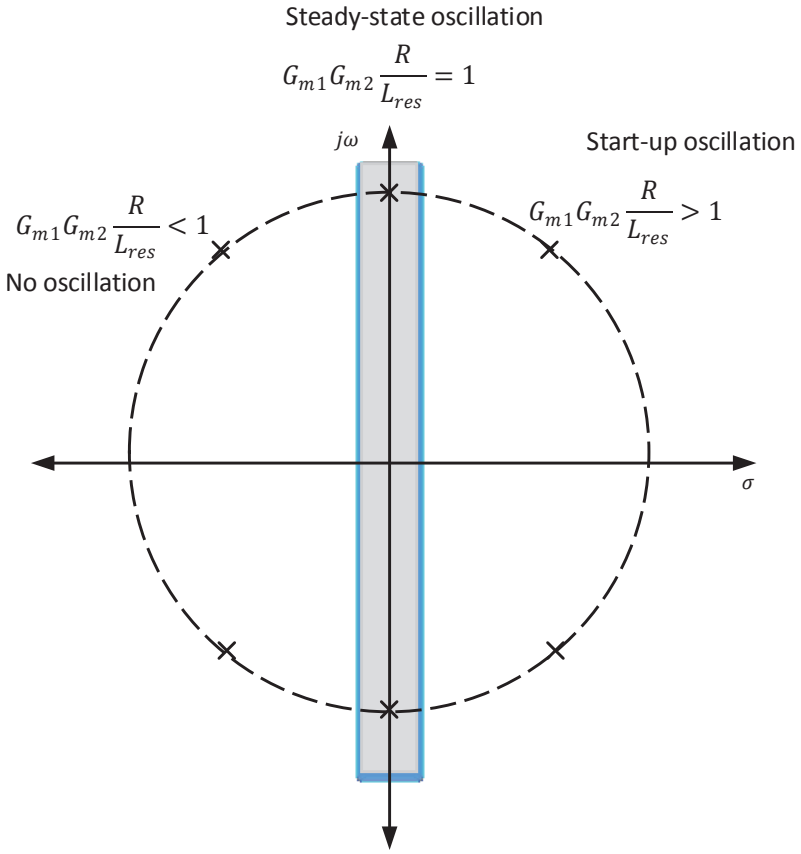


Figure 4.11: The root locus analysis of a class-E power oscillator for closed-loop poles location.

complex s-plane. When $G_{m1}G_{m2}\frac{R}{L_{res}} > 1$, the poles have a positive real part and are located on the right half of the s-plane. When $G_{m1}G_{m2}\frac{R}{L_{res}} = 1$, the poles only have an imaginary part and are located directly on the imaginary axis. When $G_{m1}G_{m2}\frac{R}{L_{res}} < 1$, the poles have a negative real part and are located on the left half of the s-plane. Fig. 4.11 illustrates the root locus analysis of the power oscillator. $G_{m1}G_{m2}\frac{R}{L_{res}}$ has to be greater than 1 to start oscillation where the oscillation amplitude starts to grow exponentially. Due to the MOSFET nonlinearities, the poles will go back to the imaginary axis and the oscillation reaches the steady-state.

The schematic of the oscillator is displayed in Fig. 4.12. It is comprised of a self oscillating class-E PA and a class-D driver utilizing a positive feedback. The class-E

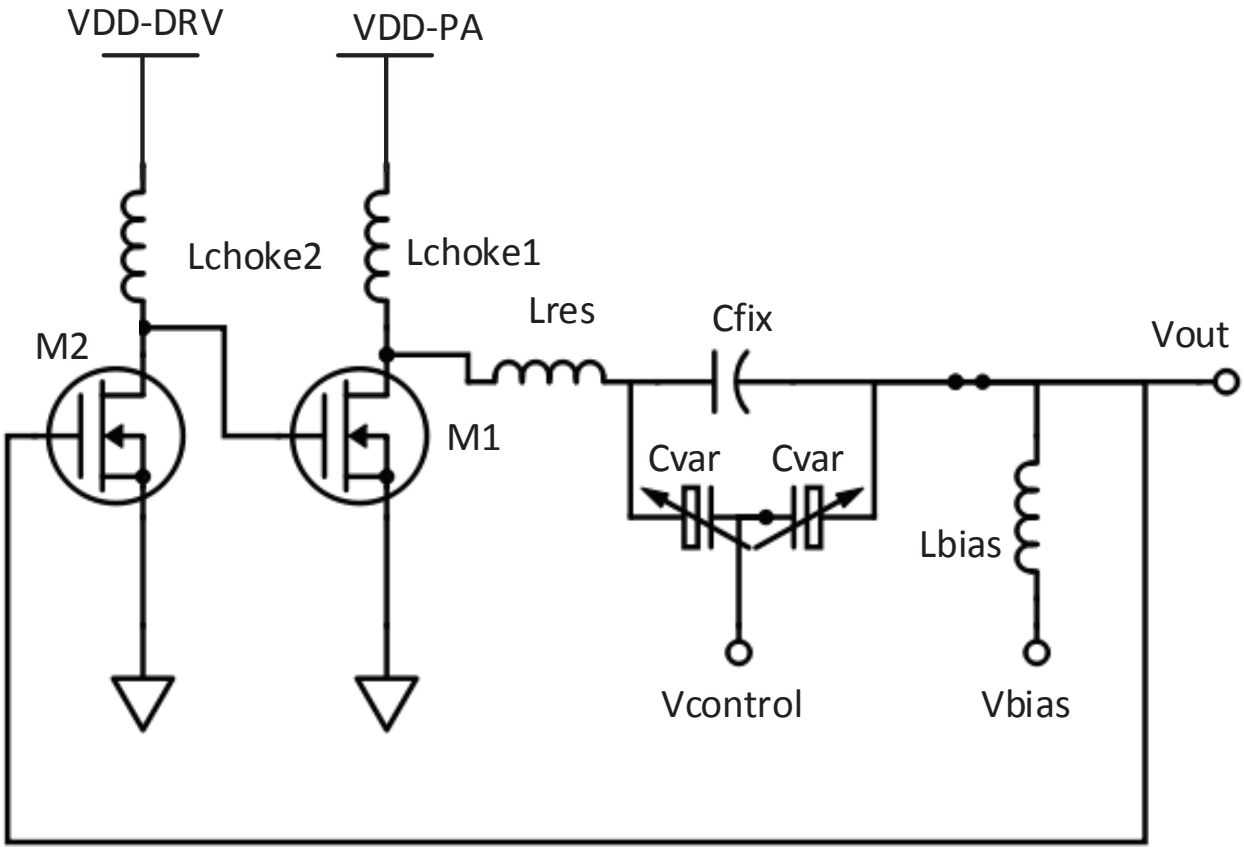


Figure 4.12: The schematic diagram of a class-E power oscillator.

Table 4.1: The dimension of Power Oscillator Circuit.

Device	size
$L_{chocke1}$	4 nH
$L_{chocke2}$	4 nH
L_{res}	0.88 nH
C_{fix}	0.1 pF
C_{var}	1-1.8pF
L_{bias}	100 nH
V_{bias}	0.6 V
R_{load}	50 Ω
Vdd-PA	0.4 V
Vdd-DRV	0.6 V

PA includes a choke inductor L_{choke1} and a common source MOS device (M_1). The class-D driver includes a choke inductor L_{choke2} and a common source MOS device (M_2). In order to provide a DC bias V_{bias} for M_2 , a large off chip inductor L_{bias} is used to provide a DC path to ground. L_{bias} was selected carefully to be large enough so no current flows in but not very large to prevent oscillation. L_{bias} =100nH, V_{bias}=0.4 V.

A series resonant circuit ($L_{res}C_{fix}$) tank along with parallel dual varactors C_{var} were used for direct modulation. Table 4.1 summarizes the dimensions and the values of the class-E power oscillator circuit.

The selection of M_1 is limited by the trade-off between the small r_{on} (recall (3.6)) and the small drain capacitance C_{drain} (recall (3.5)). Although increasing M_1 size reduces the resistive losses of the switch, it limits the maximum operating frequency of the PA due to the growing size of the drain parasitic capacitor with the width of MOS device. The optimum width in our design is 60 μm and the power supply is 0.4 V to limit the drain swing.

A class-D driver is utilized to provide the required input power. The selection of transistor M_2 size depends on the required V_{gs} and the PA drain current. From the

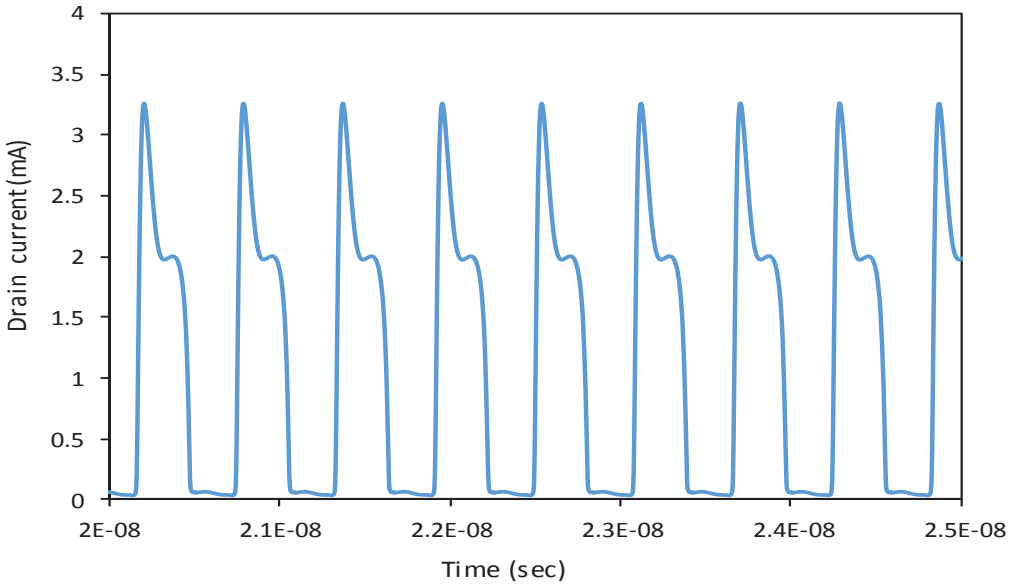


Figure 4.13: The simulation results of the drain current of the power oscillator.

power consumptions constraints, we select the drain current and the V_{gs} voltage to be around 3 mA and 0.5 V respectively. Fig. 4.13 shows the characteristics of the PA drain current and the switching behavior. The size of M_2 is 60 μm operating under 0.6 V power supply.

Metal-Insulator-Metal (MIM) capacitor is used to implement C_{fix}. MOS varactor C_{var} varies between 1 pF to 1.5 pF. The total effective resonant capacitance varies between a nominal value C_c at nominal resonant frequency f_c and an instantaneous capacitance value C_i at an instantaneous frequency f_i as:

$$C_c = C_{fix} + \frac{C_{varmax}}{2} \tag{4.20}$$

$$C_i = C_{fix} + \frac{C_{varmin}}{2} \tag{4.21}$$

(4.20) and (4.21) are used to determine the LC tank values. With $C_i/C_c = 1.7$, L_{res} equals to 0.88 nH and C_c equals to 1 pF by including the bonding pad capacitance equals to 0.5 pF and the parasitic inductance equals to 2 nH.

Table 4.2: Power consumption breakdown.

Circuit block	power consumption (mW)
Class-E power amplifier	0.8 , Vdd=0.4V
pre-amplifier	2.1 , Vdd=0.6V
Total	2.9

The optimum load was found to be 66 Ω for targeting peak output voltage of 0.3V and output power of 0.3 mW. Since the structure of the PA is single ended, and to avoid the losses associated with the matching network, the output load is selected to be 50 Ω.

Table 4.2 summarizes the breakdown of the power consumption and the total power consumption with a 2.9 mW. The transmitter achieves an energy efficiency of 42 pJ/bit at a data rate of 69 Mb/s. The oscillator phase noise at 1 MHz offset frequency from the carrier frequency is -125 dBc/Hz as shown in Fig. 4.14. The phase noise during locking is demonstrated in Fig. 4.15 and as can be seen, the noise performance improved with −155 dBc/Hz.

4.3.2 Synchronous Transmission

Fig. 4.16 presents the circuit architecture of a synchronized class-E power oscillator. To apply the new phase modulation technique at the RF front end, a synchronization with a refrence tune is important. An external clock (Synch-Clk) is used to maintain the synchronization between the carrier and symbol clocks (this will be explained in Section 4.3.3). The external reference tone is used to ensure a very accurate symbol clock. Periodically, the external clock is injected to the oscillator to maintain frequency lock. To facilitate this synchronization, an additional MOS device, M_3, was added to the power oscillator circuit with a small size 10 μm and a digital multiplexer to control the gate of the injecting device using (V_{inj}).

IL is applied to lock the transmitter to a 2.2 GHz. This allows re-synchronization, after the frequency shift (during PM) and enables coherent transmission of each symbol which provides an additional performance improvement in the communication

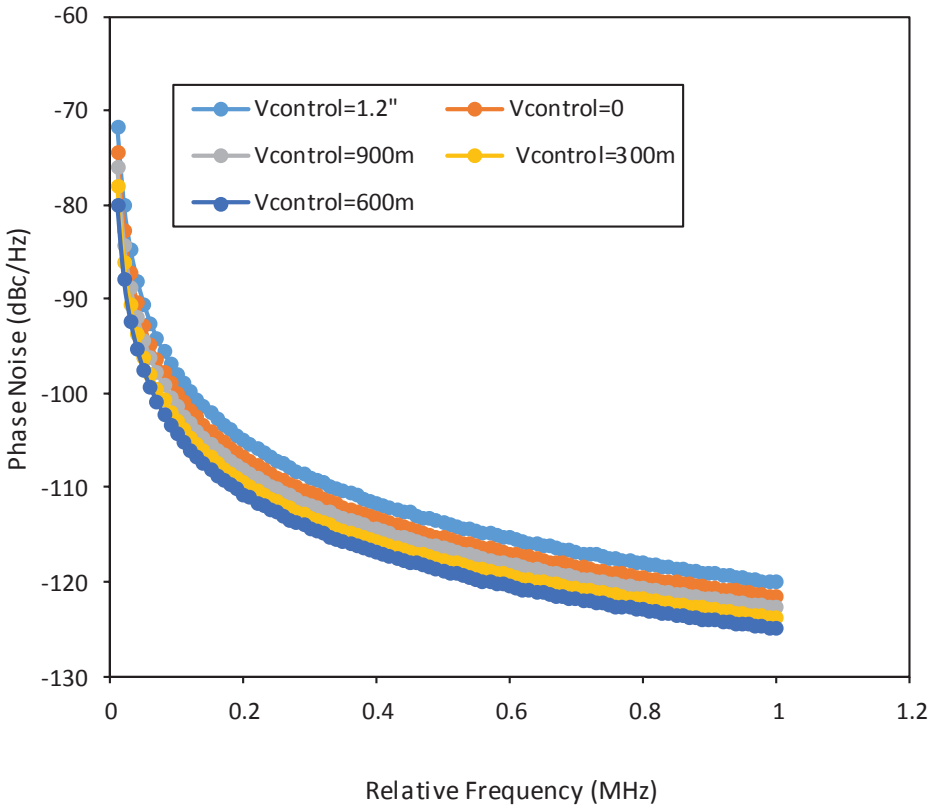


Figure 4.14: The phase noise performance of the transmitter with respect to the control voltage.

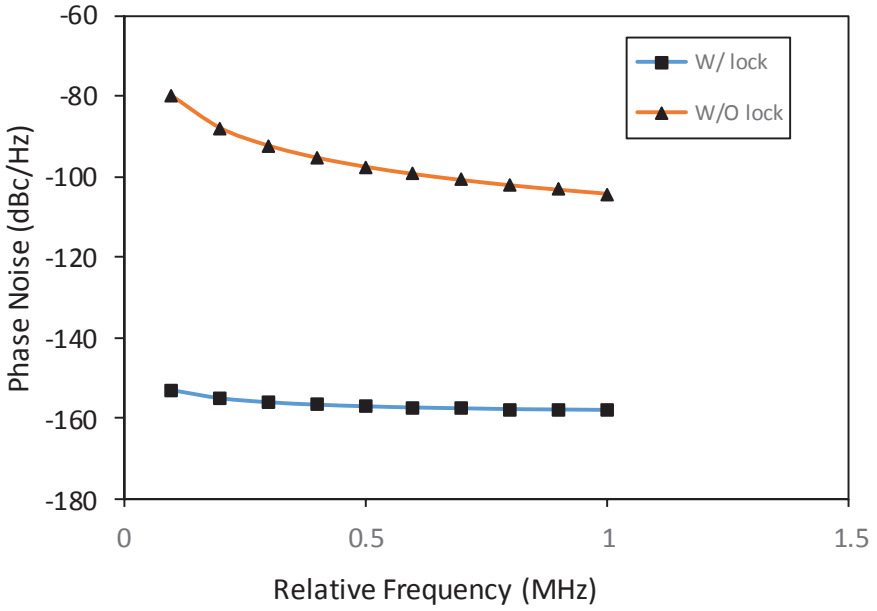


Figure 4.15: The phase noise performance of the transmitter during locking and free running.

link. The injected tone is enabled using a digital control signal ($V_{c,inj}$). V_{inj} periodically locks the system for a very short period of time. Synch-Clk is turned off during the PM as illustrated in Fig. 4.17.

The injection signal is enabled only for a short period of time before the next symbol is transmitted. The transmitter has two modes of operation: the free running and the locking which are demonstrated in Fig. 4.18. This operation ensures frequency and phase lock. During the PM, the transmitter is free running (no locking) and V_{inj} signal is disabled. During the lock and at the beginning of each symbol transmission, the oscillator output phase is reset to an initial phase ϕ_0. In the literature, IL was used in implementing PM in [33],[10],[9], where the phase relationship between the input injected signal, output signal and the locking range are defined in [28] (see (2.9)), while in this work, IL is employed to maintain synchronization. A very small locking range ($\omega_0 - \omega_{inj}$) equal to 1.18 Grad/s and a fast locking time (T_{Lock}) equal to 0.8 ns is achieved. In our design, an initial phase ϕ_0 (which results from IL) is introduced. This phase offset is equal to $\mp 12.4^o$ which has no effect on the required $\mp 90^o$ phase shift. This phase offset is eliminated at the receiver end through the carrier-data recovery loop and does not impact the performance of the QPSK transmitter.

4.3.3 The digital Circuit Design for PM Pulses

Using our new PM technique that was explained in the previous sections, the circuit design for the PM clocks and pulses is presented. Fig. 4.19 depicts the digital part of a QPSK transmitter which includes: a pulse generator circuit using a refrence signal, a serial to parallel interface of the input data and a DC level selector. The digital circuitry is implemented using TSMC 65 nm standard cells, A Spectre simulation of the digital circuit transient behavior is run. In the following subsections, each block is discussed in details. A power supply of 0.7 V is used to reduce the leakage power. Recall, the static power in CMOS inverter circuit can be found as:

$$P_s = \sum I_{leakage} \text{ X } V_{dd} \tag{4.22}$$

where $I_{leakage}$ is the total leakage current in CMOS devices and it ranges between 10μ A and 40μA. The estimated static power consumption for 15 inverter stages with a leakage current of 10μ A is equal to 150 μ W.

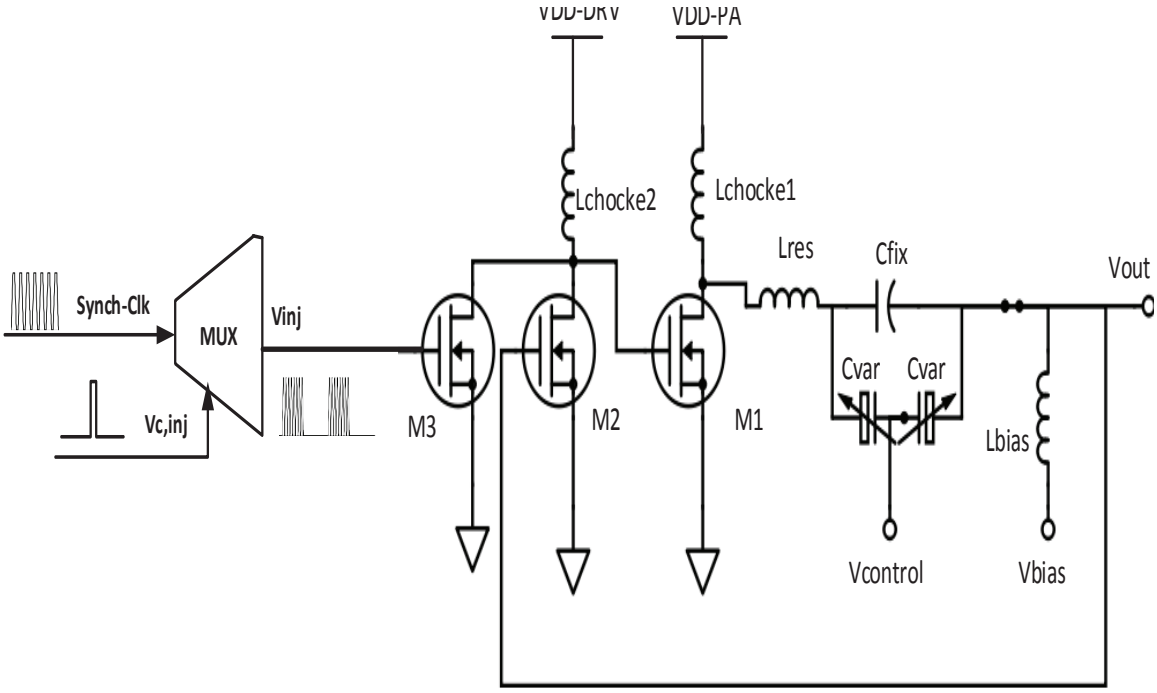


Figure 4.16: The complete circuit design of the synchronized power oscillator.

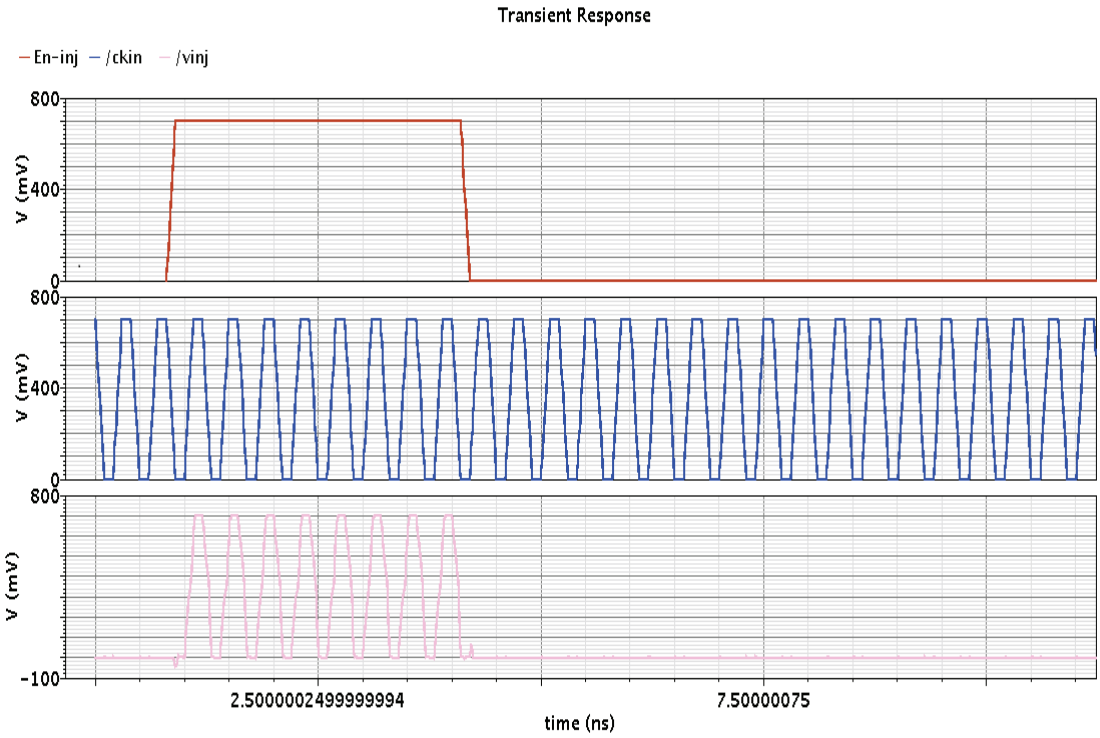


Figure 4.17: The simulation results of the IL enable/disable clocks.

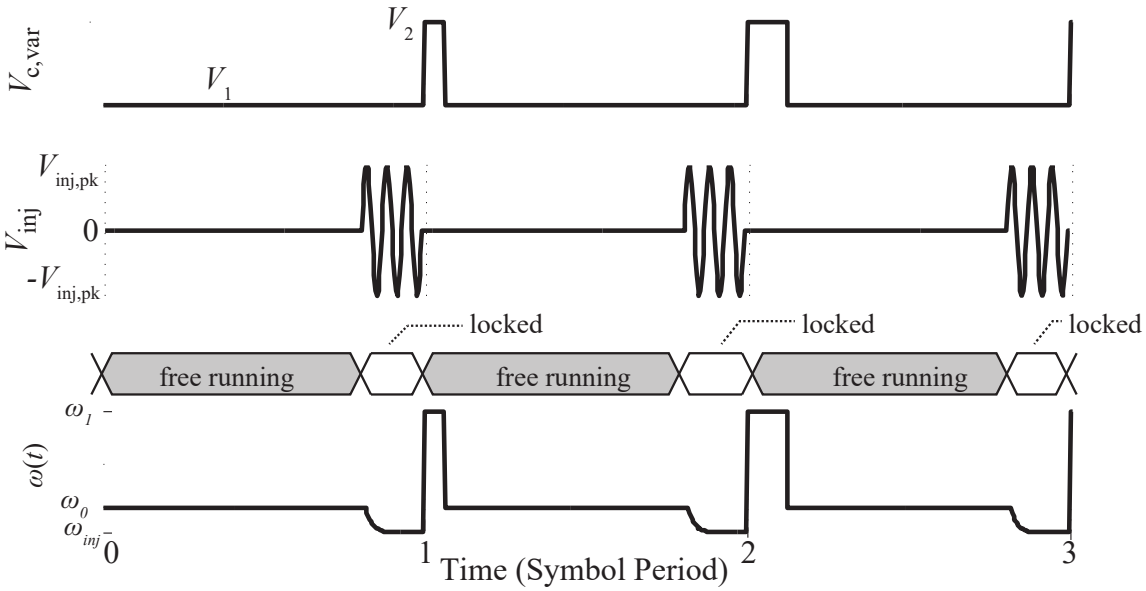


Figure 4.18: Conceptual plot showing the transmitter two modes of operation.

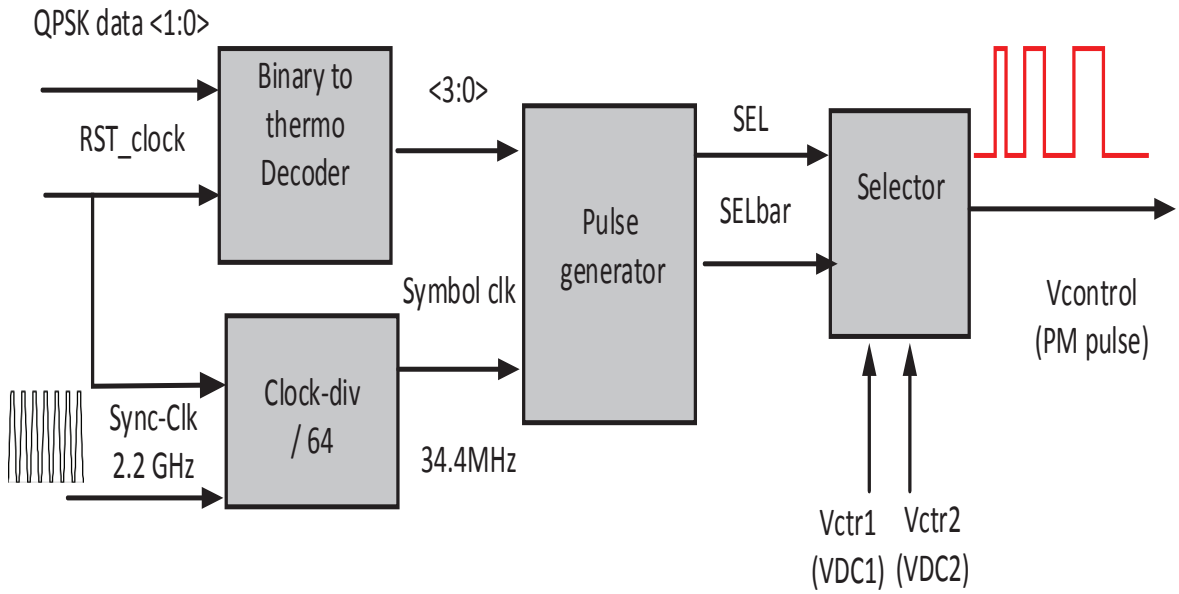


Figure 4.19: The block diagram of the digital circuit implementation of our new technique for phase rotation.

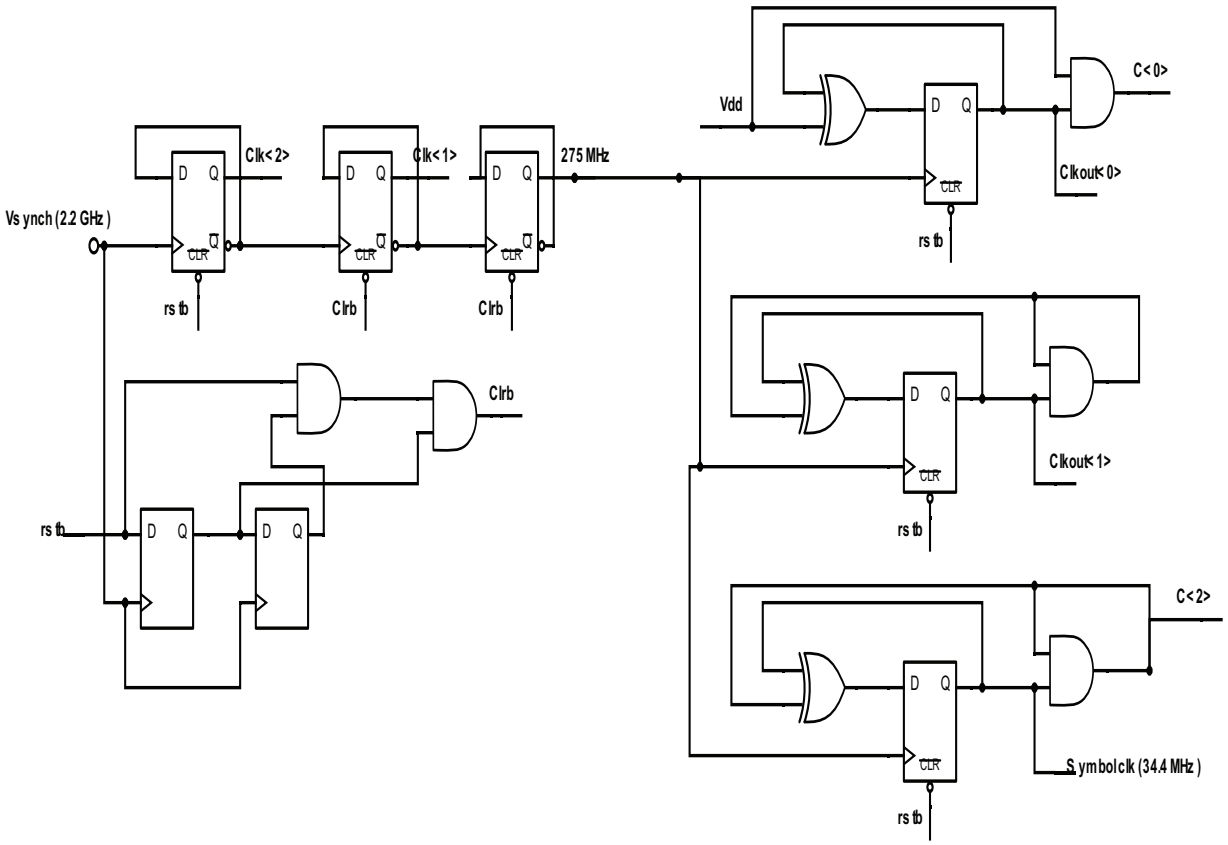


Figure 4.20: The frequency division digital circuit design.

Clock Division

Sync-Clk is used to generate an accurate symbol clock (Symbol-clk) of a 34.4 MHz using frequency division by a factor of 64. The frequency division is illustrated in Fig. 4.20. It consists of three high speed stages (divided by 8) and three low speed stages (divided by 8). The high speed and the low speed stages consist of three identical (divided by 2) synchronous D-Flip-Flop stages. Fig. 4.21 shows the transient analysis for the divide by 2, 4, 8 signals for the fast and the slow tracks.

Binary to Thermometer Converter

In order to convert the two QPSK binary signals $[1:0]$ into pulses that can be used in PM, the data is converted to thermometer code as shown in Table 4.3, then, it is loaded in parallel to an 8-stages shift register. At the beginning of each symbol period, the shift register output is serially streamed out. Fig. 4.22 shows the digital

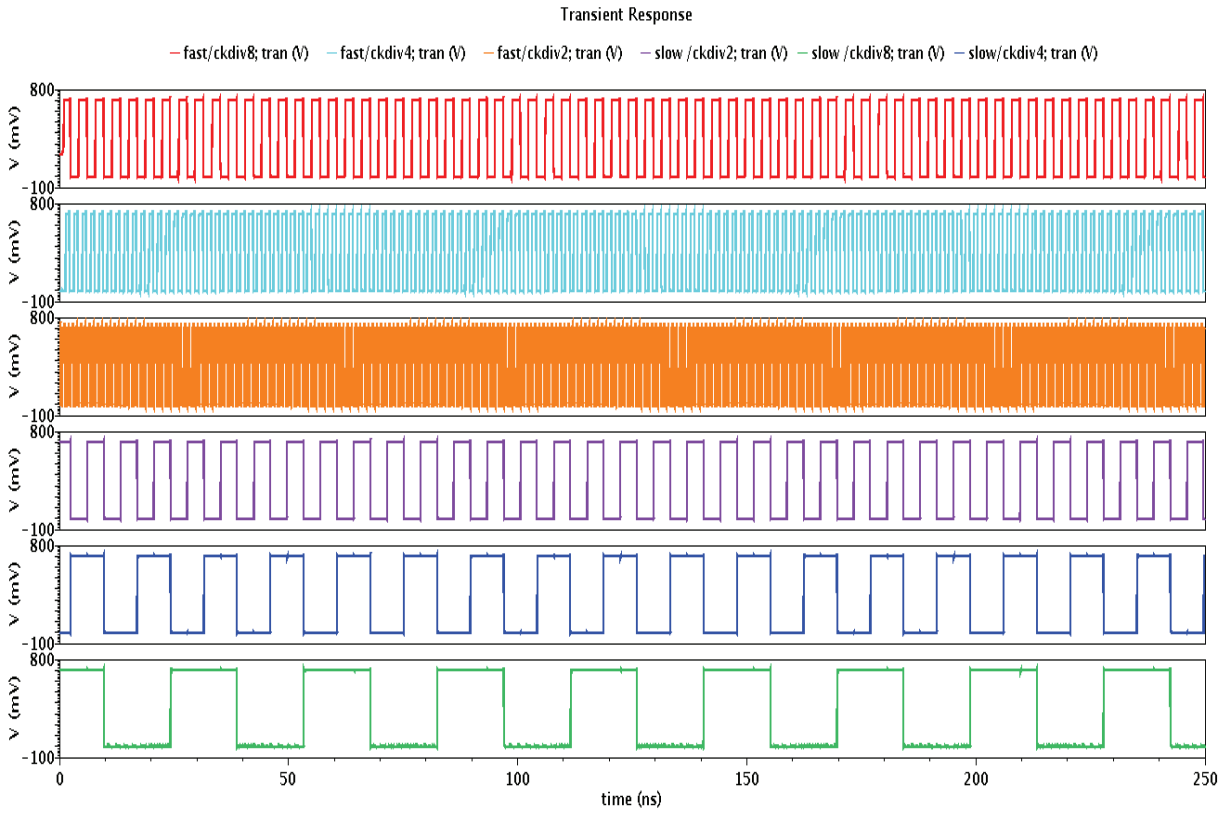


Figure 4.21: The transient analysis of the two tracks (fast and slow) frequency division to generate the symbol clock.

Table 4.3: QPSK input data and PM pulse width

Binary	Thermo
00	000
01	001
10	011
11	111

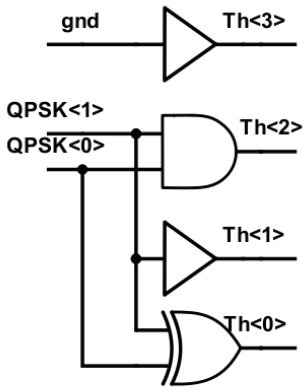


Figure 4.22: Circuit design of binary to thermometer converter.

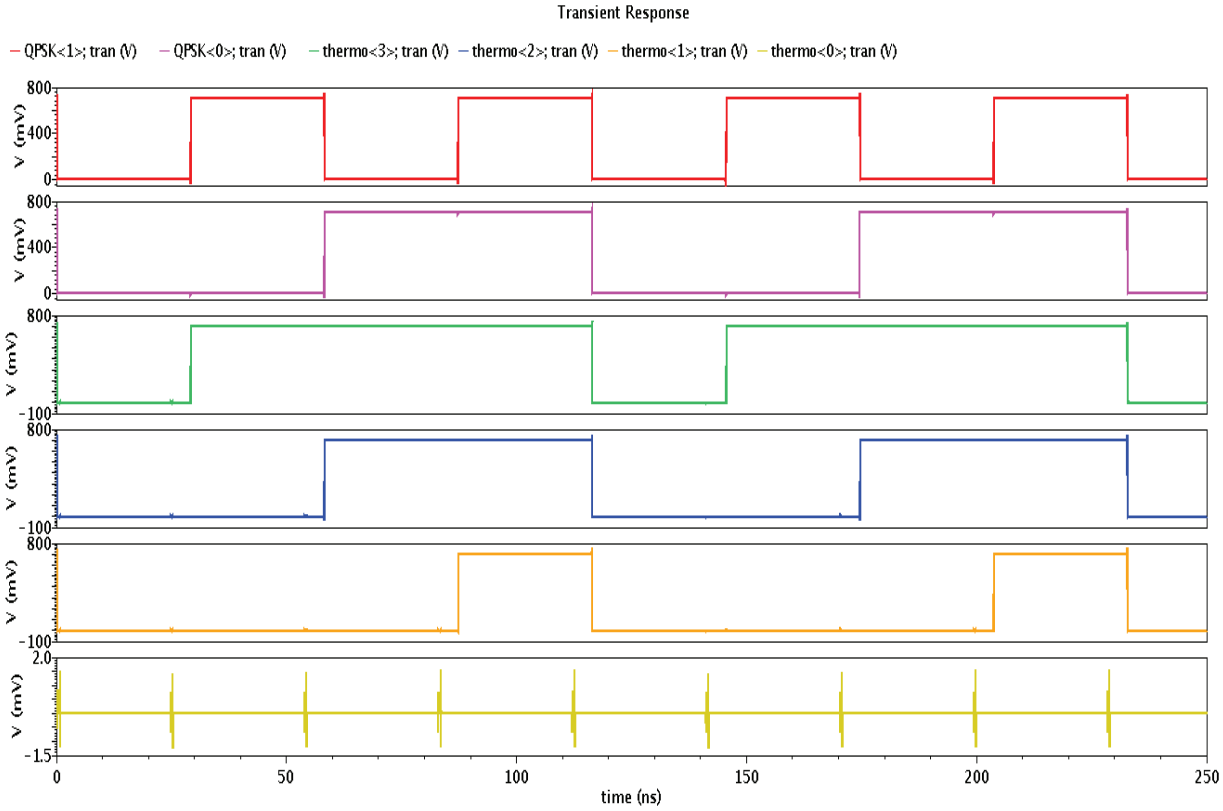


Figure 4.23: The transient analysis of the binary to thermometer converter.

circuit of the converter. The transient analysis of the two binary input bits and the three thermometer output bits are illustrated in Fig. 4.23.

Variable Pulse Width Generator

The pulse generator is designed to generate short pulses for PM ($V_{control}$). Table 4.4 presents the relationship between the serial two binary bits, the three parallel thermometer bits, and the associated PM pulse width. When the input data is 01, the phase is rotated 90^o and the pulse width is set to 0.41 ns (one period of the carrier generator). When the input data is 10, the phase is rotated 180^o and the width is set to 0.83 ns (twice the period of the carrier generator). When the input data is 11, the phase is rotated 270^o and the pulse width is set to 1.23 ns (triple the period of the carrier generator).

To allow the selection of two different frequencies (2.4 GHz and 3 GHz), two DC control voltages V_{ctr1}, and V_{ctr2} are provided externally where V_{ctr1} equal to 0.6 V and V_{ctr2} equals to 0.9 V. A transmission gate controlled by the pulse generation circuitry is used to select the voltage to be fed to the varactor. Note that the transmission gate must be sized carefully to drive a large capacitive load. Fig. 4.24 shows the schematic of the pulse generator and the DC voltage selection. Fig. 4.25 illustrates the transient response of QPSK two bits and $V_{control}$.

Table 4.4: QPSK input data and phase modulation pulse width.

Binary	Thermo	Pulse-width
00	000	0
01	001	0.41 ns
10	011	0.83 ns
11	111	1.23 ns

4.3.4 Transmitter Two Modes of Operation

Fig. 4.26 shows the transmitter two modes of operation: the free running mode (PM mode) and the locking mode (no PM). The complete operating sequences and the input QPSK data are demonstrated which include the following: V_{inj}, QPSK$<1>$,

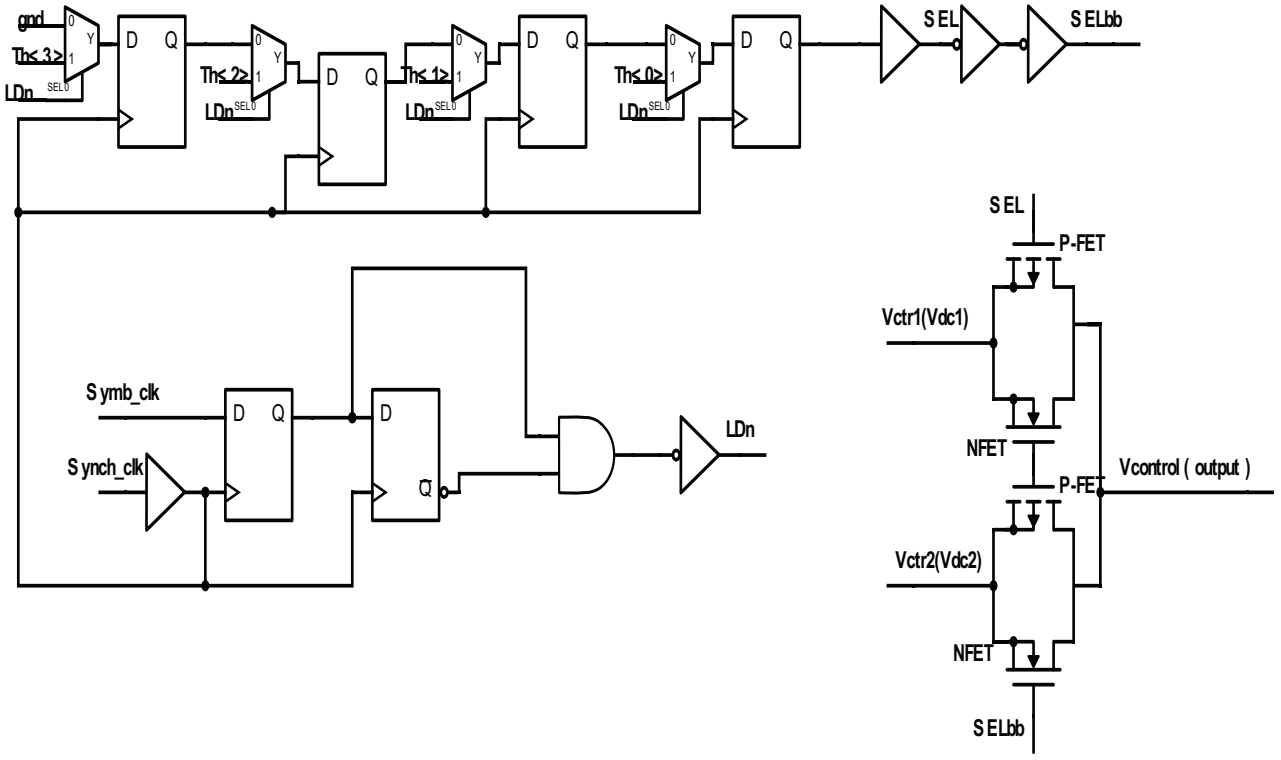


Figure 4.24: The circuit design of the pulse generator and the DC selection.

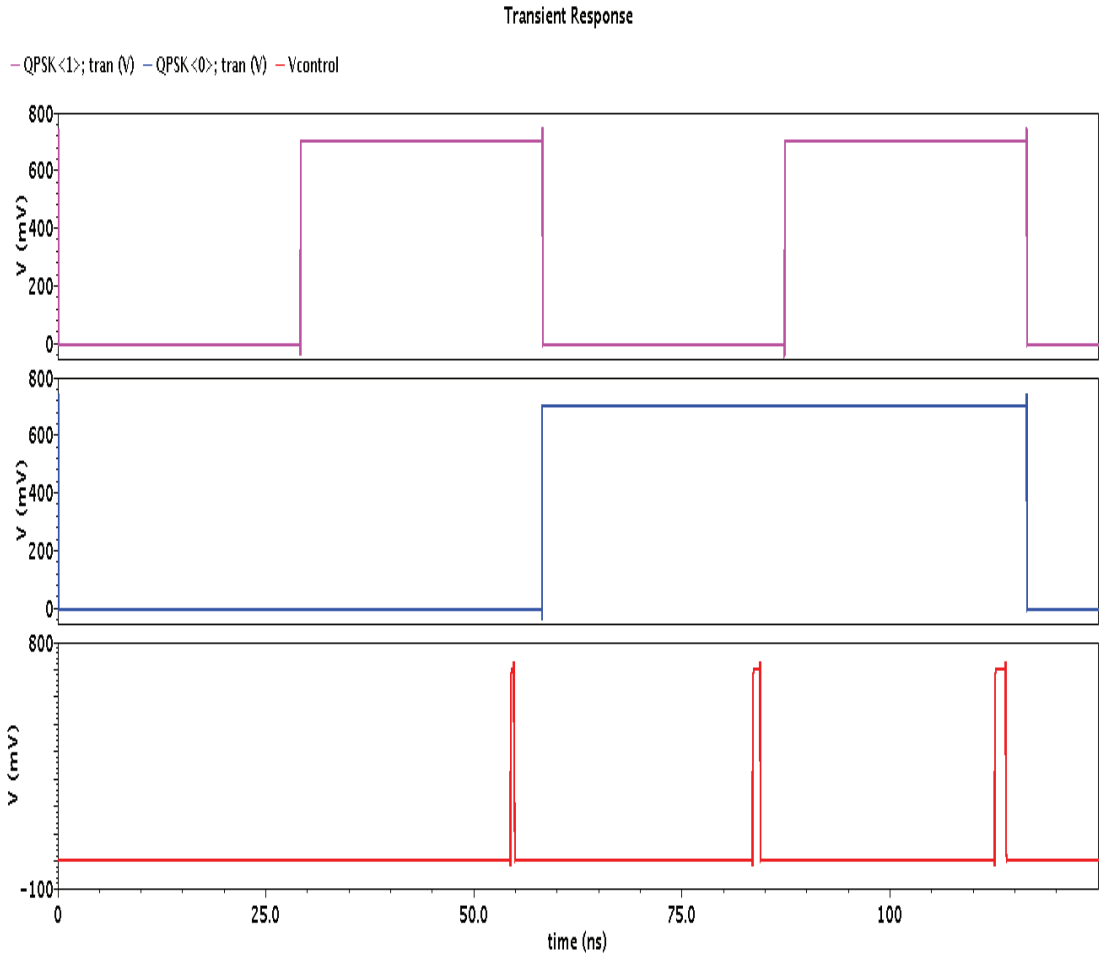


Figure 4.25: The transient analysis of the PM control pulses for 2-bits symbol.

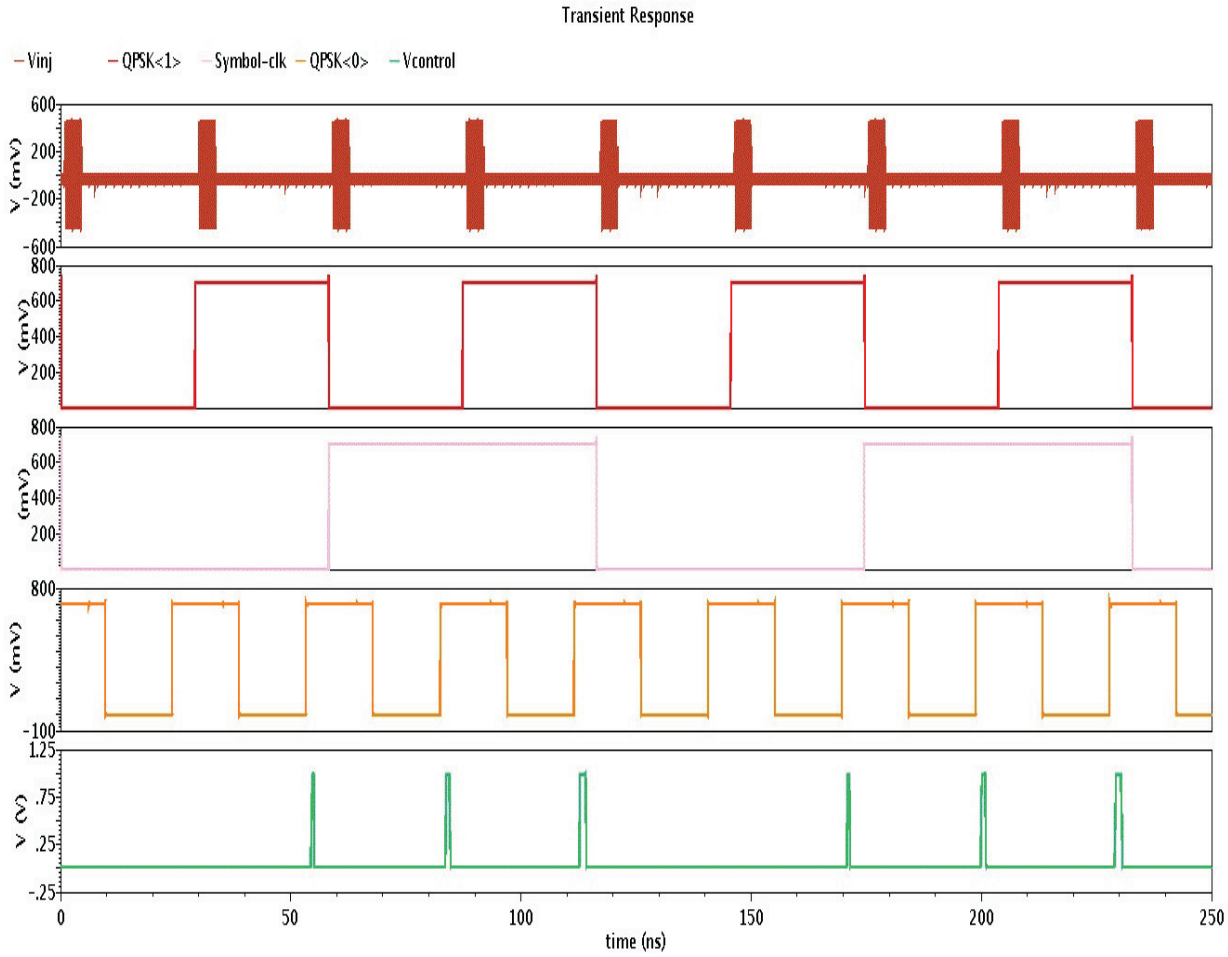


Figure 4.26: Time domain analysis for IL synchronization (enable-inj), symbol clock and modulation pulse ($V_{control}$).

QPSK$< 0 >$, Symbol-Clk and $V_{control}$. The transmitter is locked to a refrence signal for a very short time and runs free during PM at a symbol clock equal to 34.4 MHz to achieve a data rate of 69 Mbps. Note, the modulation pulse $V_{control}$ is applied at the free running mode (the V_{inj} signal is disabled) as presented in Fig. 4.27 for the QPSK output signal. Fig. 4.28 shows the zoom-in result of the transmitter output signal during the PM.

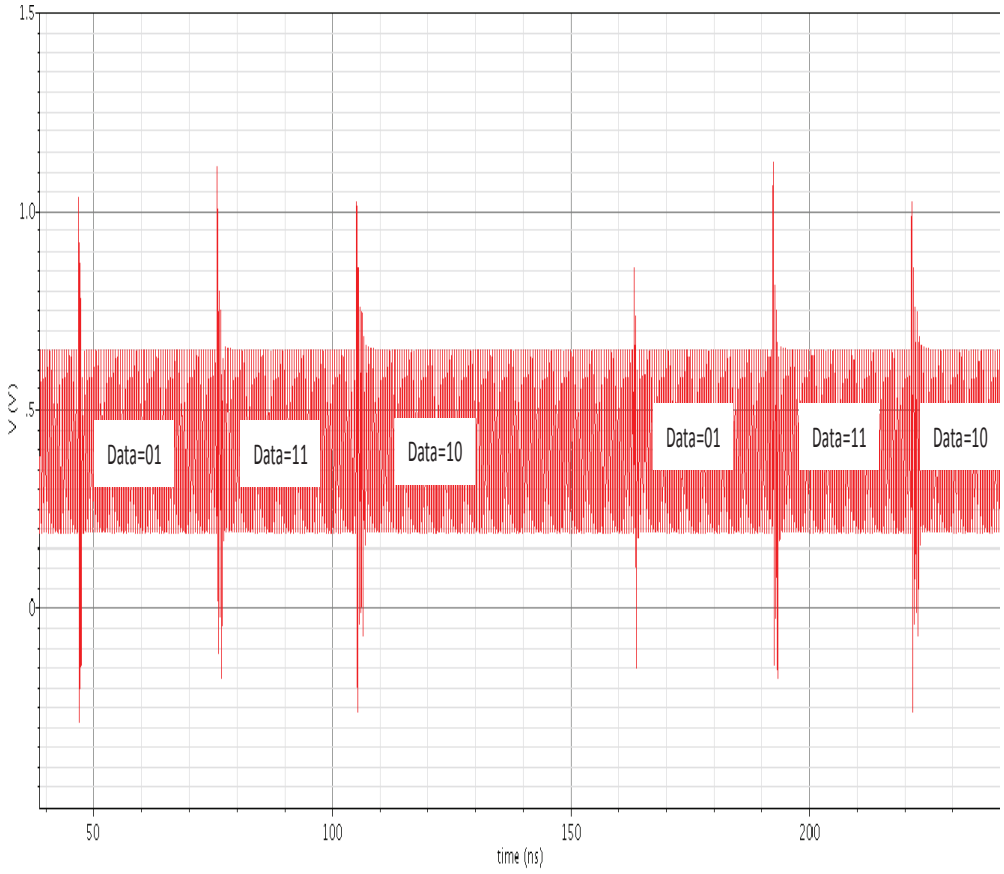


Figure 4.27: The Simulated output QPSK signal when data rate is 69 Mbps.

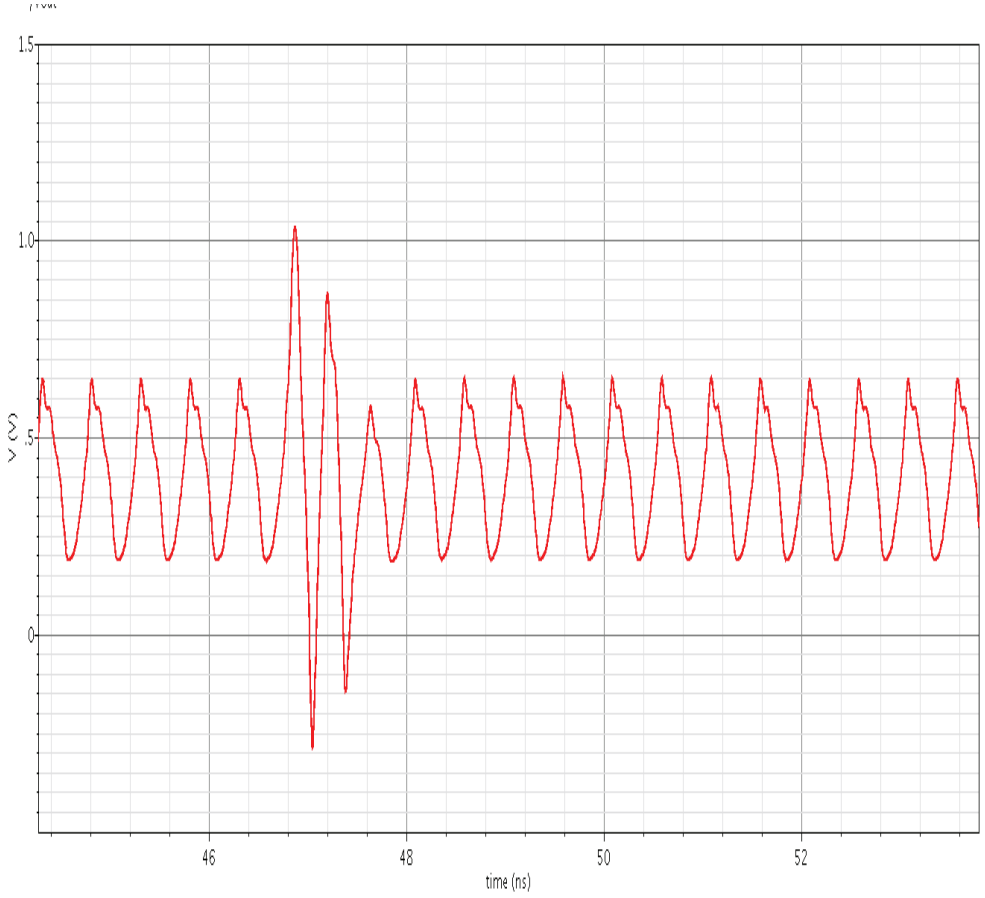


Figure 4.28: The zoom-in view for the output QPSK signal when input data is 01.

4.4 EVM Considerations

Since the quality of the transmitter is highly dependent on the quality of the carrier such as PVT variations, the robustness of the oscillator is examined. The class-E oscillator can be tuned between 1.99 GHz and 3.3 GHz when the DC voltage varies between 0 V to 1.5 V. Note, the required tuning range to implement the new PM technique is between 2.4 and 3 GHz. We extend the operating frequency ±17% to be between 1.99 and 3.3 GHz to compensate for the PVT variation.

The process variation effect on oscillation frequency is depicted in Fig. 4.29(a), the results specify that a frequency deviation is between 10-20% for the two extreme corners slow-slow (SS) and fast-fast (FF). The simulation results in Fig. 4.29(b) show that for a $\mp 10\%$ power supply variation, the frequency offset is $1 - 12\%$. Regarding temperature variations, the simulations indicate that within the temperature range of 0^oC to 100 ^oC, the frequency offset is $2 - 7\%$ as illustrated in Fig. 4.30. The oscillator is robust to $\mp 20\%$ frequency deviation due to PVT variations.

Based on the frequency resolution, the RMS phase error can be found as in (4.23). For a small phase error (assuming negligible amplitude error), EVM is mainly dominated by the phase error and can be estimated as the following:

$$\theta_{error} = 2\pi\Delta(\frac{f_i}{f_c}) \tag{4.23}$$

$$EVM_{rms} \backsimeq sin\ \theta_{error} \tag{4.24}$$

For the worst case of 20% of the frequency offset $\Delta(f_i/f_c)$ due to PVT variation, the phase error equals 6.28^o and the equivalent EVM equals 10.93%. To achieve a row BER better than 10^{-4}, an EVM better than 23% is required with a phase error equals to $\theta_{error} < 13.2^o$. That means the estimated EVM meets the requirement with a good margin.

4.5 Some Layout Issues

The proposed transmitter has been implemented in 65nm CMOS technology. The complete layout of the transmitter is shown in Fig.4.31 where it occupies an active

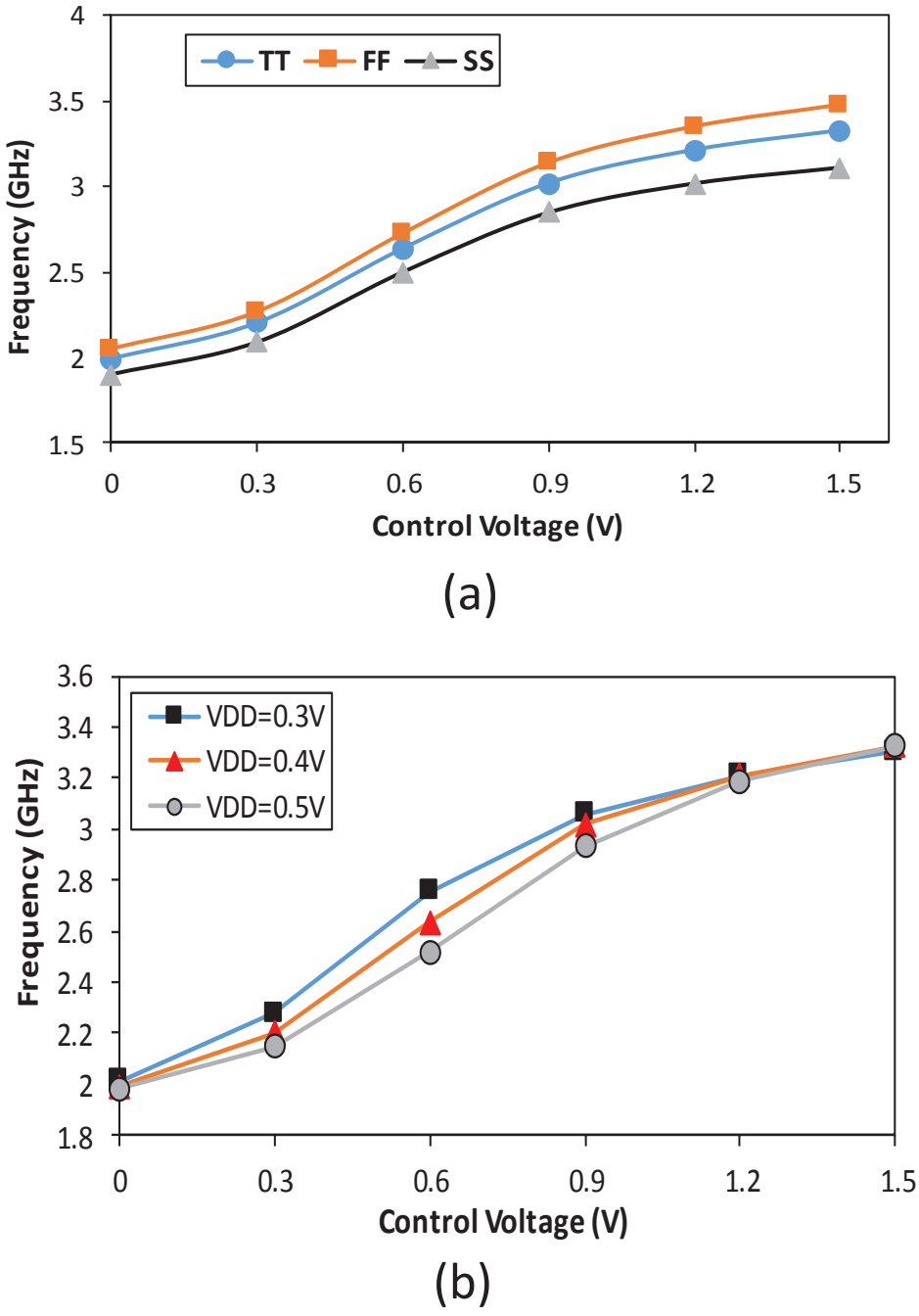


Figure 4.29: The oscillator tuning range under PVT variation (a) process effects with considering two extreme corners SS and FF(b) $\mp$10% power supply variation effects.

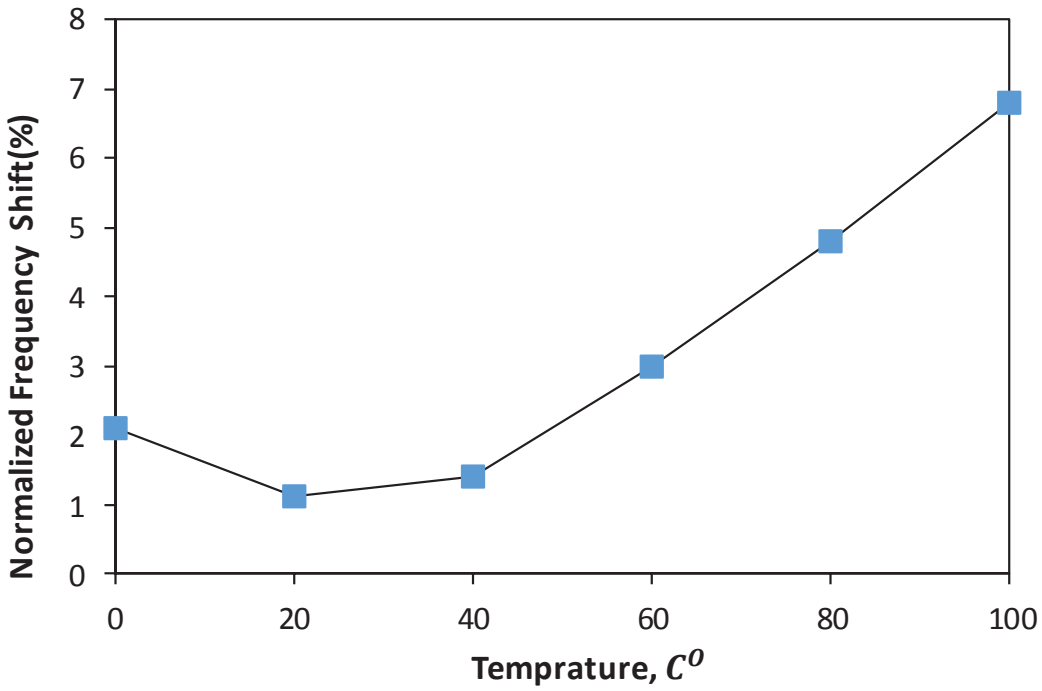


Figure 4.30: The temperature effect on the oscillator operating frequency.

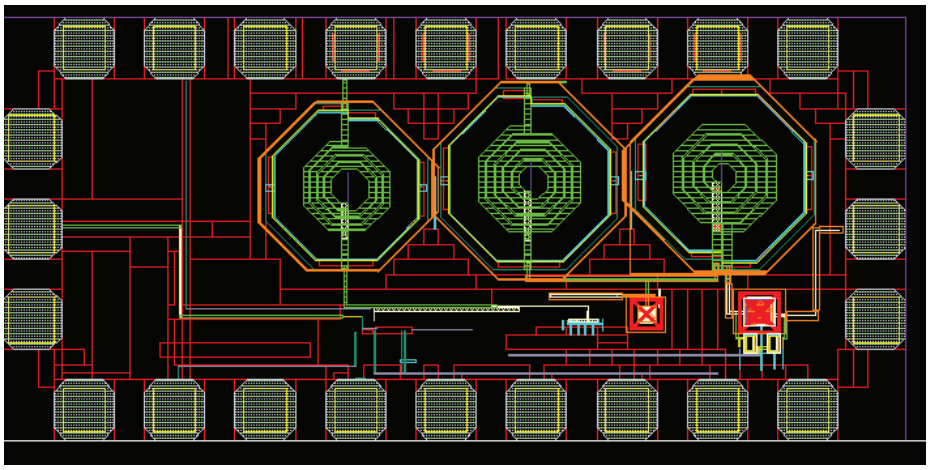


Figure 4.31: The fully integrated QPSK transmitter layout.

area around 600 μm X 600 μm. Our transmitter design is a mixed signal circuit, therefore extra care was taken in the layout. Electro-static discharge (ESD) protection is applied to all power rails to provide a DC discharge path to ground. The ESD protection is implemented using a P-N diode that is connected as shown in Fig. 4.32(a).

The digital and the analog blocks were isolated from each other to reduce the noise coupling. In addition, guard rings (which include P or N oxide layers and a metal one with many contacts) were used to isolate the analog and the digital circuit. The power supply and the ground are separated for the digital and the analog parts. Regarding the analog part, multiple power supply pads are added so that each block can be tested individually as demonstrated in Fig. 4.32(b). For the transistor layout, multiple fingers were used to minimize gate resistance and noise.

The chip resources were divided into three categories power, grounds and RF. It includes seven RF output pads, seven power supplies and ten grounds with bypass capacitors for supply lines. The ground plane includes the metal layers M_1, M_3, M_5, M_7, M_9. The power plane includes M_2, M_4, M_6, M_8 which are used to maintain a uniform metal density in the chip. The I/O pads definitions are listed in Table.4.5.

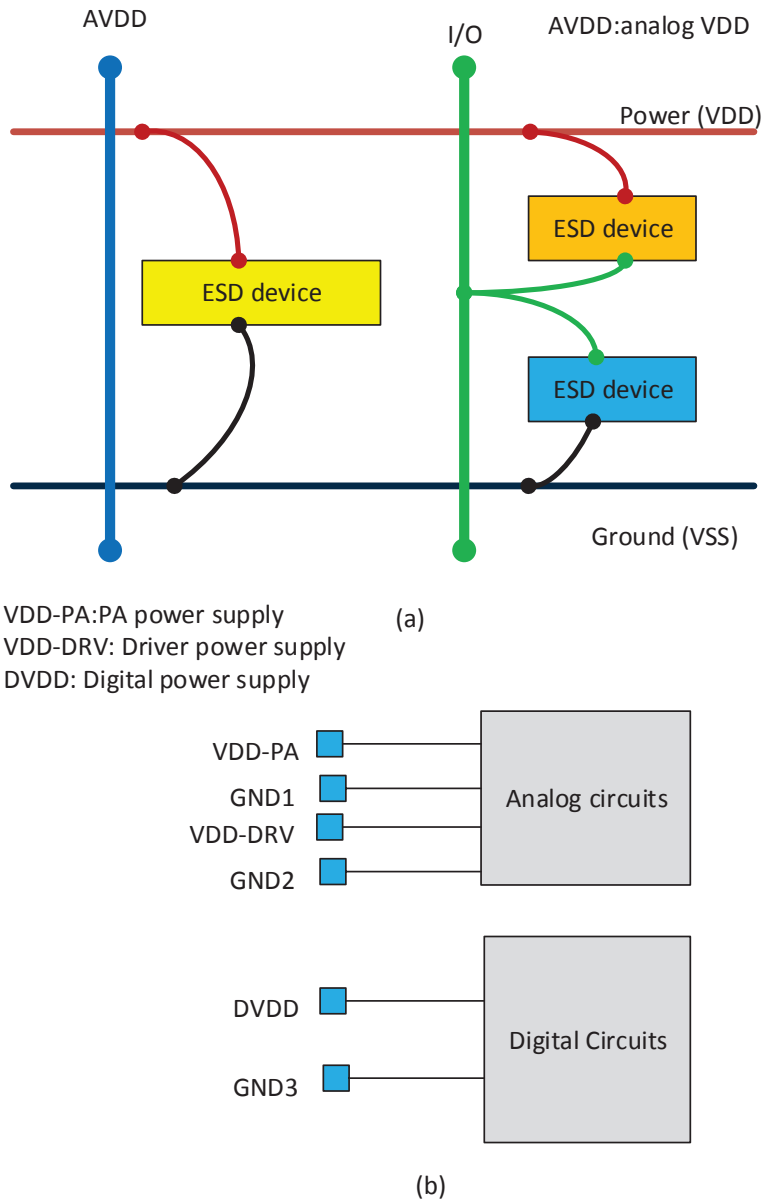


Figure 4.32: Conceptual diagram for the mixed signal layout techniques (a) ESD protection (b) I/O pads.

Table 4.5: I/O Pads definitions.

I/O pads	Function
VDD DRV	Driver power supply (2 pads)
EN INJ	Enable clock
CLK IN	RF input synchronous signal
RST	Reset clock
DVDD	Digital power supply
CLK SYMB	Vcontrol pulses (output)
QPSK< 1 >	Input data (bit 1)
QPSK < 0 >	Input data (bit 2)
VCTR1	DC voltage 1
VCTR2	DC voltage 2
VOUT	RF output voltage
VDD PA	PA power supply (2 pads)
GND	Ground

4.6 The Test Plan

The fabricated RF integrated circuit is packaged in a ceramic flat pad (CFP) and all the measurements have been performed on a packaged chip using a 24-Pin CFP (CFP24TF) printed circuit board test fixture shown in Fig. 4.33 which has short bond wires and this in turn reduces wire parasitics. The CFP24TF utilizes a 4-layer board with the outer layers separated from ground planes by a low-dielectric and low-loss material. The board resources are divided into three categories: power, grounds and RF lines.

The input pulses EN INJ,RST and RF input refrence CLKN IN were generated by Agilent technology E4438C and 33250A signal generators. Fig. 4.34 shows the complete test setup for the device under test. The internal pseudo random bit signal

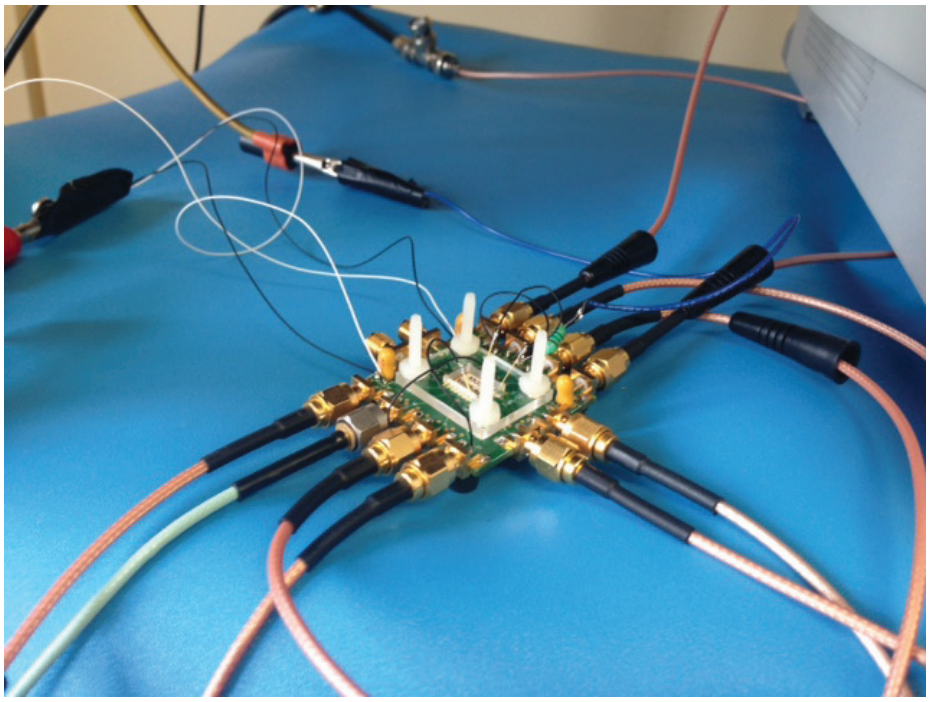


Figure 4.33: The prototype transmitter chip mounted on the RF testing fixture with all the inputs connected.

(PRBS) data sequences from BERT 200 transceiver (shown in Fig. 4.35) is applied to the transmitter. An Agilent N9342C spectrum analyzer is used to measure the output spectrum.

4.7 The Experimental Results

The QPSK transmitter is fabricated in 65 nm CMOS technology with a die area of $1mm^2$ as shown in Fig. 4.36. A couple of the packaged chips were damaged during the measurements and the following reported results are from three chips.

First, the characteristics of the power oscillator were verified. Fig. 4.37 shows the simulated and the measured operating frequency for the three characterized chips. Note, the measured frequency range is different from the one in simulation results which is mainly due to the parasitic capacitance of the test-setup and the packaging. This deviation in frequency can be adjusted by the varactor control voltage.

Fig. 4.38 shows the output peak voltage simulation and measurement results as a function of frequency. The difference between the simulation and the measurement

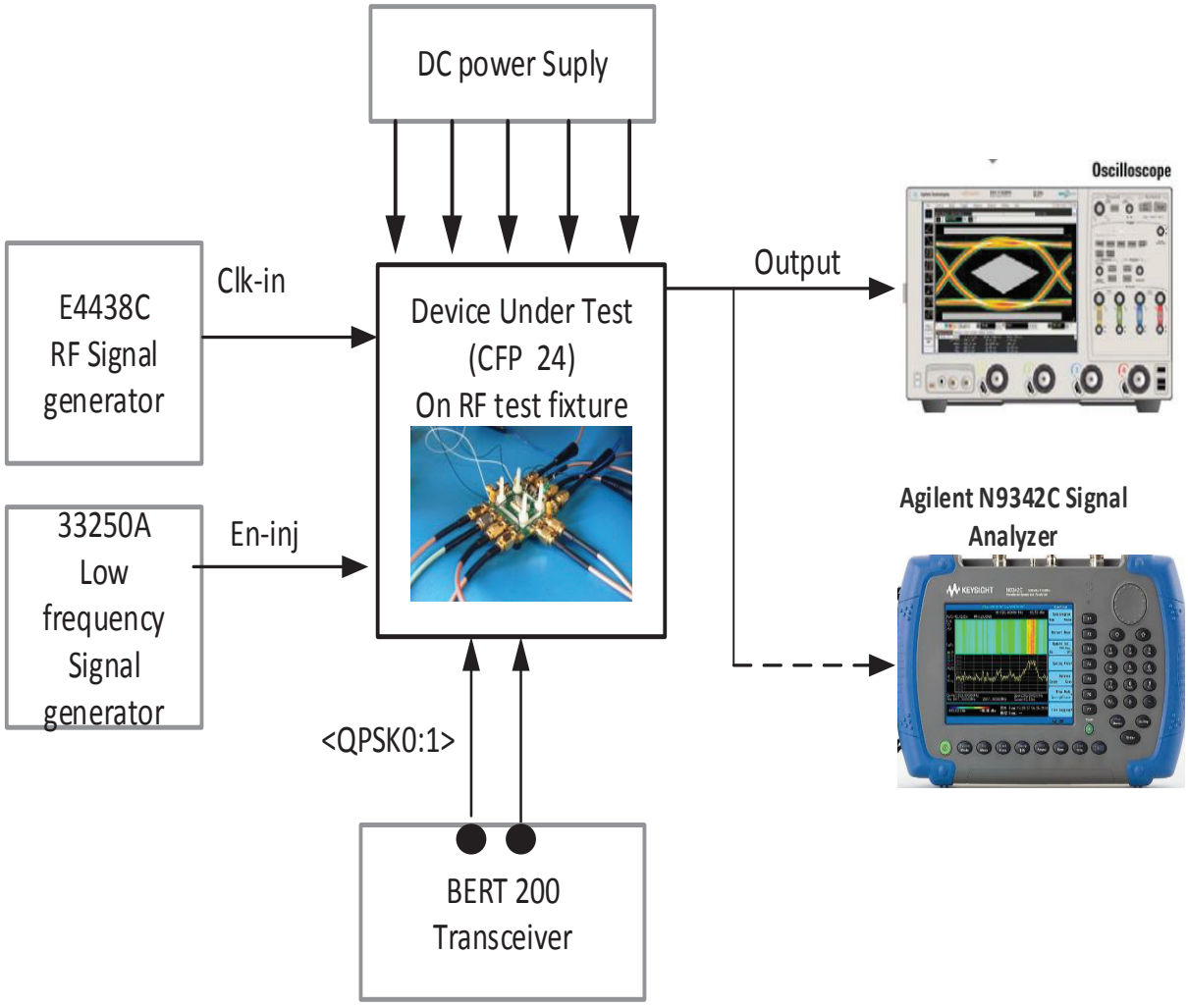


Figure 4.34: The test setup for the transmitter prototype.

Figure 4.35: Input PRBS sequences used in testing the transmitter.

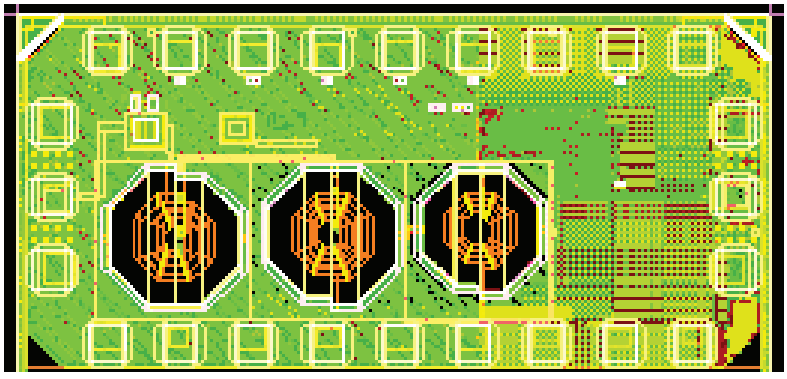


Figure 4.36: The proposed QPSK transmitter die photograph.

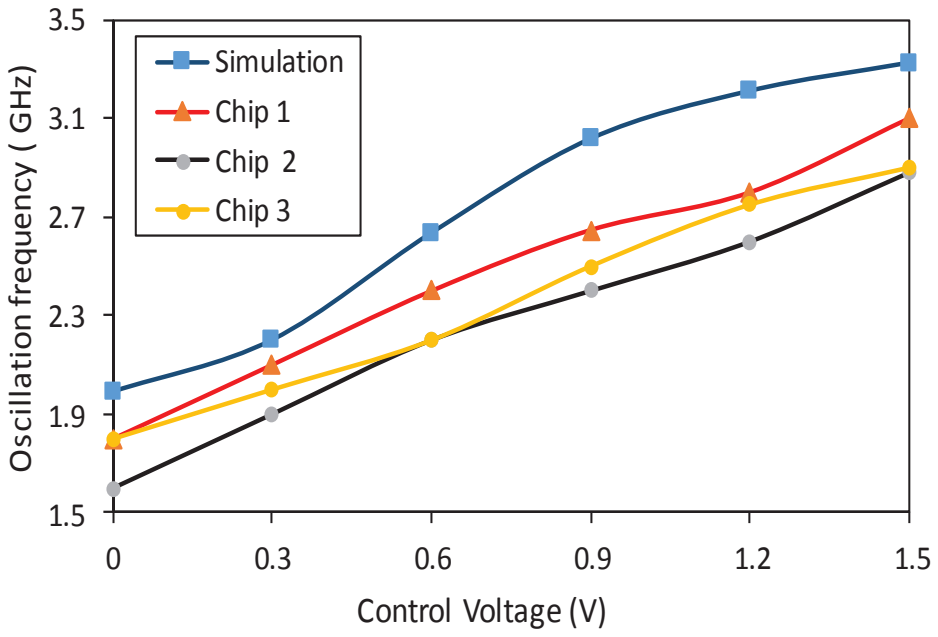


Figure 4.37: The simulation and the measured results of the oscillation frequency.

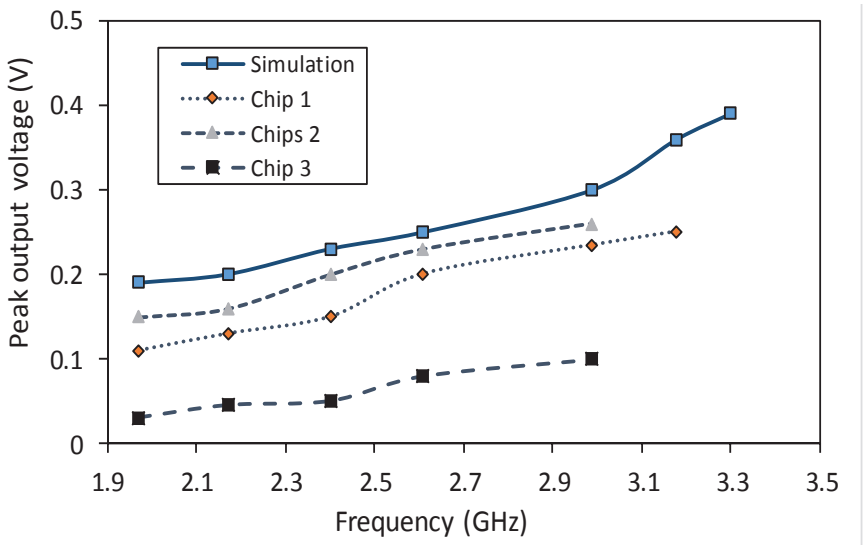


Figure 4.38: The measured and the simulated peak voltage comparison of the fabricated transmitter.

results is mainly due to the losses that result from the voltage drop on the parasitic and coupling capacitors due to bonding-wires, packaging and PCB traces.

Fig. 4.39 shows the measurement results of the QPSK transmitter global efficiency (which is the output power divided by power consumption). As can be seen, the efficiency is higher than 10% and 20% at 2.4 GHz and 3 GHz respectively. There is a negligible variation in the DC power consumption, however, the differences between the results of different chips are related to process variation effect.

Fig. 4.40 and Fig. 4.41 show the captured oscillator output voltage signals on the oscilloscope. In these figures, the frequency is approximately 2 GHz and 2.4 GHz respectively. The peak-to-peak voltages are 60 mV and 99 mV respectively. Fig. 4.42 shows the captured QPSK output signal on the oscilloscope. In this figure, the measured modulated signal is 186 mV peak-to-peak to achieve a 69 Mb/s of data-rate. Unfortunately, we couldn't import the data to compare them with simulation results shown in Fig. 4.25.

At the frequency domain, the transmitter performance is characterized using a signal analyzer to measure the power spectral density (PSD) of the transmitter. Fig. 4.43 demonstrates the measured un-modulated output spectrum of the carrier at -6.7

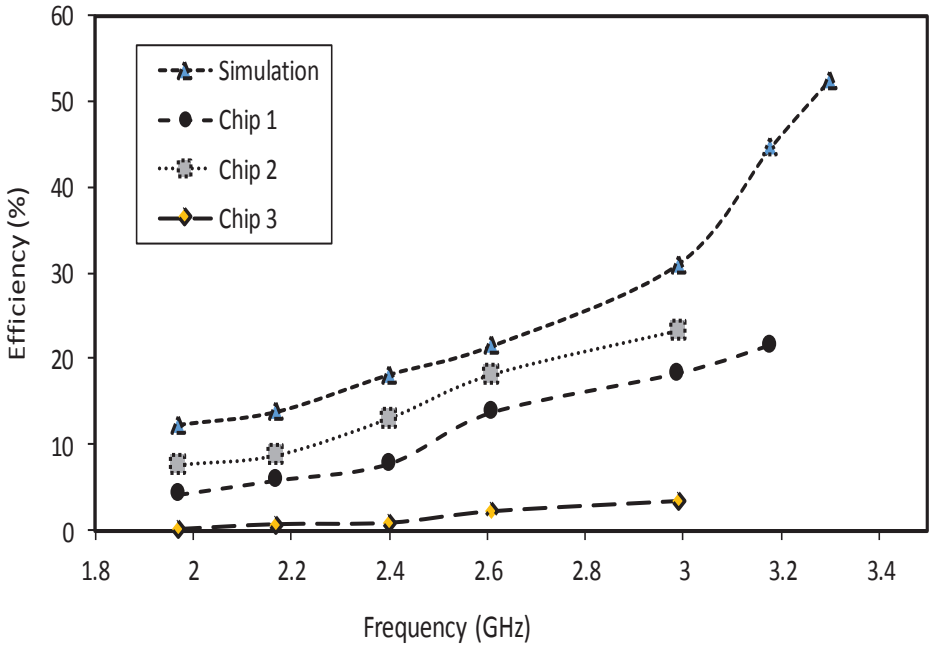


Figure 4.39: The simulation and the measured transmitter efficiency as a function of frequency.

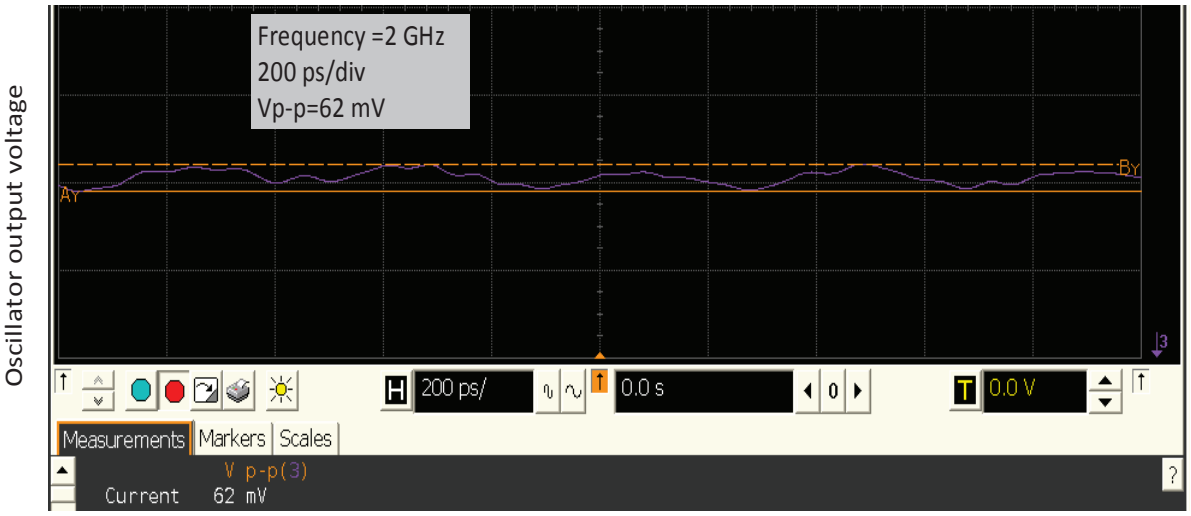


Figure 4.40: The captured power oscillator output voltage at time domain.

dBm output power. As can be seen, the center frequency doesn't fit exactly between 2.4 GHz and 2.48 GHz of the ISM band. This can be adjusted using the control voltage. Fig. 4.44 shows the modulated output spectrum of the carrier of -6.82 dBm output power at 69 Mbps data rate.

The prototype transmitter performance and the experimental results are summarized and are compared with other similar multi-PSK transmitters in Table 4.6. The prototype transmitter achieves the highest data rate with the lowest power consumption, resulting in a good energy/bit performance. The complete QPSK transmitter consumes only 2.9 mW. It achieves an energy efficiency of 42 pJ/bit at a data rate of 69 Mb/s.

$$FOM = \frac{P_{out}.Data\ rate}{Power\ consumption}(\mu W.\frac{bit}{nJ}) \tag{4.25}$$

Note that most of the transmitters listed in the comparison table have a limited output power between -9 to -15 dBm. Due to the lower output power, their overall transmitter power efficiency are limited. We have achieved a high global efficiency of 13% at 2.4 GHz and 23% at 3 GHz. In addition, this transmitter still compares favorably to other relative works even when we adopt the commonly used figure of merit (FOM) [60] found in (4.25). We achieved the best FOM of 5882 $\mu W.bit/nJ$. Finally,

Figure 4.41: The captured oscillation frequency of the power oscillator at time domain.

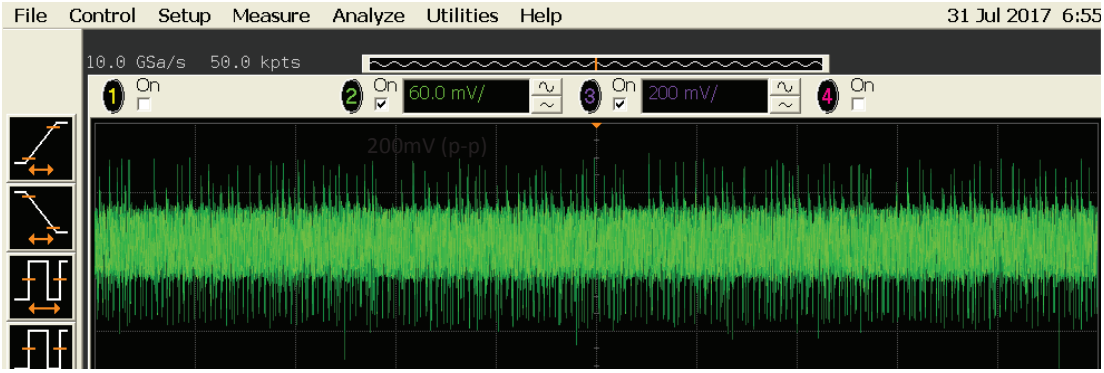


Figure 4.42: The captured QPSK modulated output signal at a data rate of 69 Mbps.

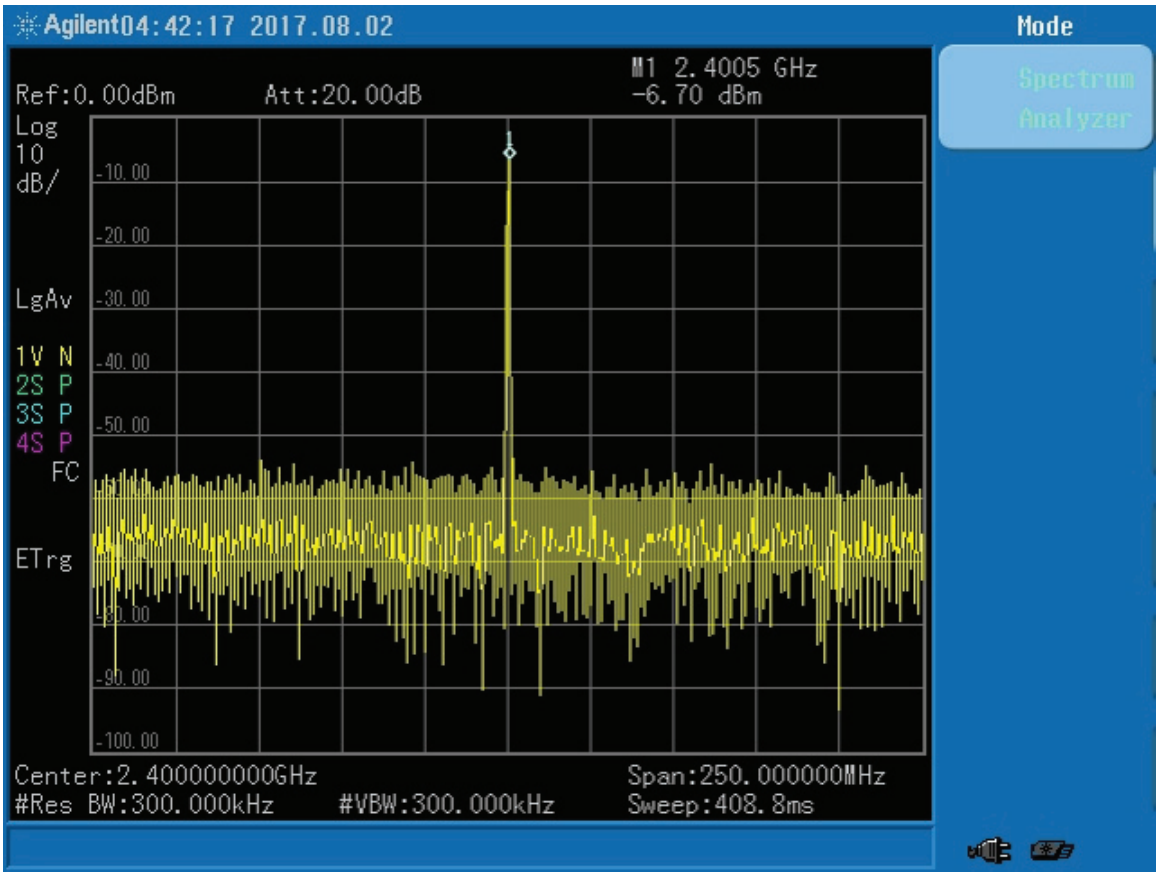


Figure 4.43: The measured transmitter un-modulated PSD.

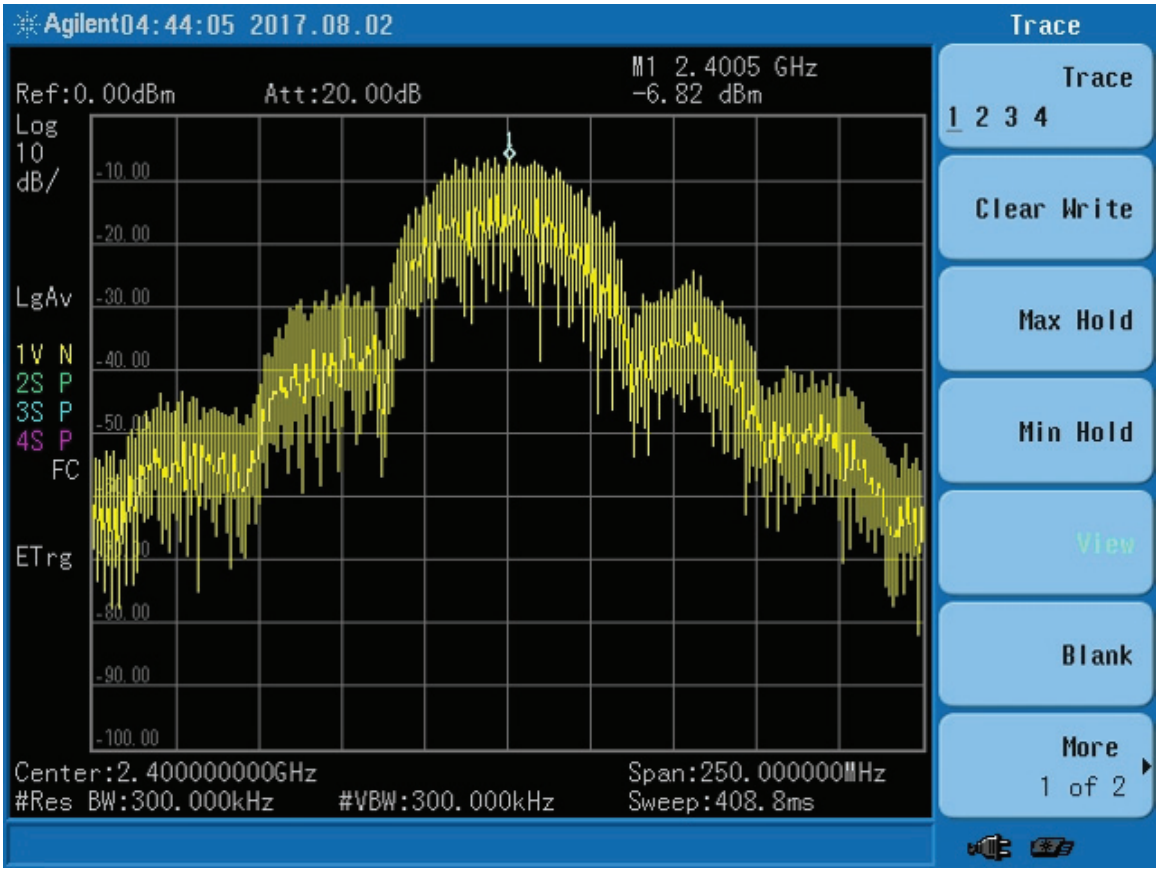


Figure 4.44: The measured transmitter modulated PSD.

Table 4.6: A Performance Summary and a Comparison with Other Transmitters.

Specification	[35]	[32]	[43]	[36]	[34]	This Work
Frequency(MHz)	400	915	2400	400	400	2400
Data rate (Mbps)	17.5	50.8	1	12.5	20	69
Supply voltage (V)	1.2-1.8	1.8	1.8	0.9	0.9	0.4
Tx global efficiency (%)	4.2	N/A	17.4	1.16	6.8	23
Modulation	QPSK	QPSK	FSK	PSK	PSK	QPSK
Power Consumption(mW)	3.5	5.9	3.7	2.57	2.2	2.9
Output power(dBm)	-8	N/A	-5.7	-15	-8	-6.8
Energy/bit(nJ/bit)	0.2	0.116	3.7	103	110-440	0.042
FOM	2013	1250	54	146	1363	5882
Technology(nm)	180	180	130	65	65	65
Core area(mm^2)	0.06	0.024	N/A	0.4	0.23	1

Fig. 4.45 compares this work with other low-power transmitters in terms of the data rate and the power consumption. It clearly shows that we achieved the highest data rate and the best energy efficiency among QPSK transmitter architectures for WSN.

We couldn't measure EVM nor capture the constellation diagram because we did not have a spectrum analyzer in our lab nor in our university. However, the EVM was estimated from the measured oscillation frequency as in (4.23). The estimated EVM is around 10.93% which still meets the BER requirement.

The testing and measurements are a challenging part of the RF circuit implementations and verifications due to many reasons, such as, the luck of certain testing equipment and RF cables or even the logistics during the experiments due to long term construction in the university.

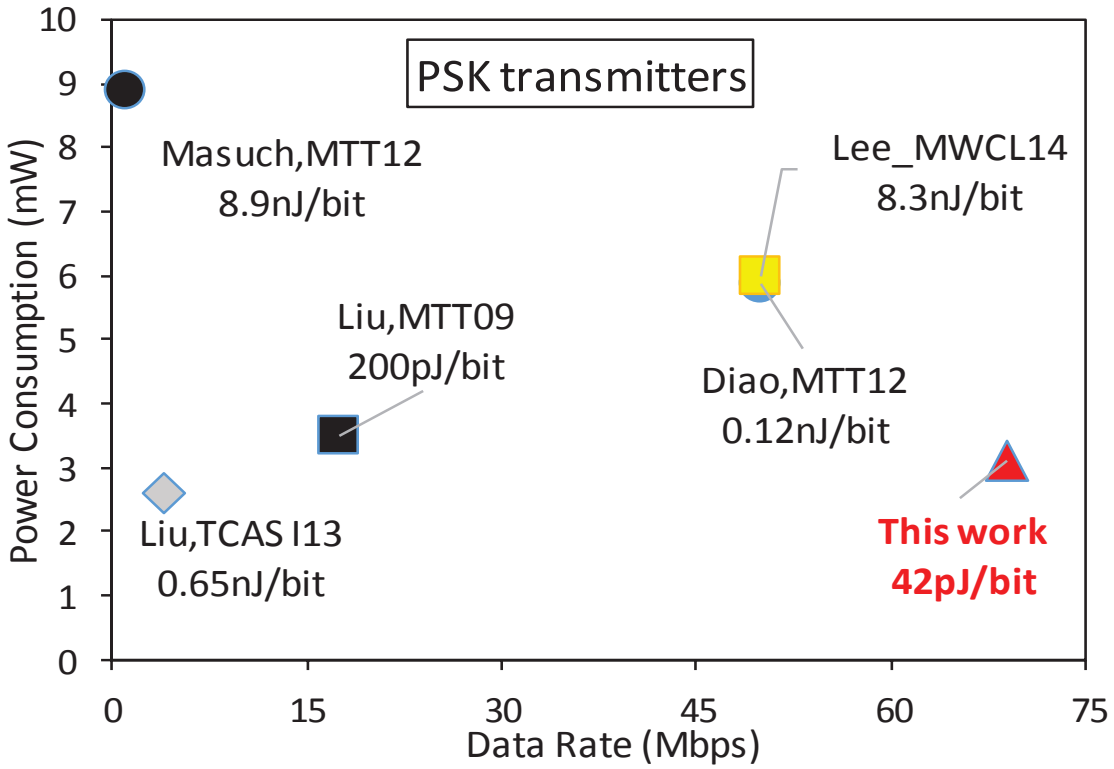


Figure 4.45: A comparison of the recent energy-efficient PSK transmitters.

4.8 Summary

An energy-efficient QPSK transmitter is presented. This transmitter is suitable for a short range biomedical imaging application and operates at 2.4 GHz with a data rate of 69 Mbps and transmitting power of -6.8 dBm. A new PM technique is presented and a detailed analysis is discussed along with the derivation of the mathematical equations.

A class-E power oscillator is the core of the design which is directly modulated to simplify the design and to reduce the power consumption. The performance of the class-E transmitter which is fully integrated in CMOS technology could be one of the choices for wireless transmission in BAN, WSN or portable applications with achieved energy/bit of a 42 pJ/bit and a 2.9 mW power consumption.

The transmitter's global efficiency at 2.4 GHz is between 7% and 13% at 2.4 GHz and between 18% and 23% at 3 GHz with a 0.4 V power supply. The class-E VCO is tunable between 1.9 GHz and 3.3 GHz. The class-E VCO is robust to $\mp$20% frequency deviation due to PVT variations and the phase noise performance is between -115 dBc/Hz to -125 dBc/Hz.

The achieved performance of the implemented transmitter was compared with similar state-of-the-art transmitters showing a significant improvement in data rate, power consumption and efficiency.

Chapter 5

The Design of a Reconfigurable and Instantaneous Triple RF Band Energy Harvester

This chapter presents an autonomous energy harvester that is able to perform high RF power tracking to maximize the harvested DC power and to enhance efficiency [26]. The harvester has a tunable matching network that varies the input impedance of the main rectifier between 900 MHz and 1.2 GHz while the second rectifier harvests from 2.4 GHz band. The results show a peak efficiency of 57%, 43% and 33% at 2.4 GHz, 900 MHz and 1.2 GHz respectively. This work is part of a second chip that includes an RF-powered transmitter. The lack of funding prevented the fabrication of the prototype. However, all the results included in this chapter are post-layout.

This chapter is organized as follows: Section 5.2 provides a system overview of the proposed architecture. Section 5.3 discusses the system level considerations of the harvester design. Section 5.4 presents the model of a dual RF band harvester. In Section 5.5, the circuit design of the control loop is presented. In Section 5.6, a detailed methodology of the proposed dual RF-band matching network is presented. In Section 5.7, the circuit design is described. The simulations result and a discussion are presented in Section 5.9. Finally, the conclusions are formalized in Section 5.10.

5.1 Introduction

In order to facilitate the next generation of WSN, unlimited life time and a small footprint are required. As explained in Chapter 1, RF scavenging is the best candidate for a fully integrated energy harvesting system for non-invasive application. The RF energy is available from different communication services such as TVs, cell phones and radios which is distributed over a frequency range between 900 MHz and 2.4 GHz. However, this energy is limited due to the free space attenuation as well as other losses in the wireless channel such as multi-path, fading, reflection and absorption. Recall that the free space loss (L_P) is a function of the distance between the source

of the RF signal and the device as given by the Friis equation in [16].

$$L_P = (\frac{4\pi d}{\lambda})^2 \tag{5.1}$$

Where λ is the wavelength and d is the distance from the radiating source. In order to take full advantage of the available RF wide band, selection should be made based on the amount of available RF power. A multi-band energy harvester is a feasible solution to extend the bandwidth and to provide multiple power sources. Furthermore, it is possible today to design a dual or multi band RF rectifier using a single antenna thanks to the different architectures reported in the literature for the dual band antenna [61–63]. These structures opened the door for an area-efficient simultaneous multi band RF harvesting without the need for multiple antennas. The power conversion efficiency (PCE) is a very important figure of merit. The PCE is determined by the harvesting frequency, the input RF amplitude and the loading conditions. In the literature, many works have been reported to improve the efficiency by reducing the MOS threshold voltage [64–68]. In fact, a high of 80% and 85% PCE are reported in [65],[68] due to the lowered threshold voltage. However, these high efficiencies are achieved at high input voltages (3 V) and (4.5 V) respectively. Lower efficiencies are reported for lower input voltages [66], [67]. In a real environment, the RF power suffers from many losses as we mentioned before. Therefore, there is a need to track the high-power RF band to improve the efficiency. Recently, several designs were reported for multi RF band harvesting system [69],[70],[66]. In [69], a simultaneous dual band energy harvester is presented. The design uses a pre-set biasing network to reduce the threshold voltage. It uses an array of large off-chip resistors and capacitors that limit the efficiency to 9.1% at 900 MHz and 8.9% at 2 GHz. In [66], the proposed structure did not harvest from dual RF bands simultaneously and did not generate multiple voltage sources. In fact, only a single source at each allocated frequency was presented.

5.2 Triple-Band Energy Harvester

The proposed solution relies on the extraction of the DC power from three radio waves that are transmitted by three separated hubs that provide strong and reliable power

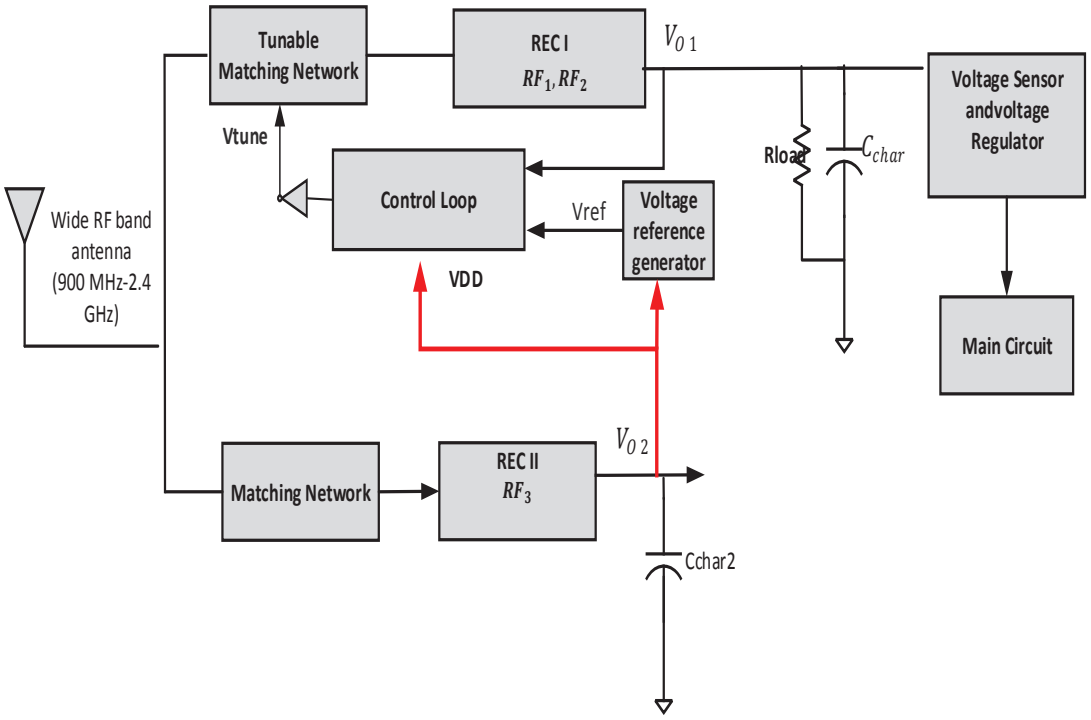


Figure 5.1: System overview of the proposed RF energy harvester.

at 900 MHz, 1.2 GHz and 2.4 GHz bands respectively.

Fig. 5.1 shows the block diagram of the RF harvester with a control loop and a tuning matching network. The control loop improves the harvester robustness and tracks the maximum RF power.

The harvester is comprised of two converters: the main rectifier (REC I) and an auxiliary rectifier (REC II) that simultaneously converts the RF power of 900 MHz, 1.2 GHz and 2.4 GHz to DC voltages. The harvested power from REC I is accumulated at a large storage main capacitor (C_{char}) to provide the required energy to power-up our main circuit, while REC II stores the accumulated power at the capacitor (C_{char2}) to power the control loop. The system begins the operation of both converters simultaneously. The selection of the operating frequency depends on the availability of the RF power to maximize the harvested DC power and to increase the PCE.

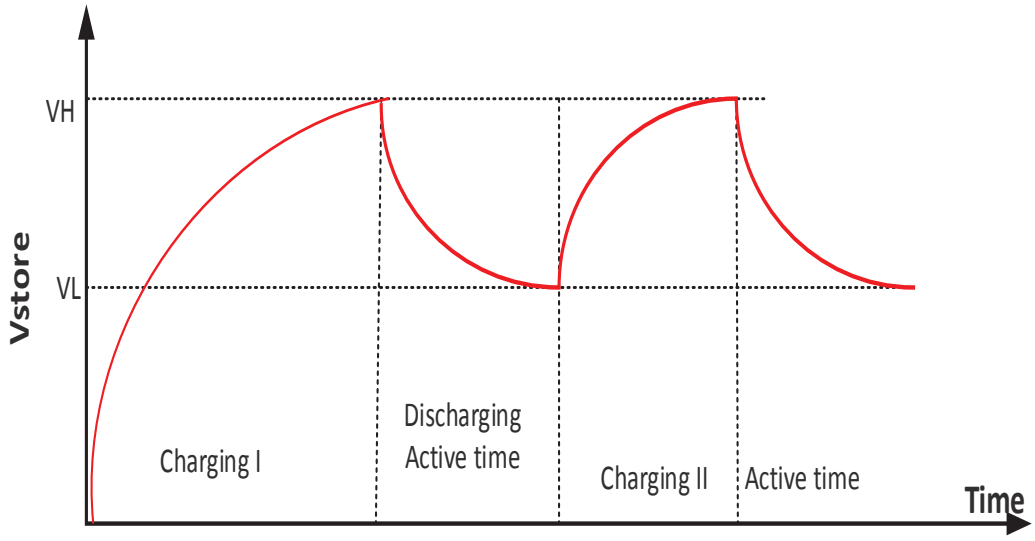


Figure 5.2: The harvester modes of operation in time domain.

5.3 System Level Consideration

Since the harvested power is accumulated at storage capacitors, the harvester has three phases of operations. Fig. 5.2 illustrates the three regions of operation where the output voltage is a function of time. The first region represents the charging phase (Charging I) when there is no initial energy and the two rectifiers' voltages increase with time until they reach a predefined voltage (V_H). In the second region (Discharge), the load currents are drawn and C_{char} and C_{char2} discharge during the active time until they reach a predefined voltage (V_L). The third region represents the second charging phase (Charging II) from the previously accumulated voltage V_L until it reaches V_H again.

The stored energy is proportional to $(V_H - V_L)$ and the size of C_{char} and C_{char2} are shown in (5.2) and (5.3). Using large C_{char} increases the stored energy but it also increases the charging time. Higher $(V_H - V_L)$ increases the stored energy without increasing the charging time. Note, the discharge speed is higher than the charging speed. Also, the active time is dependent on C_{char}, V_H, V_L and the total current drawn by the system (see (5.6)).

Since the target application is the RF powered wireless sensor node, the required energy depends on the DC power consumption of the node and the active operating

Table 5.1: System level specifications for the Triple RF Band Energy Harvester.

Specifications	Target
Harvesting bands (GHz)	0.9, 1.2, 2.4
Output voltage (V)	2.3
Load current (mA)	2
Charging time (ms)	0.2
Main charging capacitor (nF) (C_{char})	200
Active Time (ms)(REC I)	0.12
Auxiliary charging capacitor (nF)(C_{char2})	100
Active Time (ms)(REC II)	0.42

time. The required harvested power is approximately 4 mW with a load current equal to 2 mA. In this work, $V_H = 2.4\ V$ and $V_L = 1\ V$. Table 5.1 summarizes the design specifications.

$$E_{RECI} = \frac{1}{2} C_{char}(V_H^2 - V_L^2) \tag{5.2}$$

$$E_{RECII} = \frac{1}{2} C_{char2}(V_H^2 - V_L^2) \tag{5.3}$$

$$I_{load1} = C_{char} \frac{dv_{rec}}{dt} \tag{5.4}$$

$$I_{load2} = C_{char2} \frac{dv_{rec}}{dt} \tag{5.5}$$

$$T_{active1} = \frac{C_{char}(V_H - V_L)}{I_{load1}} \tag{5.6}$$

$$T_{active2} = \frac{C_{char2}(V_H - V_L)}{I_{load2}} \tag{5.7}$$

5.4 Modeling the Dual Band RF Harvester

Fig. 5.3(a) represents the block diagram of the dual band harvester model where REC I resonates at (ω_1) and REC II resonates at (ω_2) in a way that $\omega_2 = 2.67\ \omega_1$. Each converter is represented by a parallel resistor and capacitor as demonstrated in Fig. 5.3(b). At ω_1, the impedance of REC I $Z_1(\omega_1)$ is purely resistive R_1 and it matches the antenna impedance. For REC II which does not resonate at ω_1 , the impedance is not purely resistive, and does not match the antenna impedance. Similarly, at ω_2, REC I does not resonate at ω_2, the impedance is not resistive and does not match the antenna impedance, while for REC II, the impedance is purely resistive. From Fig. 5.3(c), The impedance of each converter at ω_1, ω_2 are expressed as the following:

$$Z_2(\omega_1) = R_2 - 2.23jQ_2R_2 \tag{5.8}$$

$$Z_1(\omega_2) = R_1 + 2.23jQ_1R_1 \tag{5.9}$$

Our analysis shows that input impedance of each converter Z_1 and Z_2 observed at the non-resonate frequencies (ω_1, ω_2) respectively are a function of the inductor Q-factor [25]. Therefore, a large Q-factor is required to maintain a high impedance at these frequencies.

5.5 The Control Loop Design

Since the amount of harvested power is directly proportional to the available RF power, the control loop is continuously checking the amount of harvested power to track the high RF power. This continuous tracking of the RF power in a wide bandwidth between 900 MHz and 2.4 GHz requires an autonomous and reconfigurable operation. If a low RF power occurred in one band, the harvester automatically switches the operating frequency to the other band. To do so, as explained in the previous sections, a control loop is required.

The control loop includes a two-stages error amplifier that compares the rectifier output voltage with an on-chip reference voltage (V_{ref}) that generates a tuning signal (V_{tune}). This signal is used to switch the harvesting frequency of REC I from 0.9 GHz

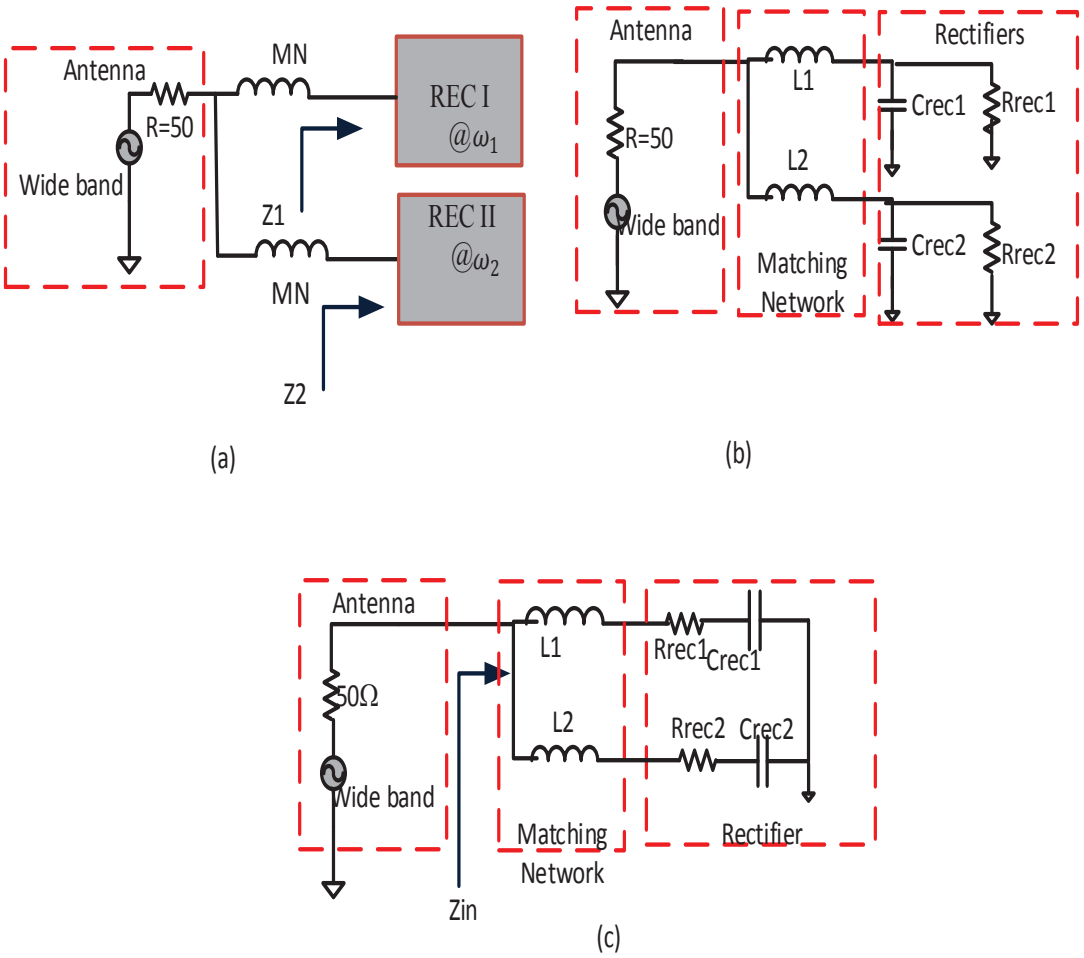


Figure 5.3: The modeling of simultaneous dual band RF harvester (a)the dual harvester (b) the lumped parallel equivalent circuit (c) the lumped series equivalent circuit.

to 1.2 GHz.

The CMOS voltage refrence circuit design shown in Fig. 5.4 is utilized [71]. The voltage refrence V_{ref} provides the control loop with a supply-independent and a temperature-stable voltage of 0.7 V.

A start-up circuit consisting of (M_{S1}, M_{S2} and M_{S3}) injects an initial current into the drain of M_6 once the accumulated voltage in the capacitor C_{char2} reaches 0.6 V. The start-up circuit is used to prevent this self biasing reference generator from a zero current operating point and it turns off as soon as normal operations starts. Table 5.2 presents the MOS dimensions of the refrence generator circuit.

Fig. 5.5 shows the post-layout simulations of the reference circuit, where $\sigma \mathrm{V_{ref}}/\sigma \mathrm{V_{DD}}$ is 31.5 mV/V for a load current equal to 10 μA while it is equal to 55 mV/V for load current equal to 50 μA. Fig. 5.6 illustrates the output voltage when the supply voltage varies between 0 V to 2 V. The reference generator is tested against temperature variation between 0^oC to 100 ^oC.

The circuit design of the error amplifier is shown in Fig. 5.7. It includes a non-inverting two-stage op-amp with an NMOS input stage (M_1, M_2). All the transistors in the op-amp are working in the saturation region except (M5, M7) are in the sub-threshold region to boost gm to improve the gain-bandwidth frequency (GBW) and to push the output pole and zero to a higher frequency.

Table 5.3 shows the devices dimensions in the amplifier circuit. Frequency compensation is achieved by including the capacitance C_c and R_z between M_4 and M_6 where $C_c = 1\ pF$ and $R_z = 0.4\ K\Omega$. The biasing current for the error amplifier is $200\mu A$. Fig. 5.8 illustrates the stability analysis of the negative feedback system performed to ensure enough phase margin. The results implies a DC gain of a 53.5 dB and a unity gain frequency of a 4 MHz. The phase margin is found to be 65^o. The control loop consumes 0.67 mW of the 1.14 mW total storied power in the auxiliary rectifier.

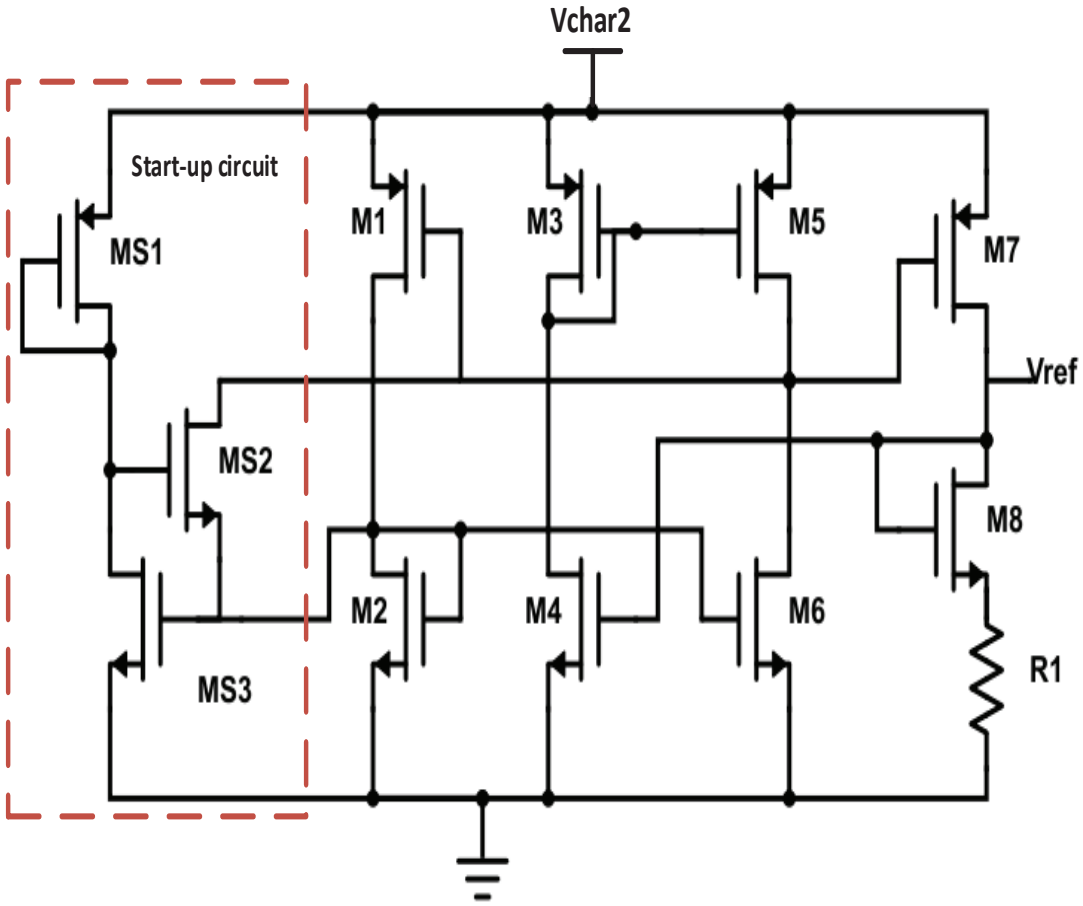


Figure 5.4: The schematic diagram of the self-biasing reference voltage generator.

Table 5.2: The Reference Voltage Circuit Dimension.

Device	width (μm)	length (μm)
MS1	1.2	0.6
MS2	0.6	0.6
MS3	0.6	0.12
M1	6	0.12
M2	0.6	0.12
M3	6	0.12
M4	0.6	0.12
M5	6	0.12
M6	0.6	0.12
M7	6	0.12
M8	2	0.12
R	2.7 $K\Omega$	

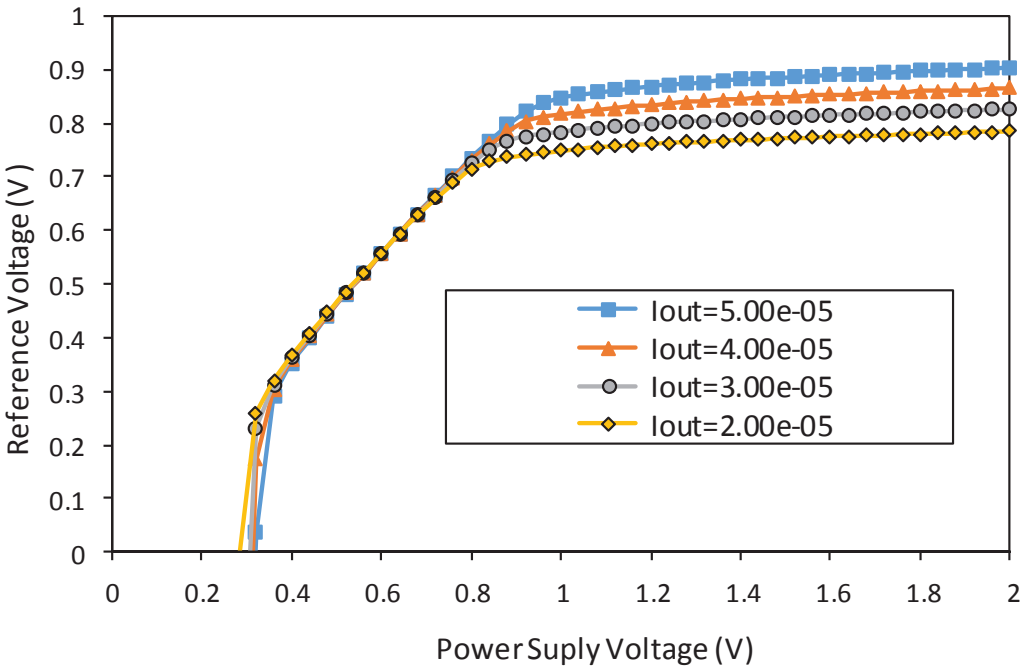


Figure 5.5: The post layout simulation of the reference voltage results verses power supply variation of a load current between $50\mu A - 200\mu A$.

5.6 The Tunable Matching Network

The impedance matching network (MN) between the antenna and the rectifier plays an important rule in the power transfer. To achieve a maximum power transfer, the MN ensures the harvester impedance matches the antenna impedance. Also, the MN can be used to improve the rectifier sensitivity by boosting the input power to a higher level [72] as can be seen in (5.10). This can be done using two high-Q off-chip inductors.

$$V_{rec} = \frac{V_{ant}}{2}\sqrt{1+Q^2} \tag{5.10}$$

Fig. 5.9 illustrates the antenna-rectifier interface modeling of a rectifier that harvests from two RF bands. The dual harvesting frequency is achieved by employing dual shunt varactors (C_{var1} and C_{var2}) at the input of the rectifier to vary the input impedance.

The proposed MN enables the instantaneous and continuous control of the input impedance based on the available input power. The effective input impedance of

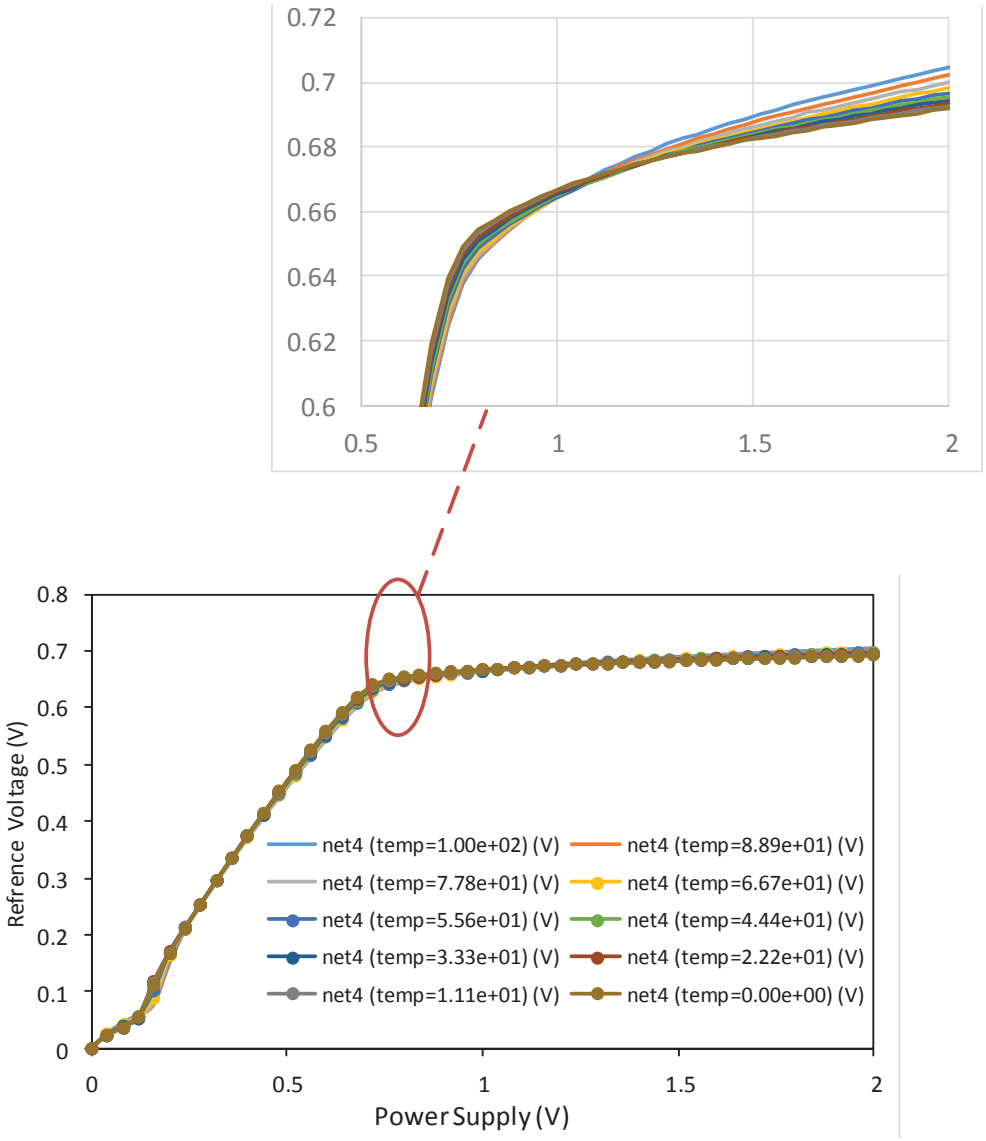


Figure 5.6: The post layout simulations of the reference voltage against the power supply variation over a temperature range of 0^oC to 100 ^oC.

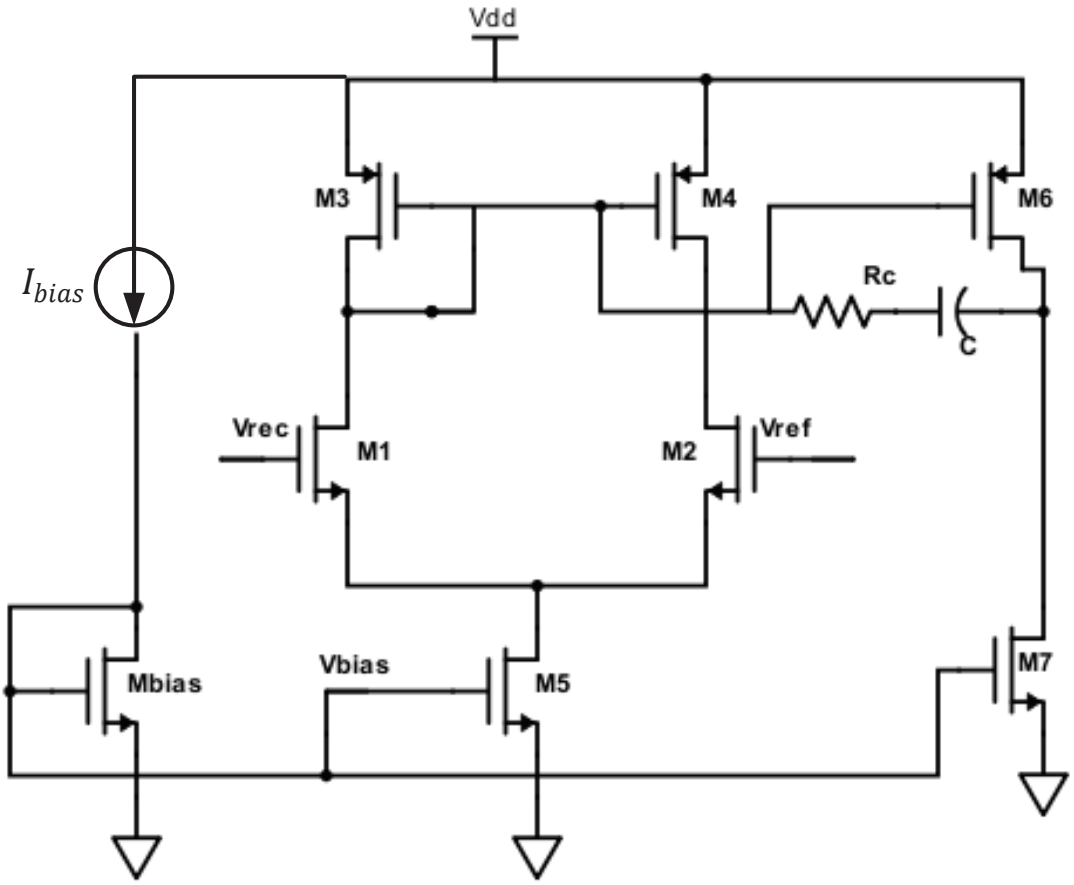


Figure 5.7: The schematic circuit of the error amplifier.

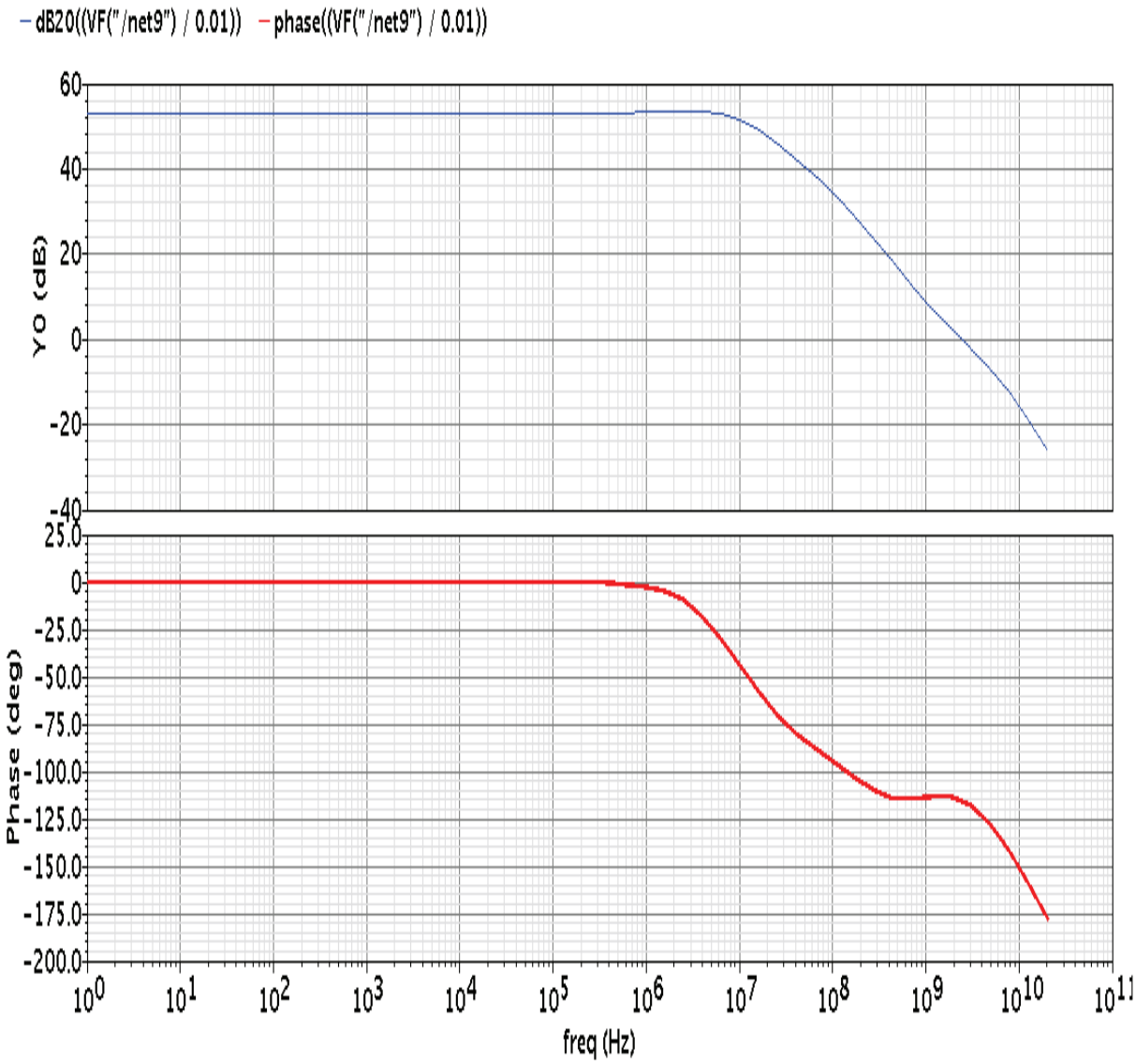


Figure 5.8: The post layout simulations of the stability analysis of the two-stages error amplifier gain magnitude and phase.

Table 5.3: The Error Amplifier Device's Dimensions.

Device	W (μm), L in/(μm)
M1	1, 0.1
M2	1, 0.1
M3	4, 0.1
M4	4, 0.1
M5	4, 0.1
M6	4, 0.1
M7	35, 0.13
Mbias	1, 0.1

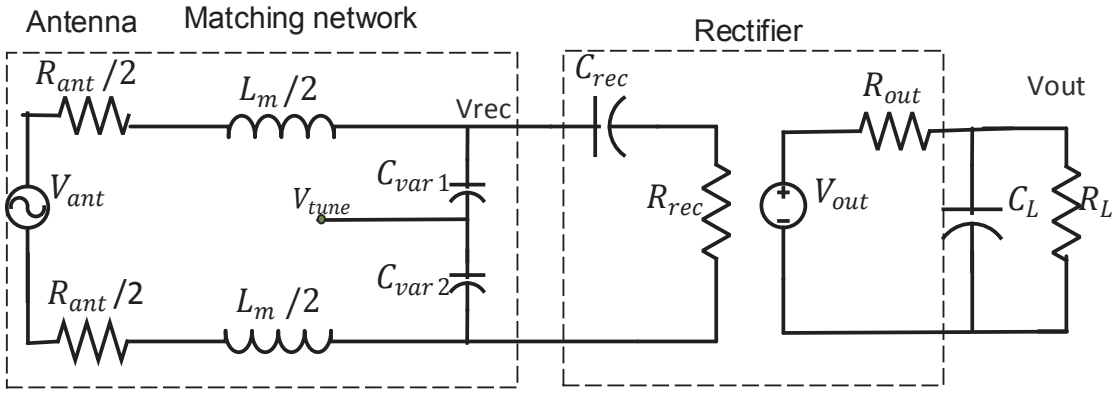


Figure 5.9: The modeling of the antenna-rectifier circuit for a dual frequency harvesting.

REC I varies based on the incoming signal from the controller to track the high RF power. Each converter is designed to resonate at its specific frequency. This has been achieved by allowing the effective input capacitance value to change, such that it varies between a nominal value C_1 and a new controlled value denoted by C_2 to tune the MN to the desired frequency:

$$\omega_1 = \frac{1}{\sqrt{L_m\ C_1}} \tag{5.11}$$

$$\omega_2 = \frac{1}{\sqrt{L_m\ C_2}} \tag{5.12}$$

where C_1 and C_2 are the rectifier effective input impedances at ω_1 and ω_2 respectively.

5.7 The Rectifier Circuit Design

Typically the design requirements of the RF-DC harvester are: efficiency, output DC voltage and sensitivity (which is the minimum voltage to turn-on the CMOS rectifier). The classic Dickson multiplier [73] consists of a cascade of diode-connected MOS transistors. At each node of the diode chain, the RF signal is injected through a pair of coupling capacitors. Through charge sharing, the output voltage of each stage is effectively multiplied with respect to that of its input. The Dickson multiplier suffers from a very poor PCE due to the losses associated with the MOS threshold voltage (V_{th}).

The aspect ratio of the transistor (W/L), the number of stages (N) and the size of the coupling capacitor (C_N) are key design parameters. The simulation results in Fig. 5.10 indicate that the number of cascaded-stages determines the amount of the harvested voltage. C_N is necessary to ensure the AC voltage is added in parallel. These capacitors should be sized carefully to avoid voltage division with the parasitic capacitors and to keep the chip area small.

Increasing the harvested voltage requires either more stages or a larger transistor but in both cases this will increase the associated losses due to the leakage current and to the parasitic capacitances. In general, increasing the dimension of the MOS transistor reduces R_{on}. However, selecting the proper dimension depends on many

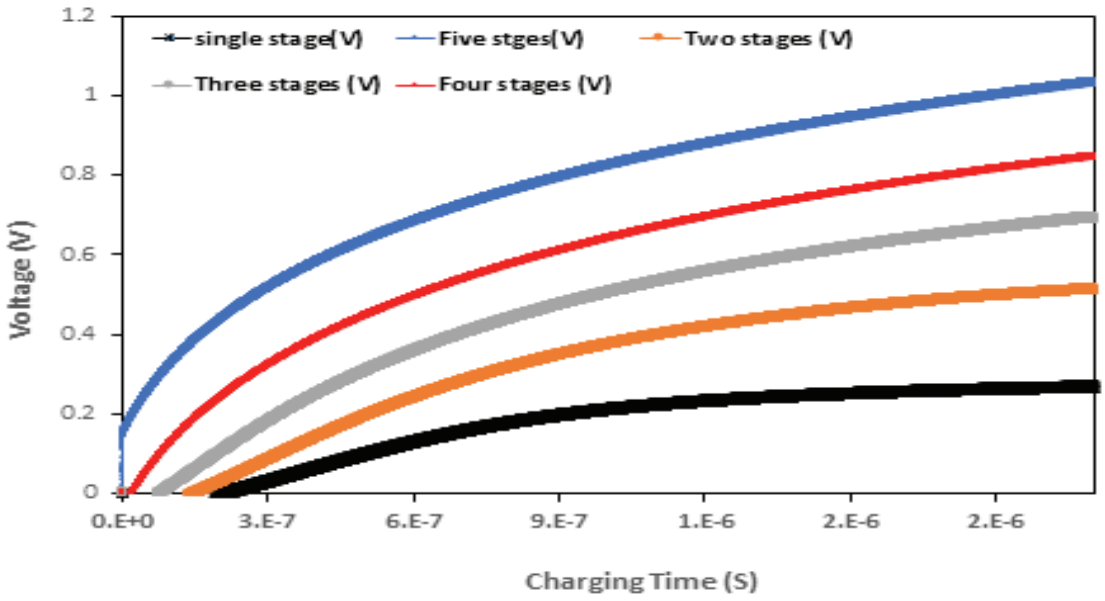


Figure 5.10: The rectifier output voltages for different number of stages at $V_{in} = 70$ mV.

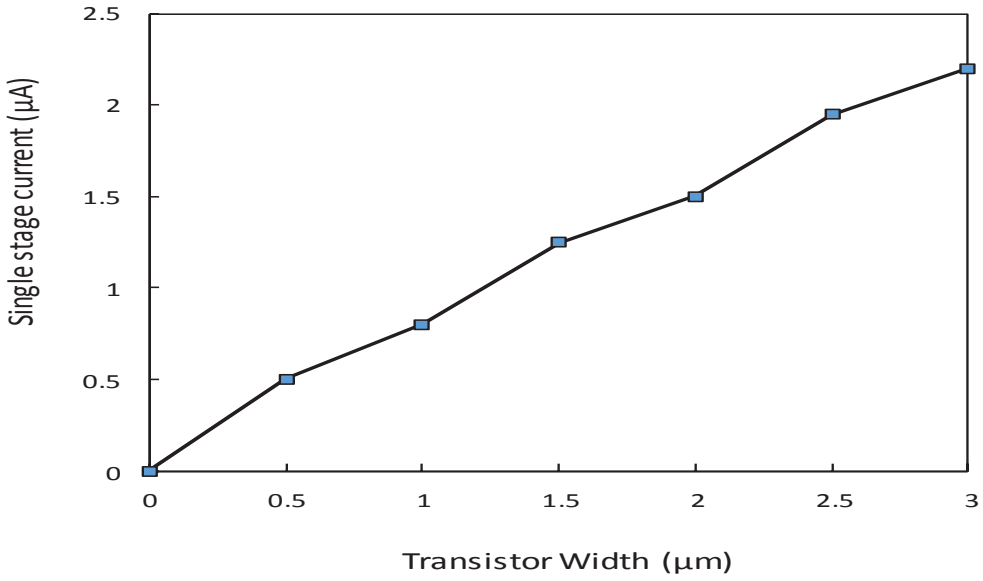


Figure 5.11: The simulation result of harvested current verses transistor width for single stage rectifier .

factors such as the required load current, the charging time and the number of stages. Selecting the proper MOSFET dimension in the rectifier circuit plays an important role in determining the load current (I_{load}).

Figure 5.11 illustrates the relationship between the transistor width and the amount of the harvested current of a single stage rectifier for an input RF power equals to -10 dBm. The result implies that the rectifier output current increases by increasing the width of the transistor. To meet the requirement of a WSN in terms of the load current, the charging time, the efficiency and the output voltage, a four-stages dual band energy harvester is presented in this work and it is boosted by a secondary two stages rectifier to improve the efficiency.

5.8 The Triple RF Harvester Circuit Design

Fig. 5.12 demonstrates the circuit design of the autonomous and reconfigurable triple band energy harvester. REC I and REC II are implemented using the conventional cross-connected differential rectifier [64]. REC I and REC II are comprised of four and two cascaded stages respectively.

The error amplifier compares the output voltage of REC I with V_{ref} and provides V_{tune} signal to switch between the RF frequencies ω_1 and ω_2 instantaneously and autonomously. REC II is resonating at a third RF band. Also, V_{tune} is utilized to boost the input voltage of REC I. This voltage is defined here as V_{boost}.

REC I operates at 900 MHz, when the rectifier output voltage V_{out1} at ω_1 is lower than V_{ref}, V_{tune} signal is enabled and it shifts the resonant frequency of the rectifier to a 1.2 GHz. At ω_2 and when V_{out1} is lower than V_{ref}, V_{tune} is disabled allowing the resonant frequency of the rectifier to go back to ω_1. REC II harvests at ω_3=2.4 GHz. When REC II output voltage V_{out2} reaches 0.6 V, the control loop (including the reference voltage generator and the error amplifier) is activated.

The control loop is activated when the amount of the harvested power at REC II reaches 1.14 mW. The control loop consumes 0.6 mW which is approximately half of the harvested power of REC II. The applied boosting voltage $_{boost}$ is used to compensate for different types of losses including the leakages.

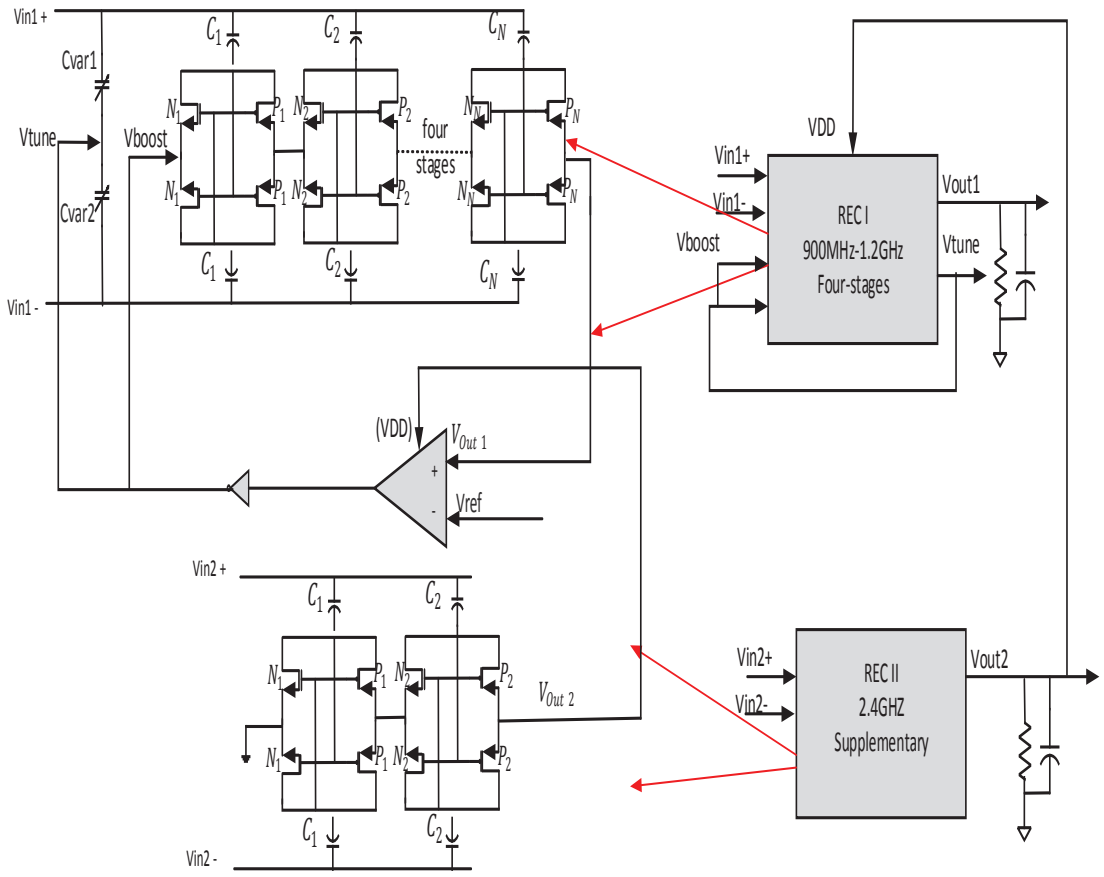


Figure 5.12: The architecture of the triple RF-band harvester with the rectifier implementation using V_{th} cancellation technique.

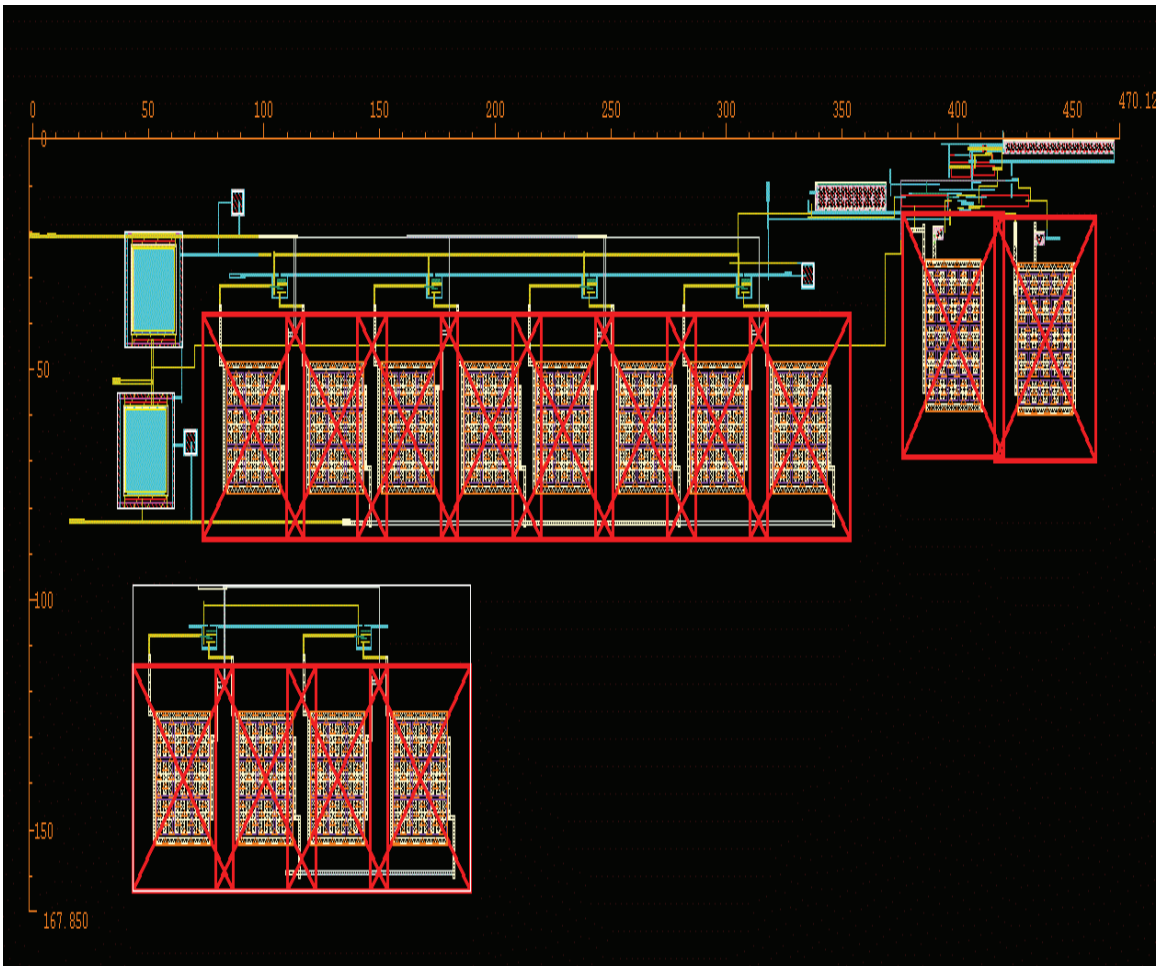


Figure 5.13: Photograph of the the harvester layout.

5.9 The Results and Discussion

The proposed triple-band harvester is designed, simulated and implemented in 65nm CMOS technology. Fig. 5.13 shows the layout of the proposed harvester. It occupies die area of 0.47 mm X 0.167 mm without pads.

Four off-chip 4 nH inductors with a Q equal to 14 are used to match the 50 Ω antenna impedance at the input impedance of the differential rectifier. The initial operating frequency is assumed to be at 900 MHz; when V_{tune} signal is disabled, the 900 MHz is maintained. When V_{tune} signal is enabled, the input impedance of the MN is shifted to 1.2 GHz. Fig. 5.14(a) shows the input impedance of REC I and REC II at 900 MHz, 1.2 GHz and 2.4 GHz respectively.

At the beginning of the harvesting operation, there is no initial energy available to

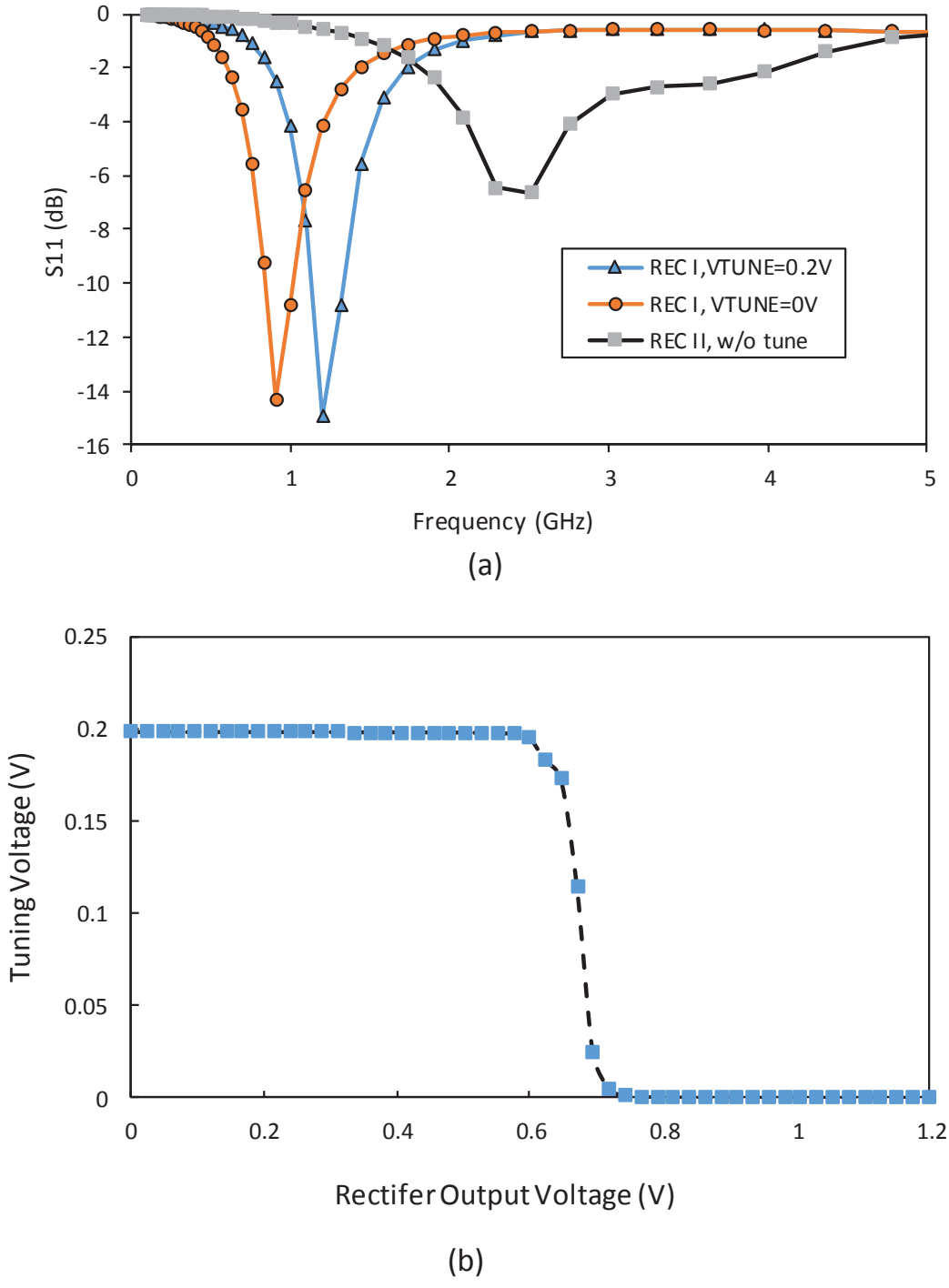


Figure 5.14: The harvester post-layout simulation results (a) input impedance for REC I and REC II(b) the tuning control voltage V_{tune}verse REC I harvested voltage V_{out1}.

activate the control loop. The harvested voltage increases slowly with time, when V_{out2} reaches 600 mV, the control loop is activated. To ensure the continuous operation, the capacitor C_{char2} discharges till $V_L = 1$ V.

Once the control loop is activated it compares the amount of the harvested voltage V_{out1} that is accumulated at C_{char1} with V_{ref}. The error amplifier output signal V_{tune} is enabled when the harvested voltage is smaller than the reference voltage V_{ref} ($V_{out1} < 0.7$ V). The error signal V_{tune} is disabled when the accumulated voltage at C_{char1} is bigger than the refrence voltage V_{ref} ($V_{out} > 0.7$ V) as illustrated in Fig. 5.14(b).

In Fig. 5.15(a), the harvested voltage V_{out1} is higher than V_{ref}. Therefore, the control signal V_{tune} reduces with time until it reaches zero (disabled). Hence, the operating frequency remains at the 900 MHz since the RF power is high in this case.

In Fig. 5.15(b), the harvested voltage V_{out1} is smaller than V_{ref}. The control signal V_{tune} increases with time (enabled) until it reaches 0.2 V. That means the harvesting frequency is switched from 900 MHz to 1.2 GHz because the RF power at the 900 MHz was low.

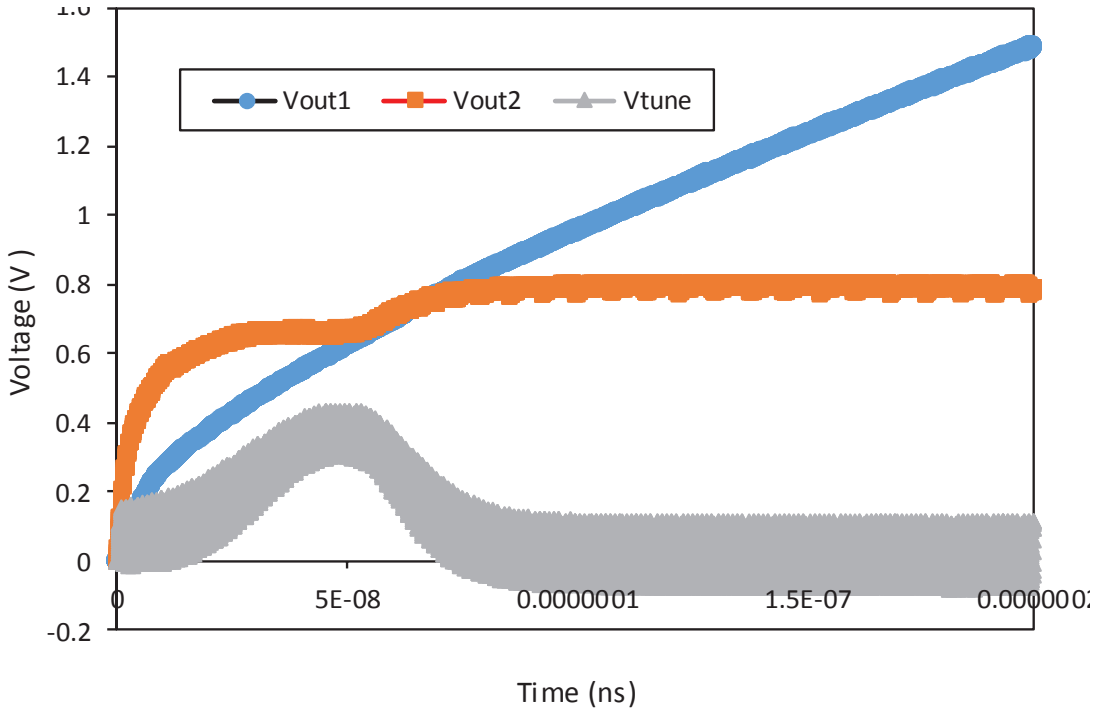
The ripple of the rectified voltage depends on the available input RF voltage. Regarding V_{tune} signal, since the ripple amplitude is around 50 mV these ripples have no affect on the tuned frequency.

As discussed earlier, this work is targeting a very low RF input voltage (amplitude). The amount of the harvested voltages of REC I and REC II are presented in Fig.5.16(a). The control signal V_{tune} is employed to boost the harvested voltage. This harvester is evaluated at the three RF bands for an input voltage varies between 50 mV and 450 mV. The result implies that a 30% and 10% increment in the harvested voltage are achieved when the boosting voltage is applied at 900 MHz and 1.2 GHz .

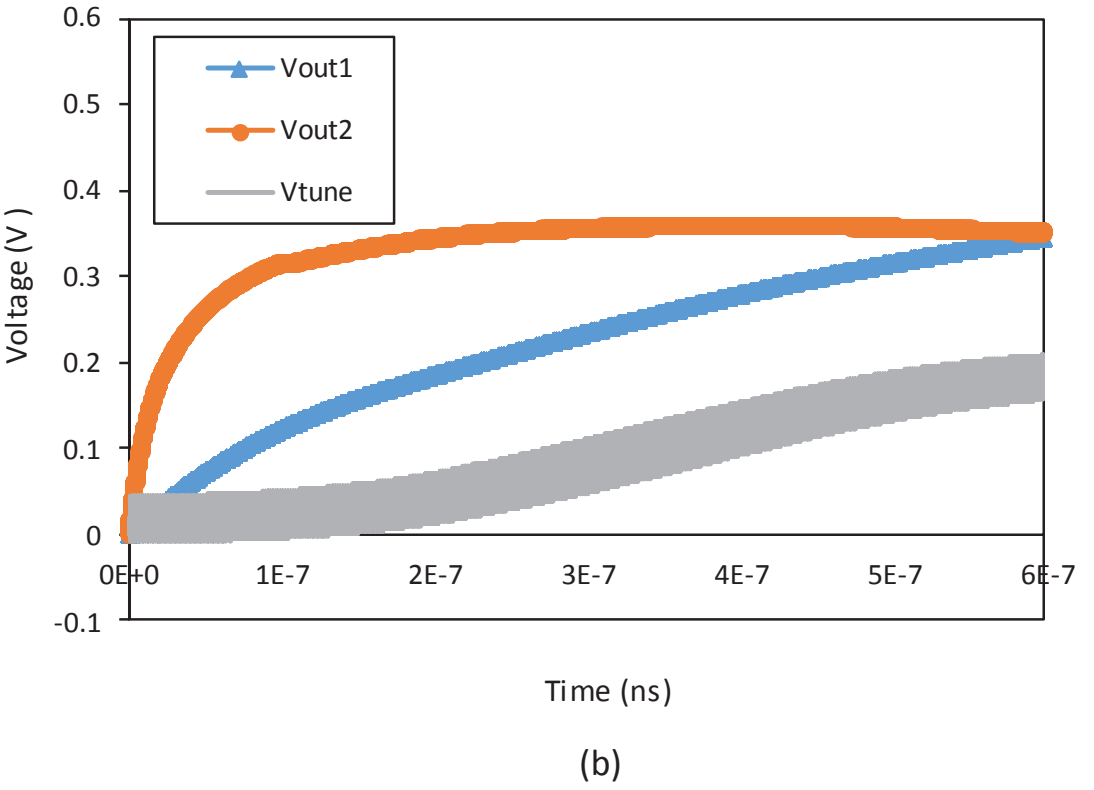
Fig. 5.16(b) shows the harvester PCE results versus the RF input voltage evaluated at the three RF bands with the boosting voltage. The PCE is defined here as the ratio of the DC output power (P_{out}) to the available RF input power (P_{in}).

$$PCE = \frac{V_{out}^2}{R_L P_{in}} \tag{5.13}$$

For an input voltage between 50 mV and 450 mV, the results indicate that the presented harvester maintains a PCE above 30% for a wide input range at 900 MHz



(a)



(b)

Figure 5.15: The harvester post-layout simulation of the output voltages and the control signals in time domain (a) when $V_{in} =$ 200 mV (b) when $V_{in} =$ 50 mV.

and 2.4 GHz and above 20% at 1.2 GHz. The results imply that the peak PCE increased from 38% to 43% at 900 MHz and it increased from 27% to 33% at 1.2 GHz when the boosting voltage was added. For REC II, the rectifier has a peak PCE of 57% at 2.4 GHz. Note, REC II has higher efficiency because the tuning matching network in REC I has created a voltage division.

Table 5.4 summarizes the performance of the proposed harvester and compares it with recently published works. Among the many comparison parameters shown in Table 5.4, the reconfiguration and the autonomous RF tracking are the important factors. The proposed solution harvests from three RF bands 900 MHz, 1.2 GHz and 2.4 GHz and utilizes only two rectifiers while in [70], [66], [69] two rectifiers are used to target two frequencies. Moreover, a high PCE is achieved compared to other state of the art works. It is important to mention here, the minimum startup power is not important in this design because whenever the harvested power is less than 0.7 V, the harvester switches the operating frequency.

5.10 Summary

An autonomous energy harvester capable of performing a high RF power tracking is presented. The proposed system is based on the RF harvesting approach from three bands. The circuit includes a reconfigurable dual multi-stage rectifier and a control loop. The harvester has the potential of being deployed with a remote sensor node to enhance the node's operational life-time. A peak PCE of 57%, 43% and 33% are achieved at 2.4 GHz, 900 MHz and 1.2 GHz. A 30% and 10% increment in the harvested voltage are achieved due to the boosting voltage addition at 900 MHz and 1.2 GHz.

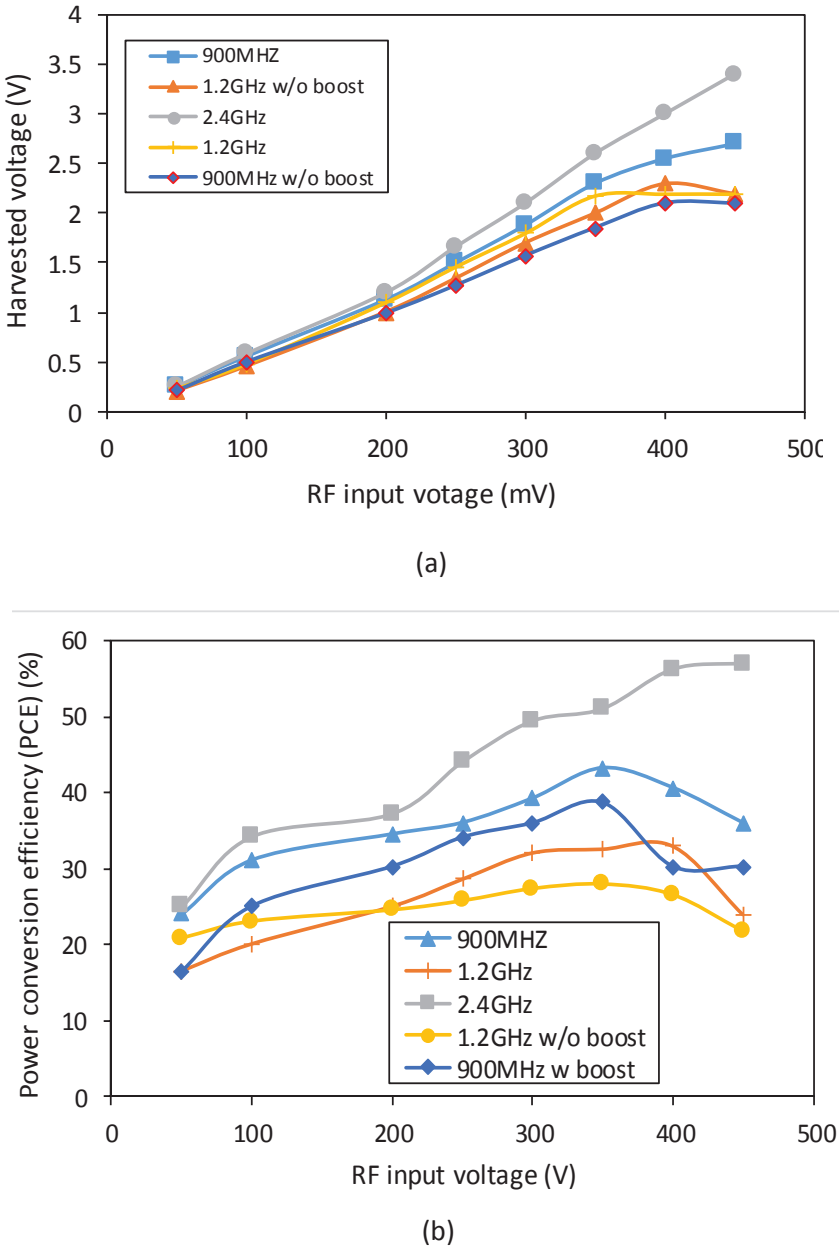


Figure 5.16: The post-layout simulations of the triple RF band harvester characterized at the three RF bands at 10 KΩ load, (a) the output voltages (b) the power conversion efficiencies.

Table 5.4: Performance and Comparison with Prior State-of-the-Art RF Harvesters.

Specification	This work	[69]	[70]	[66]	[19]	[74]
Number of harvesting bands	3	2	2	2	1	1
Reconfiguration and autonomous RF-bands tracking	yes	NO	NO	NO	NO	NO
Efficiency PCE(%)	57, 43, 33	11, 14	45, 56	55, 64	36.8	11
Minimum startup RF power(dBm)	-16	-19.3	-10,-15	-9.6	-18.4	-18
Output voltage (V)	1, 2.4	1, 1.1	0.9, 1	1	1.2	1.2
Rectifier stages	4, 2	4	2	3	5	17
CMOS Technology	65nm	$0.13\mu m$	N/A	$0.13\mu m$	40nm	90nm

Chapter 6

The Conclusion

6.1 Conclusion

In this research, a 2.4 GHz QPSK transmitter is designed and implemented in TSMC 65 nm CMOS technology under a 0.4 V power supply. Our research demonstrated a solution that is significantly more energy efficient. Such a transmitter is highly demanded to realize the communication front-end of the biomedical WSN.

This research presented two types of a class-E power oscillator circuit design. This included a design methodology, an analysis and the mathematical equations. The first type was part of a QPSK transmitter fully integrated and tested. This power oscillator was represented in Chapter 4 which utilized a class-D pre-amplifier in a positive feedback configuration and three on-chip inductors with wide tuning ranges. The second power oscillator was presented in Chapter 3 which used an inverter as a pre-amplifier in positive feedback configuration with two inductors on-chip and lower power consumption and smaller tunning ranges This oscillator was intended for more area efficient design to reduce the fabrication cost. It was intended to fabricate a second chip including the RF powered transmitter, but this was not possible due to funding restrictions.

Our novel class-E transmitter employed a class-E power oscillator for the direct modulation. This prototype optimized the power consumption and the output power to achieve a good efficiency and a high data rate.

A novel technique for the PM was presented with a detailed analysis and the mathematical equations. The presented PM technique improved the power consumption, the data rate, the efficiency and the energy/bit FOM. The new PM techniques enabled us to develop an energy efficient transmitter. The required $90^o, 180^o$ and 270^o phase shifts were achieved without the need for an additional circuit. The PM pulse generator was designed and implemented according to the developed mathematical equations of the proposed PSK modulation scheme.

The transmitter was designed and implemented using TSMC 65 nm CMOS technology. The measurement indicated a 2.9 mW power consumption while achieving a 69 Mbps data rate and an energy/bit FOM of a 42 pJ/bit.

An autonomous energy harvester was introduced in Chapter.5. It performed a high RF power tracking to maximize the harvested DC power and enhance the efficiency. This simultaneous triple RF band energy harvesting system has the potential of being deployed along with remote sensor nodes to enhance their operational life-times.

The harvester included two multi-stage rectifiers that harvested from three RF bands: 900 MHz, 1.2 GHz and 2.4 GHz. A control loop was implemented to reconfigure the harvesting frequency of the main rectifier based on the amount of available input power. The results showed a peak harvesting efficiency of 57%, 43% and 33% at 2.4 GHz, 900 MHz and 1.2 GHz respectively.

Finally its worth mention here that implementing and optimizing the RF integrated circuits in the layout level is an important, challenging and time consuming engineering task. Also, it was a lengthy process to optimize and to improve the test-setup for reducing its effect on the performance of the fabricated prototype circuit.

6.2 Recommendations for Future Work

Some improvements of the presented class-E transmitter and the triple band energy harvester for a battery-less operation are listed below as a future work.

- In the implementation of our novel power oscillators presented in Chapter 3 and Chapter 4, the compensation for any frequency deviation due to PVT variations is done using analog control voltage. This solution might not be feasible for applications requiring a high accuracy or an autonomous operation. In this case, more elaborate frequency compensation can be explored for better performance.

- As a next prototype, it is recommended to integrate on-chip the refrence frequency used in injection locking in order to be fully integrated. Since the autonomous compensation for any frequency deviation is very beneficial, one way of doing this is by taking advantage of the on-chip refrence clock.

- Our novel class-E power oscillators (including the two designs presented in Chapter 3 and 4 show promising results in terms of reducing the power consumption and the power efficiency, therefore exploring the differential architecture can be a good alternative direction.

- The autonomous triple band RF harvester is designed, implemented and verified however, it still requires a highly efficient power management unit.

- Although an energy efficient transmitter is developed in this dissertation, a WSN transceiver that can be implemented by combining this transmitter with a receiver is still required for WSN. One possible future work includes the investigation of the fundamental limitations for the energy-efficient WSN transceivers.

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