Low-Voltage and Low-Power Analog Integrated Filters implementing Current-mode Bulk-Driven Differentiators

By

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Dedicated to my Parents, Brother, Friends and Well wishers

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ABSTRACT

This work introduces a CTCM Gate-driven (GD) and Bulk-driven (BD) differentiators using the TSMC 65 nm CMOS technology as an alternative to existing integrator circuits. This CM differentiator exhibits higher stability and lower flicker noise than the voltage-mode integrator. Bilinear as well as biquadratic building blocks based on these differentiators have been introduced. These basic building blocks are then used to implement higher order filters using the GD and BD Techniques. A 6th order cascade CTCM Chebyshev band pass filter using the Gate- Driven and Bulk-Driven techniques has been designed. This design is simulated with a very low supply voltage of 0.7 V with the filter characteristics of 1dB pass band ripple and 2MHz bandwidth. The total power consumption of the designed sixth-order BD CTCM Chebyshev band pass filter is 1.45 mW which is very low in analog IC filter design. The proposed design can be realized for wireless baseband applications where LVLP is an important factor.

LIST OF ABBREVIATIONS USED

CMOS	Complementary-Metal-Oxide-Semiconductor
JFET	Junction Field Effect Transistor
IC	Integrated Circuit
LVLP	Low-Voltage Low-Power
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
BD MOS	Bulk-Driven Metal-Oxide-Semiconductor
GD MOS	Gate-Driven Metal-Oxide-Semiconductor
CTCM	Continuous-Time Current-Mode
OP-AMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
KCL	Kirchhoff's Current Law
ADC	Analog to Digital Convertor
PSRR	Power Supply Rejection Ratio
MLF	Multiple Loop Feedback

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CHAPTER 1 INTRODUCTION

1.1 Motivation

There has been a rapid growth in the use of portable wireless communication devices, hearing aids and consumer electronics in the recent years. This trend thereby produced an ever-increasing need for the development in low-power (LP) and low-voltage (LV) integrated circuits. Low power consumption will allow the devices to work for longer time. This increasing demand for the portability of electronic devices led to the modification of their components which further caused a demand in the need of LP and LV circuit design. The three major factors that are the primary drivers for the expansion of the LP and LV design are [1], [2]:

1. Rapid scaling down of the CMOS technology: The channel length of the MOS transistor is scaled down to sub-micron level and the gate oxide thickness drives into the nanometer level. As a result, the supply voltage is adjusted to maintain the device function and reliability. The circuits that are being commercially developed the supply voltages are reduced from 3 V to 1 V and are even reduced to mere 0.7 V in some instances.
2. Reducing the chip size: As the silicon chip can only dissipate limited power per unit area, a considerable reduction in the power consumption of each and every component should be achieved to accommodate more number of electronic functions and at the same time preventing overheating.
3. Longevity of a circuit: Battery size is often reduced for light weight devices. For small battery, it should work for reasonably long time. In order for a circuit to operate for a longer time with a reduction in the battery size, the power dissipation and the voltage of the design should be kept as low as possible.

Several techniques currently exist for achieving LV and LP in analog circuit designs. However, only few techniques are relevant to current-mode circuits: weak inversion

MOST's operating in sub-threshold regions [5], [6], floating gate approach [9], level-shifter techniques [3], [4], self-cascode structures [7], [8] and bulk-driven transistors [10], [11], [12], [13].

1.1.1 Weak Inversion MOST's in sub-threshold region

In this approach the transistor is maintained in sub-threshold region [5], [6] when the channel is weakly inverted. In the sub-threshold region, the voltage at the gate-source would decrease lesser when compared to the threshold voltage of a given transistor. This approach often results in producing high voltage swings for very low supply voltages serving the purpose. However, weak inversion region will not work for high frequency and high slew rate applications which require a stronger inversion region.

1.1.2 Floating-Gate Approach

Floating-gate devices [9] are available in the standard CMOS technology as they are widely used in digital circuits. They are also becoming popular in analog circuits as well due to their functionalities and are being used as memory arrays as well as in circuit blocks. Although, they can be operated with very low supply voltage, it is often difficult to store charge for the device due to the direct-tunneling and induced leakage current in deep sub-micron process.

1.1.3 Level-Shifter Techniques

Another technique that can produce high output swing for optimal supply voltages is level-shifter technique [3]. In this process, the given voltage signal is shifted from one level to other. It can minimize the delays and can increase the response time of the circuit. However, this technique involves the use of large number of transistors which in-turn increases the power consumption.

1.1.4 Self-Cascode Structures

Self-cascode structures [7] are more popular in the analog world for providing high output impedance of current mirrors which boosts the gain of the circuit. As the output impedance of the circuit increases output voltage swing reduces at the same time.

1.1.5 Bulk-Driven Technique

It is one of the most popular LV design techniques [10], [11], [12, [13]. The MOS transistor has four terminals where bulk is generally connected to V_{DD}. In this technique, the bulk terminal is used as a signal input and the gate terminal is connected to the limited reference voltage that will be able to turn on the transistor. The transistor thereby achieves the depletion characteristics of which are close to that of the JFET devices.

The best solution for the LVLP problems is Bulk-driven technique while other techniques have the obvious shortcomings. Bulk-driven technique is one of the most popular design which can provide a very good trade-off conditions for most low supply voltage applications.

1.2 Bulk-driven Technology and Its Applications

To trigger the bulk-driven technique, the gate terminal should be biased with a reference voltage which is sufficient to form an inversion layer. For instance, a $V_{GS} > V_T$ is needed for a NMOS transistor. Due to the potential difference between the drain and source, the inversion layer will serve the purpose of a conduction channel. The depletion layer associated with the conduction channel is affected by the change in the bulk voltage. This minute change in the bulk voltage of MOS transistor will affect the drain current and therefore the biasing conditions.

A good functioning BD MOSFET is a depletion type device, which can work in negative, zero and also partially in the positively biased voltage region at bulk terminal. This type of functioning results in the solution for the threshold voltage limitation problem. This technique can also boost the circuit signal swing to a larger extent, which cannot be realized by a gate-driven technique at lower supply voltages.

The drain-source current I_D of NMOS transistor in saturation region can be expressed as:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \qquad (1)$$

Where

μ_n is the mobility of electrons,

C_{ox} is the gate oxide capacitance per unit area,

W/L is the aspect ratio of transistor,

λ is the channel-length modulation parameter,

V_{GS} is the gate to source voltage,

V_{DS} is the drain to source voltage,

V_{th} is the threshold voltage,

And

$$V_{th} = V_{tho} + \gamma(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}) \qquad (2)$$

Where

γ is body-effect coefficient,

V_{tho} is threshold voltage at zero bulk-source voltage

Φ_f is the fermi potential.

A bulk-driven NMOS transistor test circuit is shown in the Figure 1, as an example to better understand its characteristics. From this test bench circuit of transistor, the ability of V_{BS} and V_{GS} to control the channel conductivity i.e. the variations in drain current can be analyzed. A 2.6um/130nm transistor with power supply of 0.7 V is simulated. For the gate-driven mode, the V_{BS} is connected to the source terminal and the input signal is supplied to gate terminal to form the conduction channel. For bulk-driven mode, V_{GS} is biased to a point where it can run the transistor into the saturation region and input signal is connected to the bulk terminal with the supply voltage V_{BS}. From the simulation output in the Figure 2, it can be seen that BDMOSFET can produce depletion characteristics that allows negative, zero and positive bias voltages, while the GD configuration required reaching the threshold voltage to produce drain current I_D. Hence, it is a clear indication that the BDMOSFET achieves higher signal swing which is a major advantage for the scaling of CMOS technologies.

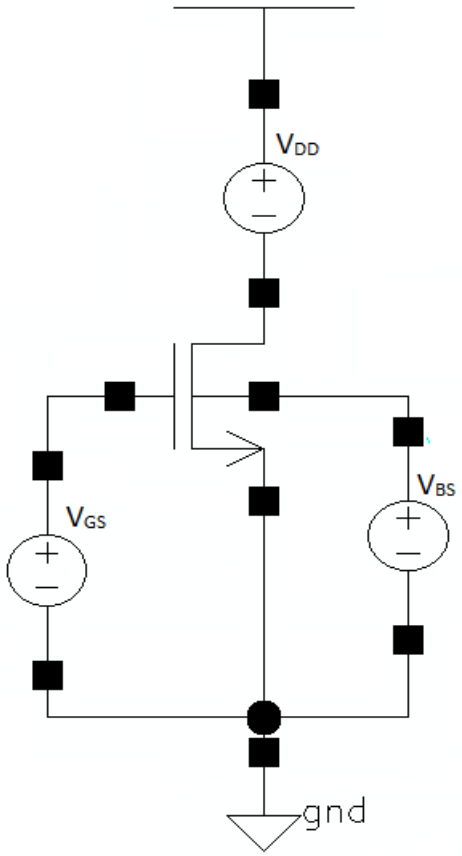

Figure 1 Comparing ID of BD and GD NMOS Simulation Configuration

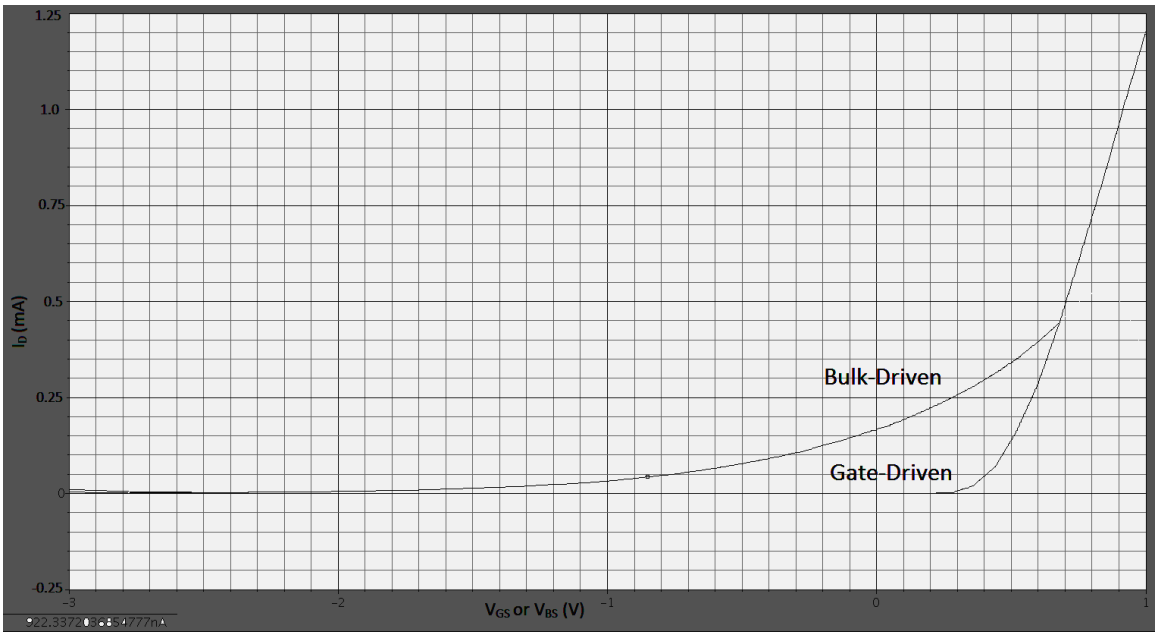

Figure 2 Drain Current (I_D) Characteristics for Variation in V_{BS} or V_{GS}

1.3 Challenges in scaling CMOS technology

The scaling CMOS technology is a successful technology that was introduced by Denard et al. in 1972 [14]. IC circuit designs took a new leap in advancing the low power electronic devices through this technology. With the rapid growth of technology in semiconductor industries, more and more number of transistors was able to integrate in a single IC chip every year. As per the predictions, the scaling CMOS technology will hit the all-time low of 22nm approximately by the end of next decade [15]. Therefore, there is a need for the innovative circuit design techniques that can accommodate challenges in scaling CMOS technology. The designs should focus on the major advantages such reducing the leakage current, low power consumption etc. The major challenges that exist in the scaling CMOS technology are physical, material, power-thermal and technological.

Physical challenges correspond to the increase of tunneling and leakage currents as the devices are being made smaller to fit for the IC chip. In general for a transistor, it has a length L, oxide thickness t_{ox}, bias voltage V and substrate doping N_a. when the scaling parameters are applied, these factors are scaled by the same factor S. The channel length, oxide thickness and bias voltage is reduced by 'S' and the substrate doping is increased by the factor 'S'. Due to the reduction of length, oxide thickness, threshold voltage the leakage current in sub-micron devices increases considerably. These leakage currents are of various types: PN junction reverse-bias current, Sub-threshold leakage current, Gate oxide tunneling current, Injection of hot carriers, Gate-induced drain leakage and Punch-through leakage current [16], [17]. Leakage currents can further be made negligible by both process variations and novel circuit design techniques.

Material challenges evolve due to defects in the materials that cannot provide perfect insulation and conduction for the channel with respect to scaling CMOS technology. To overcome the physical challenges such as leakage currents, high-k materials are introduced to replace the silicon SiO_2 as gate dielectric [18]. These high-k materials are used to reduce the leakage currents as the dielectric material is often very thin in these

materials. But these materials cannot satisfy the requirement of smaller CMOS devices. A trade-off solution should be proposed to mitigate these challenges.

Power challenges are major considerations in a day to day world. These are due to the increased number of transistors embedded per unit area in the integrated circuit (IC) chips which tend to increase the power consumption and also lead to power loss due to excessive heating. When the supply voltage is high for any given circuit specifications in the integrated chips, the power density dissipation tends to grow. At a point, the power dissipation becomes equal to the energy loss due to heating making the circuit unreliable if used for a long periods of time. There are two types of power dissipations: static and dynamic. Dynamic power is due to the transistor switching on and off whereas static power dissipation is due to leakage currents in the circuit. Due to these factors, the circuit performance and reliability of devices are greatly affected.

Technological challenges originate from the manufacturing technologies of the integrated circuit chips. The transistors are fabricated using lithography and masks on integrated circuit boards. These processes are not able to cope with the scaling CMOS devices due to their Nano sizes. The current optical-based fabrication technology cannot produce the resolution that is needed for smaller CMOS sizes. As a solution, a Nano imprint lithography technology is proposed [19] but has not been implemented in production and is still under prototype development.

Even though there are methods available for the entire problem mentioned above, the cost of the products will see the record high which will not be economical. Due to this a trade-off solution should be provided by designing the circuits depending on the applications and the major results required.

1.4 Thesis Contribution

1.4.1 Design of a novel current mode circuit that operates at a Low Supply Voltage

The existing analog filter designs using voltage-integrators demand a supply voltage of 1 V or higher to turn on the transistors. Reducing the supply voltage affects the functioning of the circuit providing an inadequate response. Current-mode BD differentiator based analog filter design can function with the supply voltage as low as 0.7 V. As the proposed design consists of lesser number of transistors, a supply voltage of 0.7 V can potentially turn on all the transistors.

1.4.2 Reduction in Power Consumption compared to Conventional Circuits

The low supply voltage is the key factor for the power consumption of the circuit. As the supply voltage is minimum, the static power consumption of the circuit tends to be very low. The proposed BD differentiator operates with the mentioned low supply voltage and the power consumption is less compared to the existing designs.

1.5 Thesis Organization

This thesis is organized as follows:

Chapter 2 briefly describes continuous-time current-mode (CTCM) circuits and their s-domain transfer function along with the operation of different current-mode integrator circuits.

Chapter 3 provides the design and detailed operation of GD CTCM differentiator and BD CTCM differentiator with simulation results obtained from Cadence TSMC 65nm CMOS technology and performance parameters are tabulated.

Chapter 4 presents the second and sixth order filter design based on GD differentiator and BD differentiator and the realization factors for the Chebyshev band pass filter and the simulation results including performance comparison table.

Chapter 5 provides the details of various analyses required and the sensitivity results for different techniques presented in chapter 4 using Monte Carlo analysis.

Chapter 6 discusses conclusions about the BD differentiator and the filter design approach designed in this thesis and comparison with other existing current-mode filters. Few suggestions for future work are discussed.

CHAPTER 2 CURRENT-MODE FILTER DESIGN

2.1 Current-Mode Circuits

As discussed in chapter 1, the rapid scaling down in the CMOS technology is reducing the transistor sizes to accommodate developing technologies. The scale-down of device sizes thereby demands an aggressive reduction in supply voltages. The best possible solution to accommodate this situation is to design circuits in current-mode (CM) rather than voltage mode (VM) due to their simplicity, reliability and very efficient power considerations. However, current-mode can be referred as a system that uses a current transfer function i.e. the ratio of output current to input current. One of the most simple and highly efficient designs used in current-mode are through the implementation of current mirrors. A current mirror is an inverting amplifier that reverses the direction of input current. It operates at zero input resistance and infinite output resistance. The input is applied to the drain of M_1 (Figure 3) and it mirrors the current to the branch M_2 with an amplification factor '-A' [20].

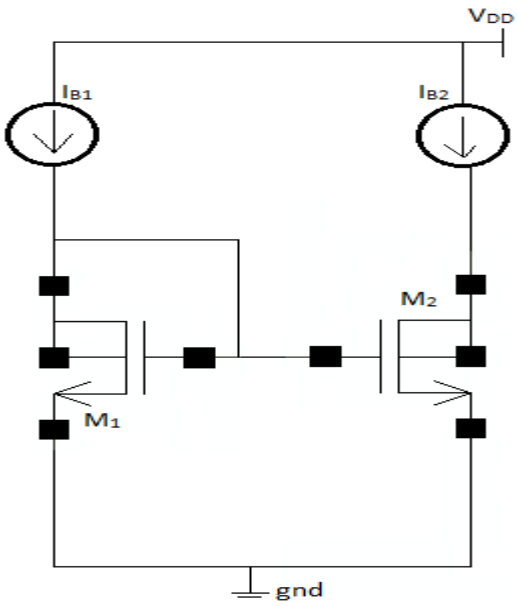

Figure 3 A simple Current Mirror

The transfer function of the current mirror circuit is

$$\frac{I_{out}}{I_{in}} = -A \qquad (2.1)$$

2.2 Voltage Mode Verses Current Mode

In the circuits designed in voltage-mode, voltage is considered as a process variable to define the circuit. Current-mode design [21] is the processing of current signals in an environment where the circuit performance is minimally affected with the voltage fluctuations. Current-mode design uses the current form for input and output rather than voltage as in the case of voltage mode design. The current mode design is preferred over voltage mode due to various advantages such as operation at low supply voltage, low power consumption, high slew rate, improved accuracy and high dynamic range and linearity. In voltage mode, complex circuits are often used to implement mathematical operations such as addition, subtraction and multiplication etc. whereas in current-mode, simpler current mirrors that are simple to build and operate can be used to achieve any mathematical operation with minute changes. In an attempt to better demonstrate the difference between current mode and voltage mode circuits, the cascode design of transistors in both the modes is used as an example as shown in the Figure 4.

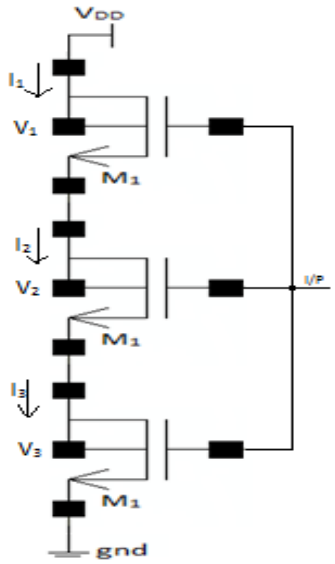

Figure 4 Cascode CMOS Transistor Structure

In voltage mode, voltage drop of (V_1+V_2+V_3) occurs across all transistors which makes the circuit critical to operate at low supply voltages. While in current mode, as current is the operating parameter, no losses occur during operation thereby allowing the whole circuit to operate at lower supply voltages.

Current mirrors [22] are widely used for developing current mode circuits and are simpler to build and can also be used for the realization of many mathematical operations such as addition, subtraction and multiplication etc. Also, precision tuned current-mode circuits can reach higher frequencies than their voltage-mode counterparts as the parasitic capacitance of their transistors does not affect the current signal appreciably. Current mode systems operate with lesser power and at the same time with higher speeds as small voltage swings could produce large current swing due to the characteristics of the MOS transistor. Also, conventional voltage mode circuits consists operational amplifiers primarily, while the major building blocks of current-mode circuits are current mirrors, thereby substantially reducing stability problems and at the same time can potentially be used for the development of components smaller in size.

2.3 Advantages of Current-Mode (CM) Circuits

There are several advantages in current-mode approach [22], [23], [24] and [29] compared to voltage-mode. The major advantages are:

Operating with Low Voltages: The circuit design in current-mode approach needs very low voltages for satisfactory operation unlike designs in voltage-mode. Mostly, current-mode circuits require within 1 V additionally could further be reduced to 0.7 V through the use of bulk-driven technique.

Lower Power Consumption: In this approach, a small voltage swing in the supply voltage can produce large current swings. And thus, this current swing can be able to operate the circuit satisfactorily with very less power consumption.

Higher Dynamic Range: Dynamic range is described as the maximum to minimum signal ratio which the circuit can perform. This ratio majorly depends on the voltage noise and current noise in the signals provided to the circuit. As the noise ratio is much lesser in current mode circuits compared to voltage mode, then a higher dynamic range can be achieved in the current mode designs. The expression of dynamic range can be expressed as:

$$DR = 20\log\left(\frac{I_{out}}{I_{in}}\right) \qquad (2.2)$$

High Bandwidth: Bandwidth and center frequency of the circuit are primarily controlled by the change in the capacitor values. In general, active circuits are affected by stray capacitances such as junction capacitances. This effect will limit the bandwidth in voltage-mode circuits whereas in current mode the effect of stray capacitances is very minimal providing flexible bandwidth considerations.

Simple Mathematical operations: It is very much easy to perform mathematical operations such as addition, subtraction and multiplication in current-mode approach comparing to voltage-mode. For instance, addition in voltage-mode is performed either

with active devices such as op-amps, resistors or with passive devices like inductors. These operations with active components in voltage mode require more than one power supply. These usages of additional inputs require more components to perform the operation and thereby increase the physical size of the circuit and higher power consumption as well. According to Kirchhoff's current law, desired mathematical operations can be achieved through minor changes in the current mirror building block shown in Figure 3. For example, a current adder [22] could be designed by using this basic building block as shown in Figure 5.

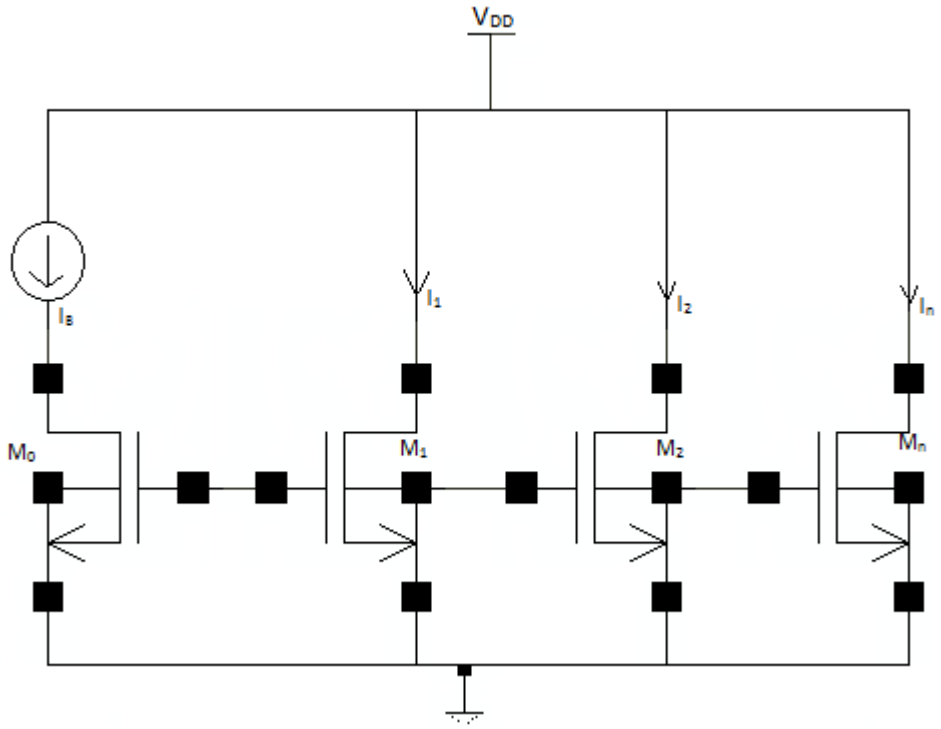

Figure 5 Simple Current Adder

As shown in Figure 5, current mirrors can be used as single or multi input and output current adders. Assuming all the transistors to be identical (i.e. identical W/L ratios), the total output current becomes

$$I_{out} = I_B + I_i \qquad (2.3)$$

Where, $I_i = I_1 + I_2 + \cdots + I_n$

2.4 Current-Mode Approach Applications

Current-mode approach in analog signal processing has been developing very rapidly due to its ability to provide elegant and simple solutions to circuit problems at LV and LP. There are many applications that can be designed in current-mode approach [25], [26], [27], [28]: A/D and D/A converters, analog IC filters, sampled data filters, wireless transmitters and receivers in mobiles, magnetic disk drive read channel IC's, RF circuits, neural networks, optical systems, DC to DC convertors etc. As described in the section earlier, current-mode approach has several advantages thereby making the circuits designed in current mode accommodate the demands in the field. In this thesis, our aim is to design continuous-time current-mode filters with the best possible methods and some of the available procedures are also discussed in this chapter.

Integrator or differentiators are used as major building blocks in the design of continuous time filters. Integrators or differentiators are used to design higher order filters depending up on the specifications and the application in which they are being used. A brief description for both integrator and differentiator is presented below:

2.4.1 Integrators and differentiators

Integrator and differentiator blocks are used to design higher-order filters to meet prescribed specifications. The output of the integrator is proportional to the product of time and input signal. It performs the time integral of either voltage or current depending on the mode of operation. Whereas, the differentiator is the rate of change in input signal with respect to time. In general, integrator and differentiator are referred as first-order low-pass and high-pass filters; respectively. The major applications of the integrators are in the design of A/D convertors, wave shaping circuits, analog/digital filter design. Differentiator plays a crucial role in electronic analog computer processors, filter design, PID controllers, process control and instrumentation etc.

Extensive research has been done on both the differentiator and integrator describing their wide range of applications [36], [39], [36], [37], [43] and [44]. Either integrators or differentiators can be used in almost all the applications but they are chosen depending on the requirement of the circuit and advantages acquired using these blocks. In current-mode approach, the first and foremost design of these blocks is performed by the log-domain technique followed by OTA-C and current-mirror technique. Some of the log-domain integrator/ differentiator approach reported in [30]-[33] and [36]-[39] made significant growth in current mode filter design because of their exponentially increasing linearity. The major drawback in the log-domain designs are higher power consumption and poor matching of currents in the mirror. OTA-C [41], [42] technique is very famous block in the filter design due to its flexibility in tuning the circuit through the use of the transconducatnce parameter. But the disadvantage of this technique is operational frequency range is very low due to the constant gain bandwidth product. The other technique involves the use of current mirrors [43] and [44] which are easier to build, operate and also consume less power. In this technique, the design of integrator is efficient at higher operational frequencies and cannot be used in applications that have lower frequencies. An elaborate explanation of these techniques described is provided below:

2.5 Log-Domain Filters

Designing filters in log-domain is alternative to the designs using op-amp-MOSFET-C, OTA-C and switched Capacitors during which the supply voltage limits the maximum dynamic range that can be obtained. Another disadvantage of implementing these conventional methods is the use of linear resistors that requires higher chip area which is often impractical and further they require tuning for high frequency operations. The approach of designing components such as differentiators and integrators and thereby using them to build filters in the Log-Domain was first proposed by Adams [34] as Trans-linear filters. However these filters were later termed as log-domain filters because of the logarithmic relationship between voltages and currents. These filters proposed by Adams [34] were first order and a synthesis method was proposed by Frey [35] to design

log-domain filters of higher order. In the log-domain filter methodology, the currents having large dynamic range are compressed into voltage and are re-expanded into currents after the operation is performed thereby eliminating the possibility of voltage swings across the integrator's capacitor. The log-domain principle uses the exponential relationship between the collector current and base-emitter voltage of a bipolar transistor or the drain current of a MOS transistor.

2.5.1 Log-domain Integrator

As discussed, log-domain integrator [31], [36] and [37] consists of current to voltage transformer at input and voltage to current transformer at output. The transistors M_2, M_3, M_5 and capacitor C performs the integration of the circuit in voltage form and supplies to the expander. The exponential linearity is achieved by operating the transistors M_1 to M_4 in weak inversion state. To maintain the transistor in weak inversion region the circuit is limited to very low biasing currents leading to the possibility of high noise factor in the circuit. Another drawback is this circuit exhibits very poor matching of currents in the mirrors. The log-domain integrator building block is as shown in Figure 6.

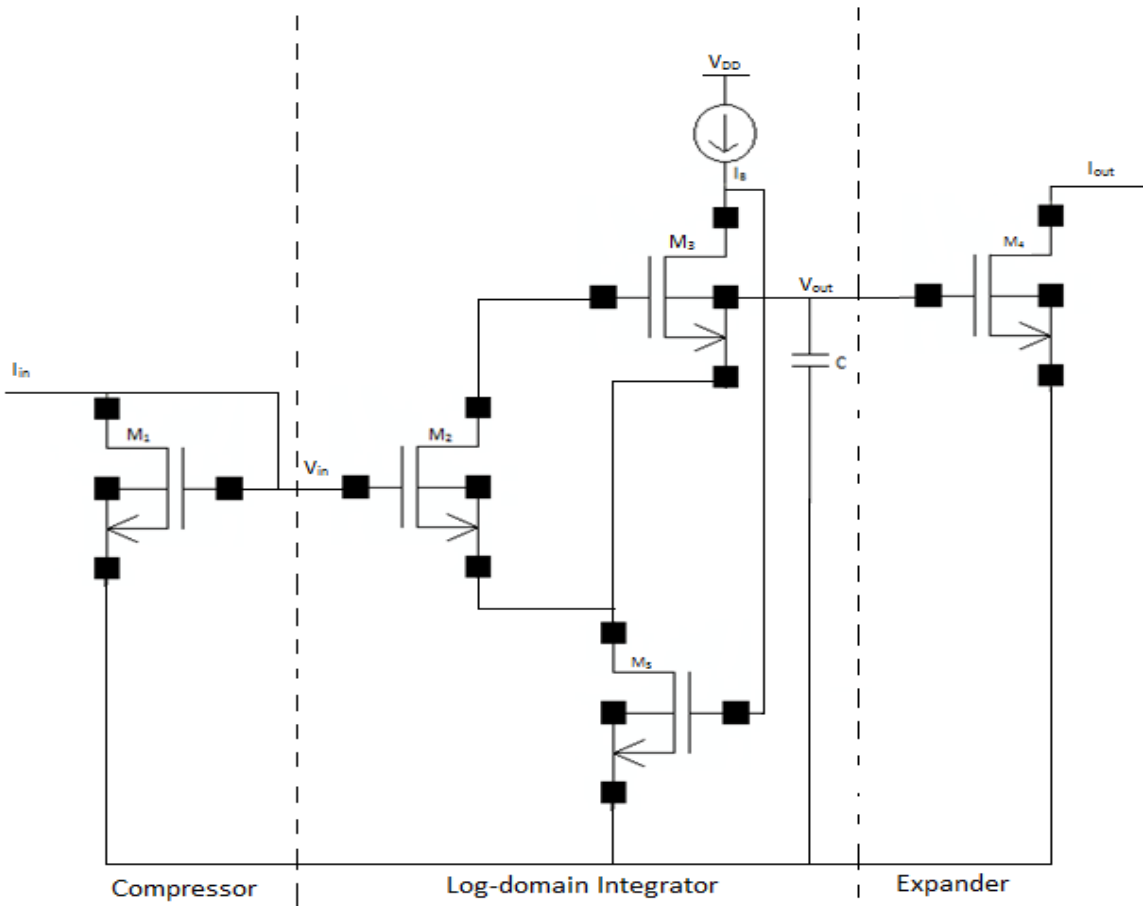

Figure 6 Schematic of log-domain Integrator

2.5.2 Log-Domain Differentiator

The schematic of log-domain differentiator is shown in the Figure 7 based on trans linear circuit by seevinck [38]. The same principle of transformation applies to the differentiator except the major block performs the differentiator function. The schematic of the log-domain differentiator [39] is shown in Figure 7.

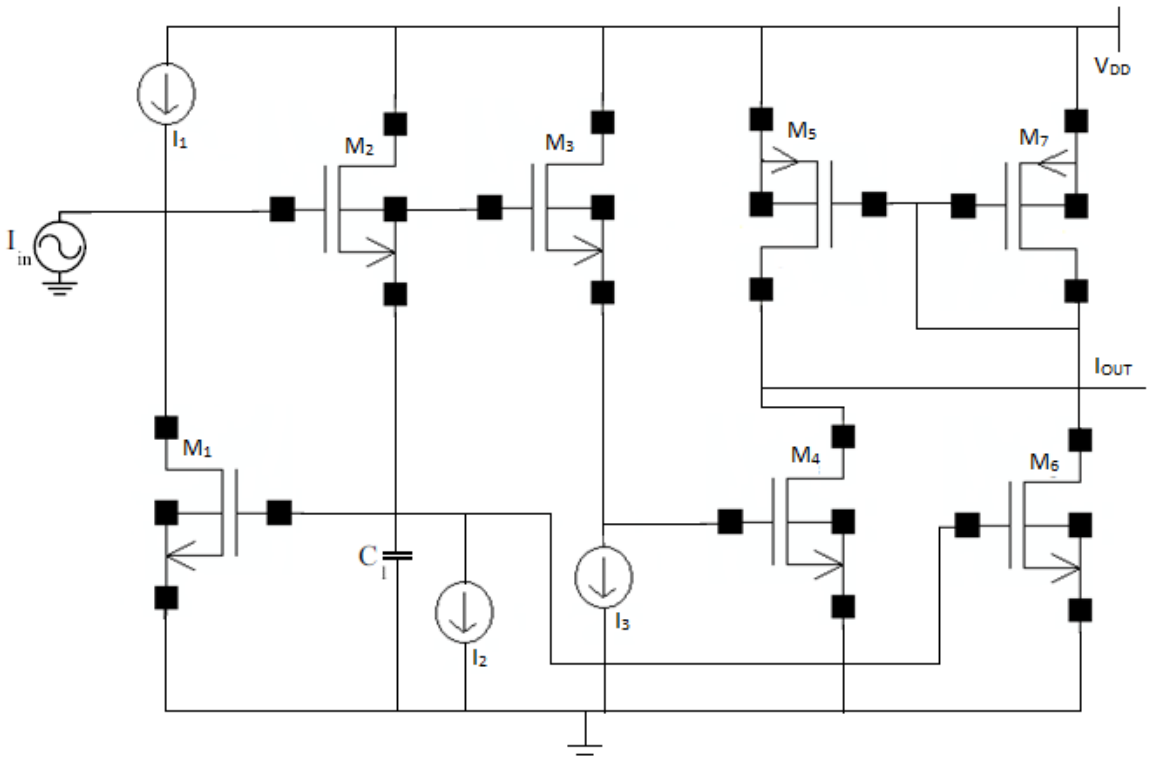

Figure 7 Schematic of Log-Domain Differentiator

The transistors M_1 to M_4 forms trans linear loop pushing the transistors to be in weak inversion region. The PMOS transistors present in the circuit can be in any region as they are not the part of Trans linear functioning. As reported in the [40], the log-domain differentiator performs at very low power than that of the log-domain integrator.

Several components such as lossy differentiators, lossless Differentiators, integrators and further biquadratic filters and also Low-pass, high-Pass, Band-pass and notch filters have been designed using the log-domain methodology through the use of single components [30]-[40].

However, the circuits designed in the log-domain mode are plagued by a serious limitation of higher power consumptions due to additional components that are required to do the compression and expansion of the current that is applied to maintain the linearity of the circuit. Therefore, the implementation of the log-domain principle was not used in this thesis.

2.6 Operational Transconductance Amplifier (OTA)

An Operational transconductance amplifier (OTA) [41], [42] block is one of the most versatile and reliable component in analog filter design due to its characteristics. The complete circuit operates with the transconductance (g_m) parameter which is varied by a change in the bias current (I_B). For better understanding, OTA building block could be compared with the design of transistor. The basic OTA block consists of three terminals; V_{in+}, V_{in-} and I_{out}. The change in bias current (I_B) of the circuit affects the transconductance (g_m) in the same way as the affect in drain current (I_D) tunes transconductance (g_m) in a transistor. With a simple change in the design of the OTA by adding extra transistor pairs parallel to the output load an OTA block could be converted in to a multi-output OTA. The bandwidth, output power and the gain of the amplifier could also be controlled through precise tuning. The circuit diagram for the basic OTA building block [43] is shown in Figure 8.

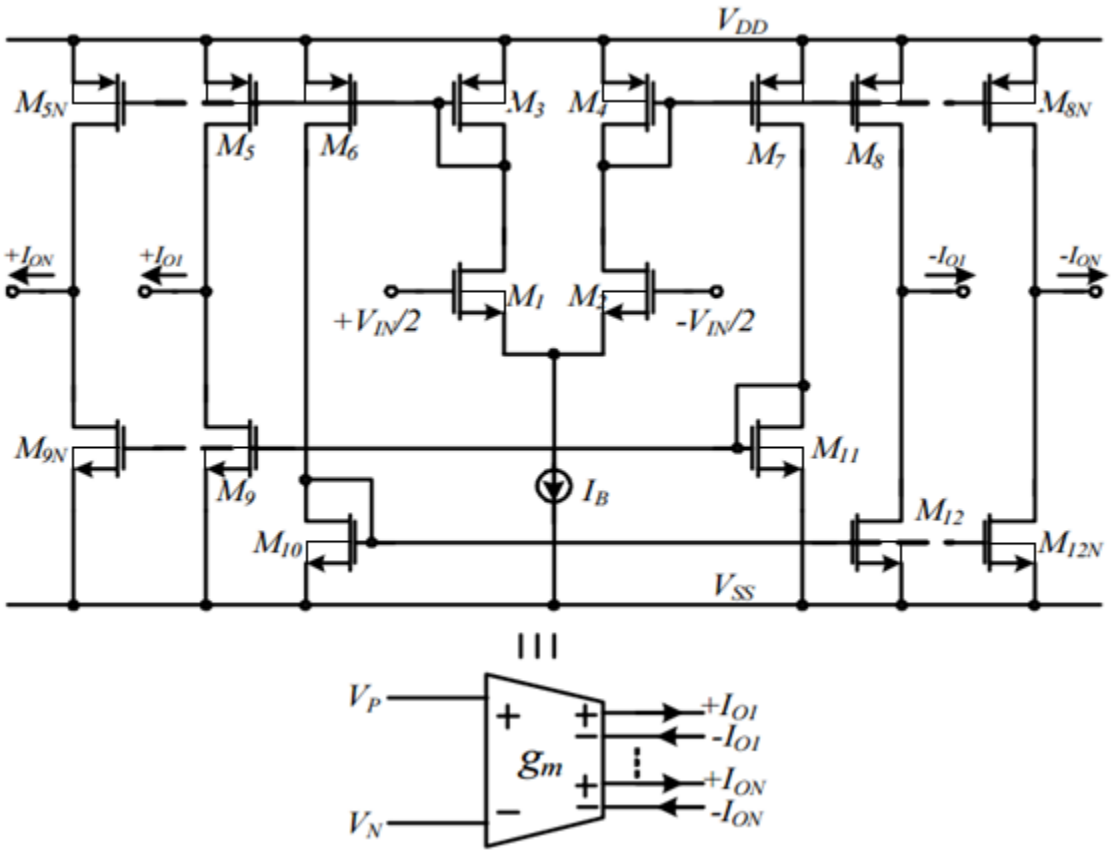

Figure 8 Basic CMOS Multi Output OTA Design

The relation between the output current and the differential input supply of the OTA block as shown in Figure 8 can be expressed as

$$\frac{I_{out}}{V_{in}} = g_m = \sqrt{I_B \left(u_0 . C_{ox} . \frac{W}{L}\right)_{1,2}} \qquad (2.4)$$

From equation (2.4) and Figure 8 the transconductance (g_m) is operated by the bias current along with the parameters of input transistors M_1 and M_2. Depending upon the position of the capacitor (C), OTA block could be used as an integrator or differentiator. The major design structures of current-mode transconductance amplifier with capacitor (OTA-C) are described below.

2.6.1 OTA-C Integrator

OTA-C integrator is designed by placing the capacitor in the same way as a simple RC integrator circuit. In this design [43], OTA block serves as a resistor and the capacitor performs the charging and discharging process as required. The only difference is instead of resistance the transconductance parameter controls the design. The g_m and C values can be tuned to achieve the desired frequency response in the filter design. These integrators can also be classified as lossless and lossy integrators. The circuit designs shown in Figure 9 are operated as lossless and lossy integrators.

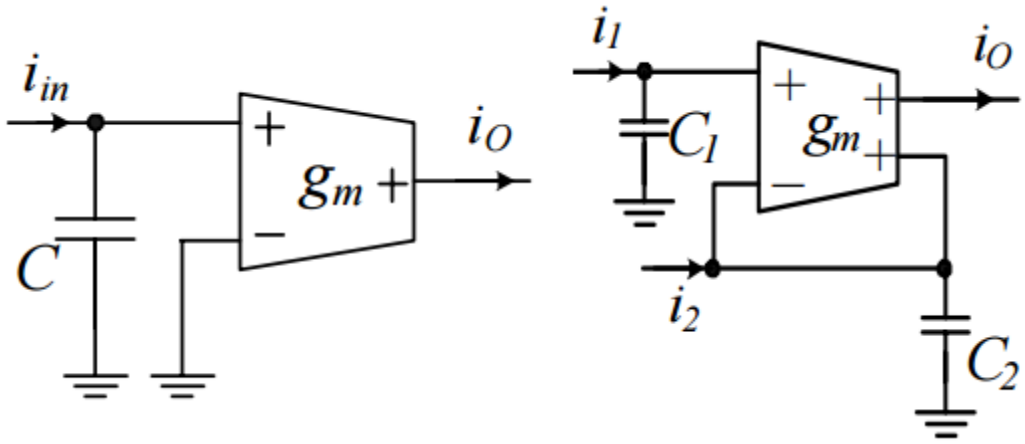

Figure 9 Lossless and Lossy OTA-C Integrators

The transfer functions for lossless and lossy integrators are shown in equations (2.5) and (2.6)

$$\frac{I_{out}}{I_{in}} = \frac{g_m}{s.C} \qquad (2.5)$$

$$I_{out} = \frac{g_m}{C_1} \frac{[i_1 - i_2\left(\frac{C_1}{C_2}\right)]}{s + \frac{g_m}{C_2}} \qquad (2.6)$$

2.6.2 OTA-C Differentiator

The OTA-C differentiator design is very similar to the OTA-C integrator circuit, except for the position of the capacitor. This circuit can also be used as a first-order high pass filter block in several applications. As shown in [44], the lossless differentiator circuit can be used to design a universal filter which will be able to produce any frequency response that is desired through precise tuning of transconductance g_m and capacitor C values. The diagram of lossless OTA-C differentiator is shown in the Figure 10.

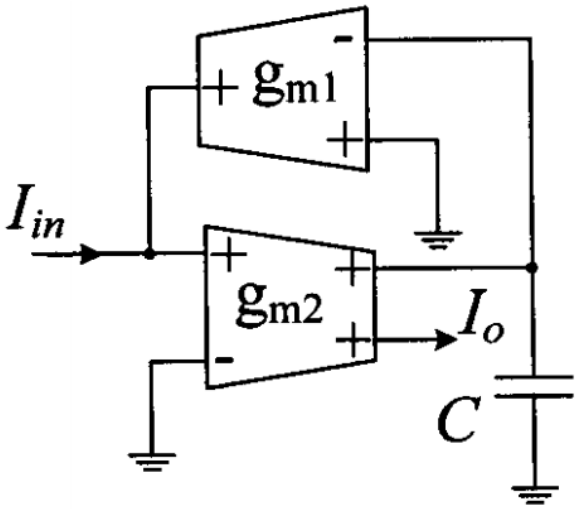

Figure 10 Lossless Multi Output OTA-C Differentiator Circuit

The transfer function of this lossless OTA-C current differentiator is shown in equation (2.7)

$$\frac{I_{out}}{I_{in}} = \frac{s.C}{g_{m1}} \qquad (2.7)$$

Various higher order filters to achieve different functionalities could be designed through the use of these basic building blocks of integrator and differentiator. Various approaches available are: current-mode OTA-C filter realization using canonical forms [45], [46], current-mode dual output OTA-C filters [47], [48], current mode OTA only without 'C' filter design [49]. However, OTA-C designs also suffer from low dynamic range of input voltage and low linearity too. To improve linearity, larger resistances are added to the circuits which in turn increase the chip size and power consumption of the circuit.

2.7 Current-mode integrator using current mirrors

The current-mode integrator using current mirrors [50], [51] are available in two types- Lossy current integrator and lossless current integrator:

2.7.1 Lossy Current Integrator

The circuit design of the lossy current-mode integrator is shown in the Figure 11.

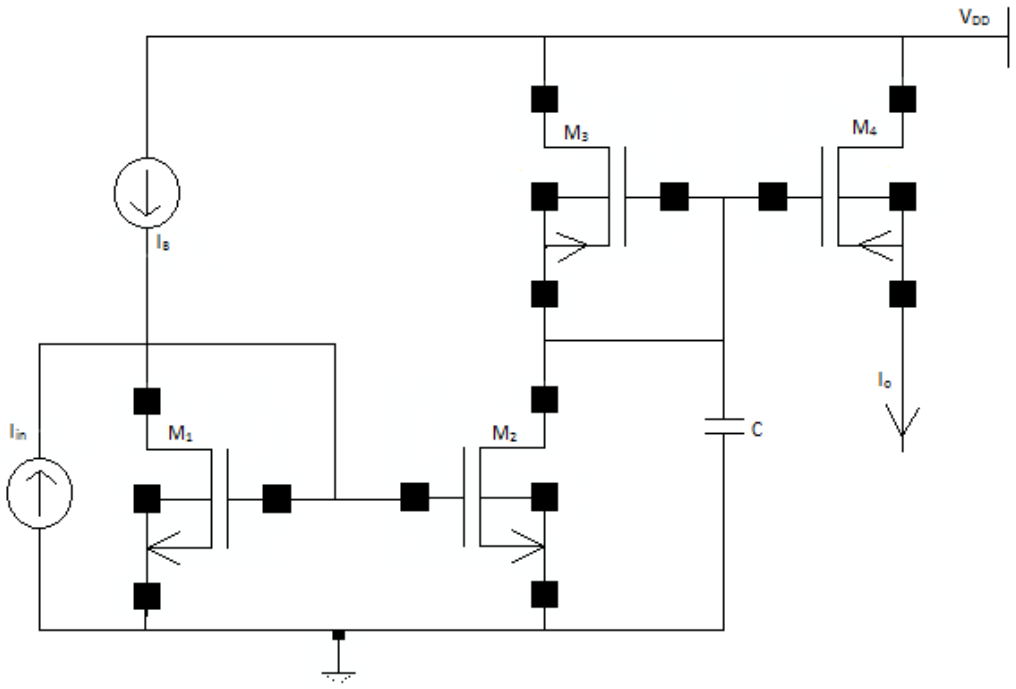

Figure 11 Lossy Current Integrator

From the figure, it can be seen that the integrator is designed using both PMOS and NMOS transistors. The PMOS transistors provide dc biasing for every current mirror and function as active loads. This circuit can also be modified to be multi-input and multi-output design through the addition of current sources parallel to input signal and

transistor pairs parallel to the output load M_4. The input transistors M_1 and M_2 are used to achieve very low input impedance and a capacitor 'C' is coupled to ground satisfying the functionality of integrator. These lossy current integrators can be directly used as first-order building blocks in some of the applications. This current-mode integrator is described as lossy due to the movement of poles from the origin considering the circuit exhibits finite gain.

The output current for lossy current integrator in the above figure can be expressed as

$$I_o = I_B + I_i \qquad (2.8)$$

Assuming the small signal model of the circuit, transfer function can be achieved as:

$$T_1(S) = \frac{i_o}{i_i} = \frac{g_{m2} g_{m4} R_1 R_3}{1 + SCR_3} \qquad (2.9)$$

2.7.2 Lossless Current Integrator

The lossless integrator design is achieved through providing a feedback to the circuit as shown in Figure 12 and 13 that can cancel the loss in the integrator. There are two types of lossless current integrator designs reported: Type 1 and Type 2. The type 1 lossless integrator is shown in the Figure 12.

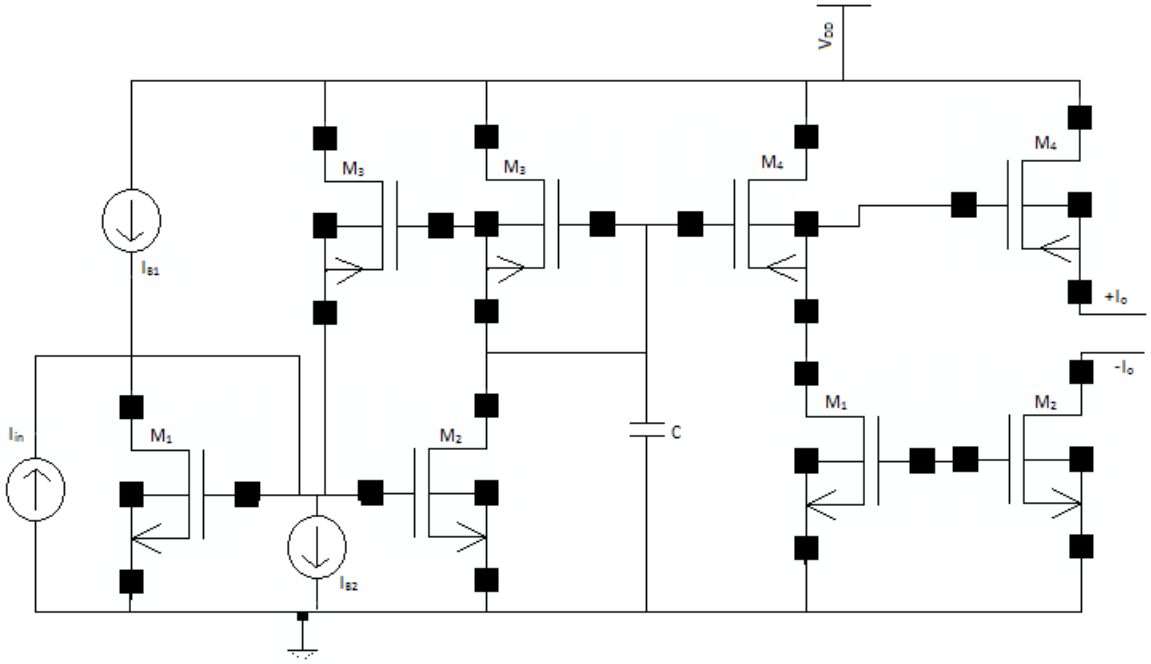

Figure 12 Type I Lossless Current Integrator

The transistor M_5 acts as a positive feedback to the circuit minimizing the loss, while the transistors placed at the output load M4 and M8 are used to invert the output current and could potentially use to increase the output current when desired by changing the W/L ratios of the transistors. The type-2 lossless integrator has a much simpler design that is achieved through reducing the number of transistors and at the same time performing the operation without any loss. The type-2 lossless integrator is presented in Figure 13.

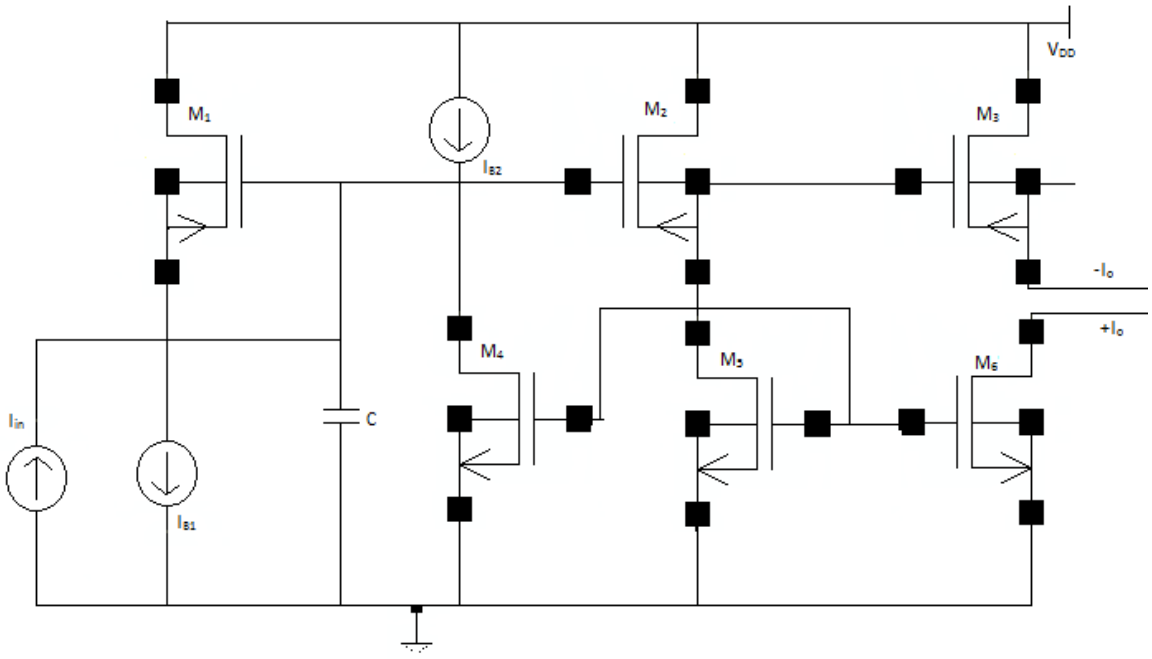

Figure 13 Type 2 Lossless Current Integrator

In the lossless current integrator shown in Figure 13, the feedback operation is performed by the transistors M_4 and M_5, minimizing the loss in the circuit. However, there are few disadvantages with this design. As described earlier, these integrators can only operate in the frequency range of around 10 MHz and the boost in the gain is also often required. Moreover, lossless current integrators have infinite gain at DC making the system unstable due to the offset voltage produced. These designs are tested at a supply voltage of 2.5 V which is considered very high in the current scaling CMOS technologies and often need modifications for the circuit to function at low power and at higher frequency ranges.

2.7.3 Cross-Coupled Gain Boosting Current Mode Integrator:

A novel approach was proposed in [52]. In this design the integrators are connected in a cross-coupled fashion thereby making them to behave as a full differential current mode integrator. The operation of this integrator is similar but the analysis of the full differential integrator is different as they have two input and two output terminals and the transistors are cross coupled. The circuit diagram for the cross-coupled gain boosting current mode integrator is shown in Figure 14.

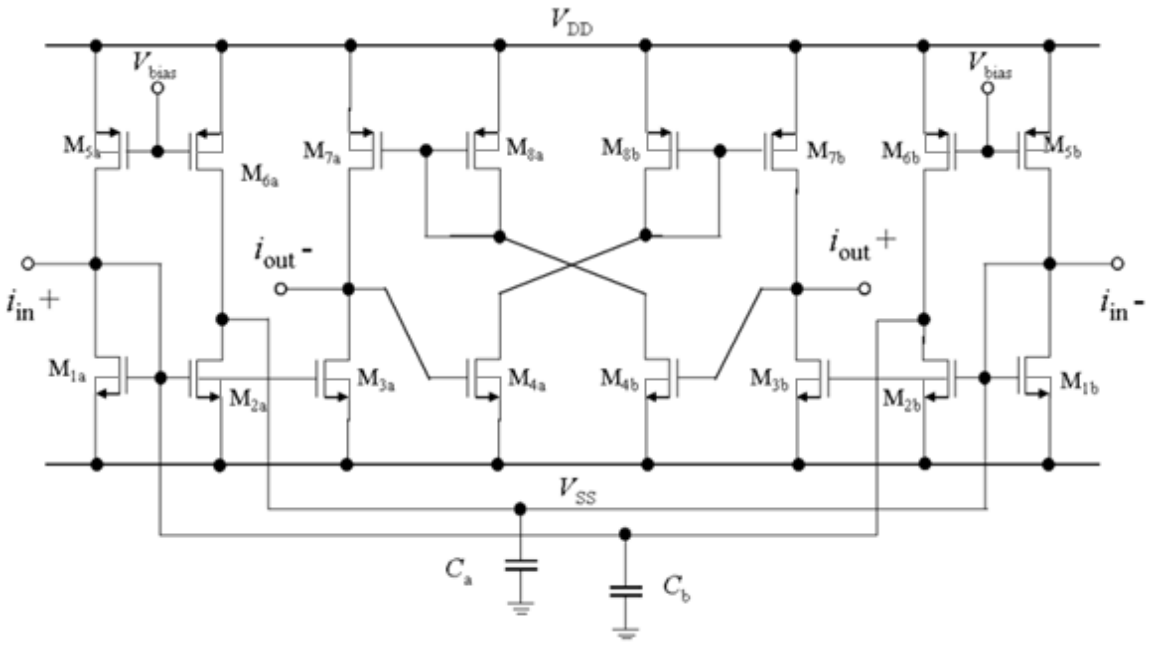

Figure 14 Cross-Coupled Gain Boosting Current-Mode Integrator

The gain of the circuit can be increased through two methods: The first approach is through increasing the transconductance (g_m) and output conductance (g_{ds}) and the other approach is through decreasing the value of capacitance (C). The change in the capacitance value affects the time constant of the integrator which in-turn changes the cut-off frequency. Thus, g_m or g_{ds} value is increased which thereby increase the current

gain of the circuit. The small signal model of the presented current integrator is shown in the Figure 15.

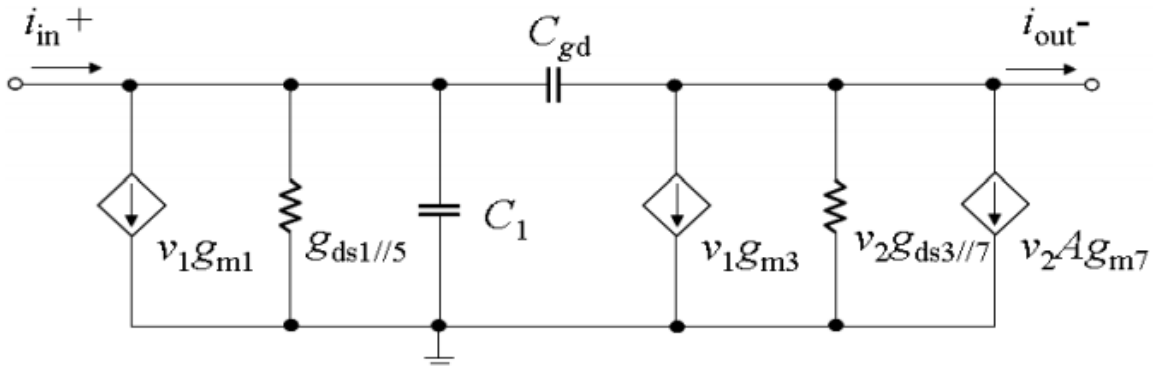

Figure 15 Small-Signal Equivalent Circuit

The difference to the normal design of the integrator is the outputs of the integrator are connected to opposite branches of transistor M_4 and M_8 transferring the value of A. Through this cross coupling procedure the transconductance value of integrator increases to ($A.g_m$). As the circuit is symmetric and since all the transistors are identical half of the circuit is analyzed and used to predict the behavior of the full circuit making the analysis simple. Applying KCL on the circuit

$$(g_{m1} + g_{ds1//5} + sC_1)V_1 + sC_{gd}(V_1 - V_2) = i_{in} \qquad (2.10)$$

$$g_{m3}V_1 + g_{ds3//7} + Ag_{m7}V_2 + sC_{gd}(V_2 - V_1) = i_{out} \qquad (2.11)$$

Solving equations (2.10) and (2.11), the pole can be calculated through

$$P_1 = \frac{g_{m1} + g_{ds1}}{C_1} \qquad (2.12)$$

The current gain and unity gain frequencies are calculated from the equations (2.13) and (2.14)

$$A = \frac{g_{m3} + g_{ds3} + Ag_{m7}}{g_{m1} + g_{ds1}} \qquad (2.13)$$

$$w_o = P_1 A = \frac{g_{m3} + g_{ds3} + Ag_{m7}}{C_1} \qquad (2.14)$$

The parameters of the conventional integrator and the novel current integrator shown in Figure 14 are presented in Table 1.

Table 1 Comparison between Fully Balanced and Cross-Coupled Current-Mode Integrator

Parameter	Fully Balanced Current-Mode Integrator [15]	Reported Cross-Coupled Gain Boosting Integrator
Pole, P_1	$\frac{g_{m1} + g_{ds1}}{C_1}$	$\frac{g_{m1} + g_{ds1}}{C_1}$
Gain, A	$\frac{g_{m3} + g_{ds3}}{g_{m1} + g_{ds1}}$	$\frac{g_{m3} + g_{ds3} + Ag_{m7}}{g_{m1} + g_{ds1}}$
Unity Gain Frequency, w_0	$\frac{g_{m3} + g_{ds3}}{C_1}$	$\frac{g_{m3} + g_{ds3} + Ag_{m7}}{C_1}$

From the table, it can be seen that the gain of the novel circuit is better than that of the conventional one. On the downside, this design makes the circuit more complex as the number of transistors are increased which thereby boosts the power consumption. Overall, the achieved gain is 38.1 dB through this novel circuit which is still quite low for many applications.

CHAPTER 3 DESIGN OF NOVEL CM DIFFERENTIATOR

3.1 Introduction

Two major ways exist for designing analog current mode filters. The First approach involves the realization of the filter using operational transconductance amplifiers and capacitors (OTA-C) [53] and the second method involves the use of a grounded capacitor at the gate of a transistor to approximate an integrator [54]. The first approach often uses larger circuits and operates at lower frequencies, while the second approach is only good for higher frequencies. This chapter introduces a continuous-time current-mode differentiator based on [55] that can operate on a very low supply voltage of 1 V and 0.7 V and frequency ranges from dc to 1 GHz. This circuit is simpler to construct and consumes far less power.

3.2 Current-Mode Differentiator Verses Voltage-Mode Differentiator

In analog voltage-mode circuits, Integrators are benefitted over differentiators. The two major drawbacks of voltage-mode differentiators are that in-principle they amplify high frequency noise too and thereby become unstable at higher frequencies due to the presence of operational amplifier. On the other hand, differentiator designed in current mode will not have these drawbacks. When the input of the differentiator reaches the limited frequency range, its frequency response becomes flat and decreases due to the effect of parasitic capacitances on the circuit thereby eliminating high frequency noise. Stability problems do not exist as we rely on the current mirrors in current-mode designs instead of using operational amplifiers. Moreover, flicker noise which is inherent to MOS transistors can also be potentially eliminated through differentiator blocks.

3.3 The Differentiator

The continuous-time current-mode differentiator is constructed using six MOS transistors and one capacitor. The first pair of transistors M_1 and M_2 is used to form an active load that acts as an input resistance. This load is connected to the input of the current mirror pair M_3 and M_4 through the coupling capacitor C. The output of the differentiator is measured at the drains of M_5 and M_6. The active load of the circuit creates a very low resistance at the input of the circuit to keep the RC time constant small. The circuit diagram of the continuous-time current-mode (CTCM) differentiator is shown in Figure 16.

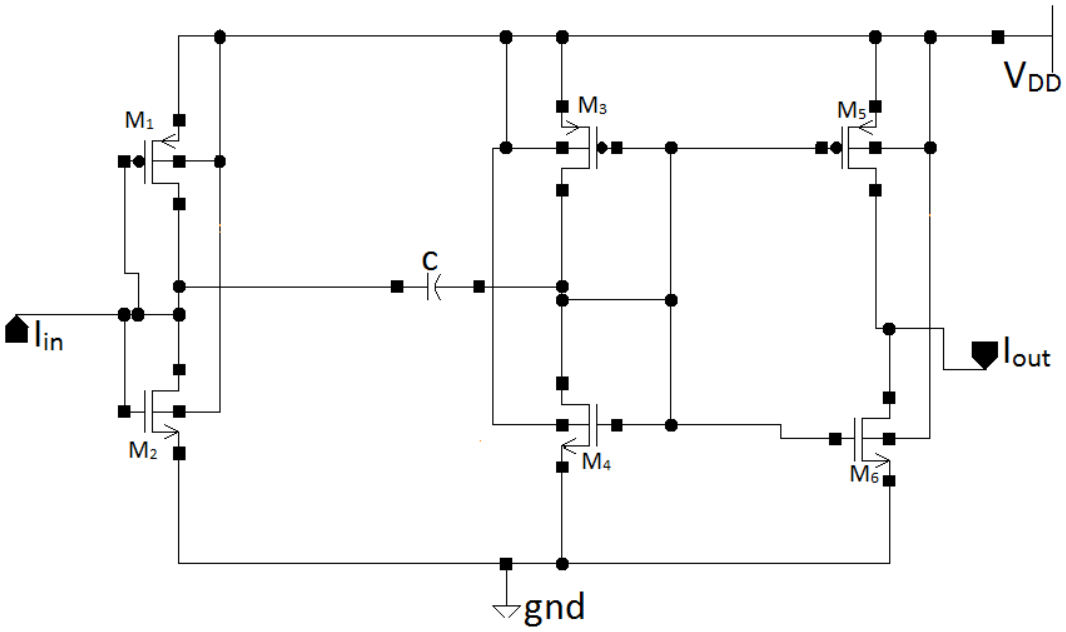

Figure 16 Gate-Driven Differentiator

Considering all N-type and P-type transistors are identical, the current equations are to be given as [55]

$$N-type \quad I_{Dn} = \beta_n(1+\lambda V_g).(V_g - V_{thn})^2 \qquad (3.1)$$

$$P-type \quad I_{Dp} = \beta_p(1+\lambda(V_g - V_{dd})).(V_g - V_{dd} - V_{thp})^2 \qquad (3.2)$$

By ignoring the channel length parameter (λ) the equations can be written as

$$For \quad \beta_n \neq \beta_p, \quad I_D \approx \beta_n \beta_p \frac{(V_{dd} - V_{thn} - V_{thp})^2}{(\sqrt{\beta_n} - \sqrt{\beta_p})^2} \qquad (3.3)$$

$$For \quad \beta_n = \beta_p, \quad I_D \approx \frac{\beta_n}{4} (V_{dd} - V_{thn} - V_{thp})^2 \qquad (3.4)$$

The approximate value of the current (I_D) can be found using these equations for most of the cases. To determine the response of the circuit to the ac input we require the transconductance parameters (g_m and g_{ds}) of the transistor. The g_m and g_{ds} equations for the MOS transistor are given as [55]

$$g_m = \frac{\partial I_D}{\partial V_d} = 2\beta(1 + \lambda V_{ds})(V_{gs} - V_{th}) \qquad (3.5)$$

$$g_{ds} = \frac{\partial I_D}{\partial V_d} = \beta\lambda(V_{gs} - V_{th})^2 \qquad (3.6)$$

After getting these transistor parameters a small signal model of the differentiator circuit is shown in Figure 17.

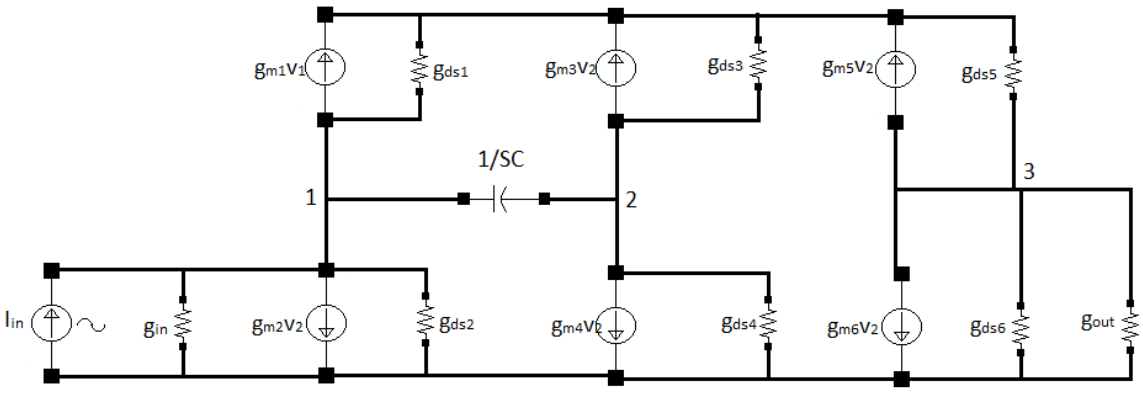

Figure 17 Small-Signal Model for the Differentiator

Assuming all the N-type and P-type transistors to be identical and also the node voltages being equal, the following assumptions can be reasonably made:

$$g_{m2} = g_{m4} = g_{m6} = g_{mn} \qquad (3.7)$$

$$g_{m1} = g_{m3} = g_{m5} = g_{mp} \qquad (3.8)$$

$$g_{ds1} = g_{ds2} = g_{ds3} = g_{dsn} \qquad (3.9)$$

$$g_{ds4} = g_{ds5} = g_{ds6} = g_{dsp} \qquad (3.10)$$

As $(g_{mp} + g_{mn}) >> (g_{dsp} + g_{dsn})$ the transfer function of the circuit is approximated to

$$\frac{I_{out}}{I_{in}} = \frac{-g_{out}(g_{mp} + g_{mn})S}{(2g_{mp} + 2g_{mn} + g_{in})(g_{mp} + g_{mn} + g_{out})\left(S + \left[\frac{(g_{mp} + g_{mn})^2 + g_{in}(g_{mp} + g_{mn})}{(2g_{mp} + 2g_{mn} + g_{in}).C}\right]\right)} \qquad (3.11)$$

Where $S << \frac{(g_{mp}+g_{mn})^2 + g_{in}(g_{mp}+g_{mn})}{(2g_{mp}+2g_{mn}+g_{in}).C}$

Then the transfer function becomes:

$$\frac{I_{out}}{I_{in}} = \frac{-g_{out}(g_{mp} + g_{mn})SC}{\left((g_{mp} + g_{mn})^2 + g_{in}(g_{mp} + g_{mn})\right)(g_{dsn} + g_{dsp} + g_{out})} \qquad (3.12)$$

Since the output of the differentiator is the input of the current mirror and the input of the differentiator is the output of another current mirror it can be assumed that:

$$g_{out} \gg g_{dsn} + g_{dsp} \qquad (3.13)$$

$$g_{in} \ll g_{mp} + g_{mn} \qquad (3.14)$$

From all the assumptions made and the equations resolved, the final output/input transfer function of the circuit is obtained to

$$\frac{I_{out}}{I_{in}} \cong \frac{-S.C}{g_{mp} + g_{mn}} \qquad (3.15)$$

The current-mode differentiator circuit is designed and simulated using the cadence TSMC 65nm CMOS technology. The W/L ratios of PMOS and NMOS transistors are 2.6um/130nm and 2.6um/130nm; respectively upon the assumption that all the transistors are identical.

V_{DD} = 0.7 V, Vin = 500mV, Fin = 1MHz and C = 0.1pf

From the simulation with AC analysis, the behavior of the design for different frequencies can be measured. The response in Figure 18 clearly shows that the slope of the differentiator is 20dB per decade for the frequencies ranging from dc to 700MHz. The resulting simulated transfer function is

$$\frac{I_{out}}{I_{in}} = -\alpha S = -2.3059 * 10^{-9}\, S \qquad (3.16)$$

The transconductance values of NMOS and PMOS transistors are 22.236 uS and 22.236 uS respectively. By substituting all the parameters in the equation (3.15) the value of alpha becomes $2.248*10^{-9}$. The obtained theoretical value of alpha matches very closely to the simulated value. The magnitude and phase response of this differentiator are shown in Figure 18 & Figure 19.

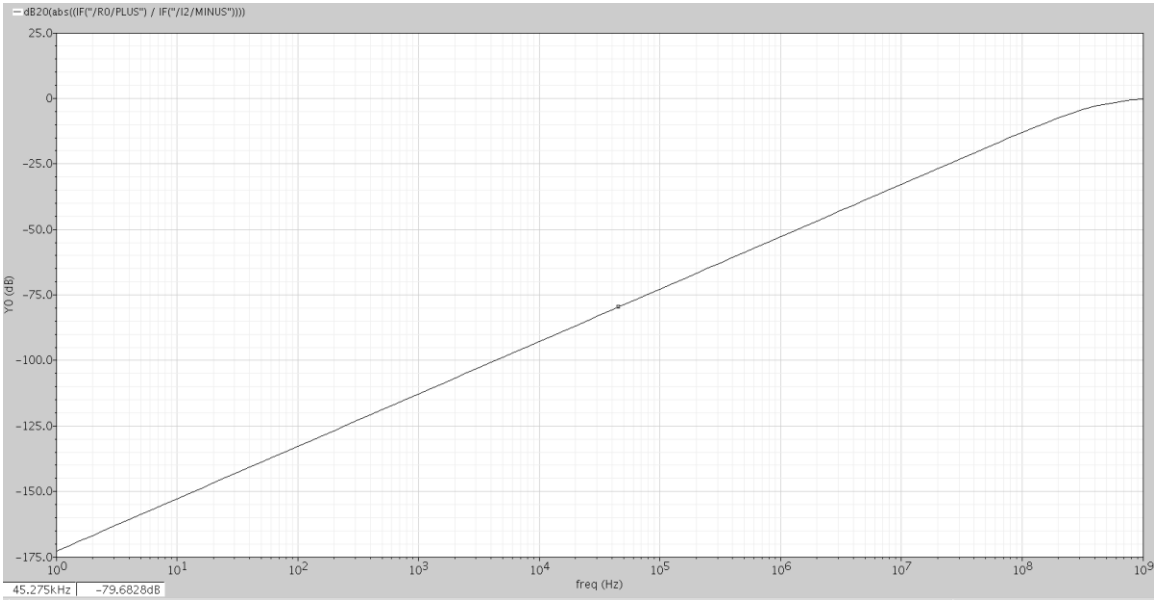

Figure 18 Magnitude Response of the Gate-Driven Differentiator

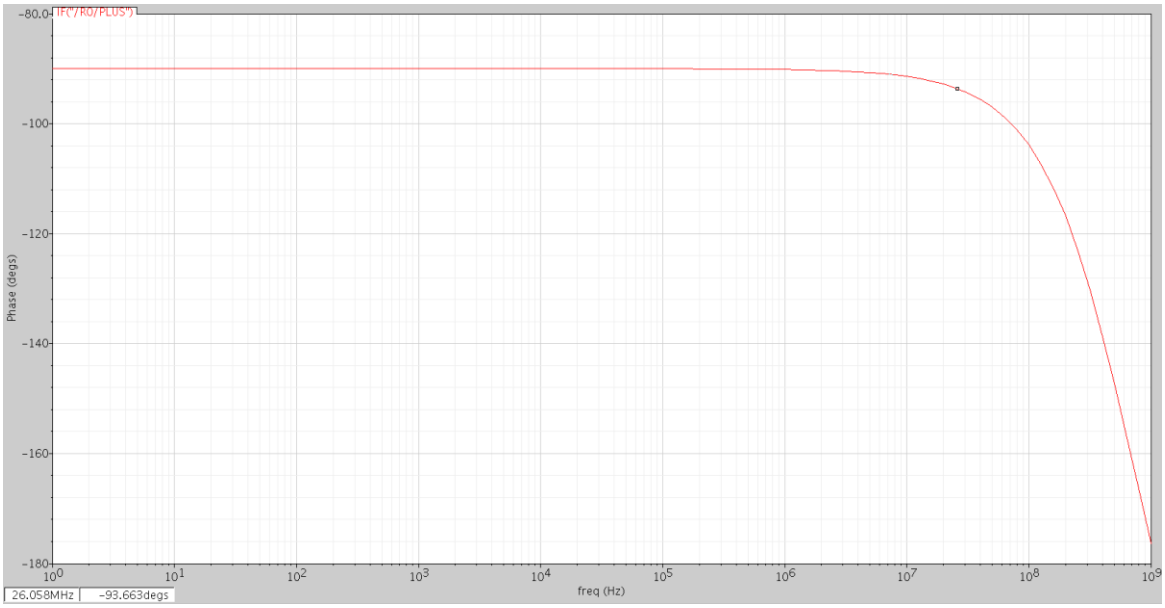

Figure 19 Phase Response of Gate-Driven Differentiator

The performance parameters are shown in Table 2.

Table 2 Performance parameters of the Gate-Driven Differentiator

Process	65nm
Supply Voltage	0.7 V
Gain Bandwidth Product	433.660 MHz
Unity Gain Bandwidth	700 MHz
Power Consumption	192.5 uW
Input Referred Noise	204.7 uA/sqrt(Hz) @ 1KHz for V_{in}=100mV
Power Supply Rejection Ratio	-57.75 dB

3.4 Bulk-Driven Current-Mode Differentiator

A novel bulk-driven current-mode differentiator is designed for the better performance and better adaptability when incorporated into a filter design. The NMOS transistor in the differentiator circuit is replaced with a transistor that is developed through the implementation of bulk-driven technique. In general, the CMOS transistor consists of a fourth terminal other than gate, source and drain. The fourth terminal of the transistor is termed as the bulk, which is generally connected to the source terminal and input signal is supplied to the gate terminal. In this design, the input signal is provided to the bulk terminal and a limited reference voltage is connected to the gate terminal of the NMOS transistor. This reference voltage is set to be greater than or equal to threshold voltage thereby pushing the transistor to the saturation region. This improved circuit design of the novel bulk-driven current-mode differentiator is shown in Figure 20.

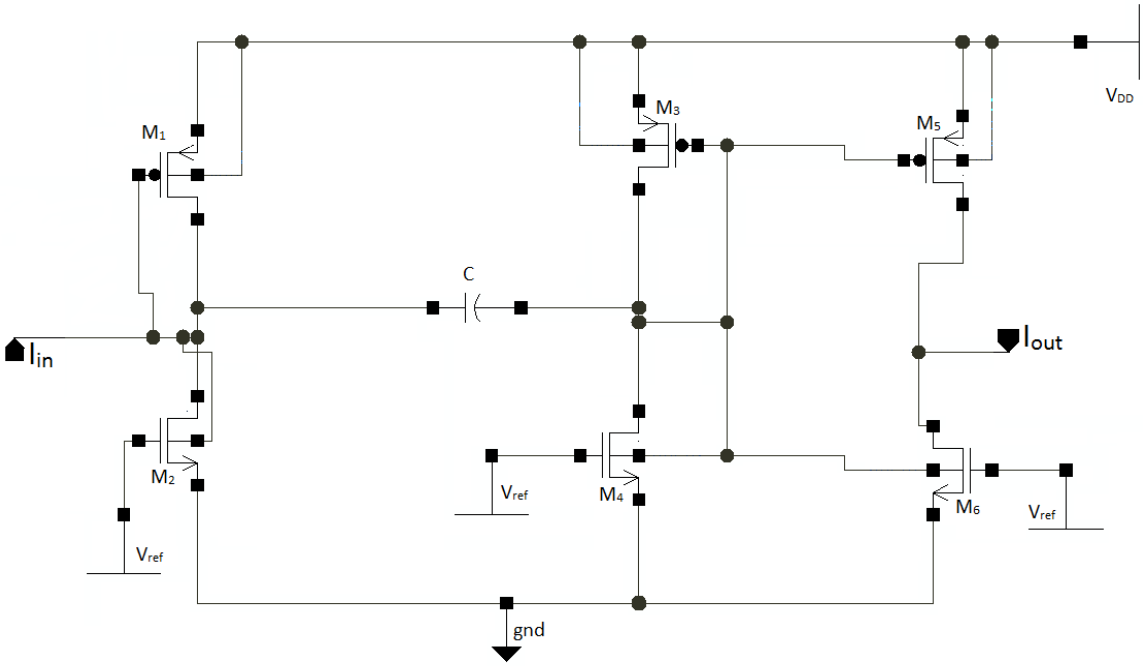

Figure 20 A Novel Bulk-Driven Differentiator

This bulk-driven differentiator is also a simpler circuit with six transistors and a linear capacitor. As shown in Figure 20, there are three gate-driven PMOS and three bulk-

driven NMOS transistors. When the ac input signal is applied to the bulk terminal, the threshold voltage (V_{th}) increases due to the increase in the potential difference between the source and substrate. As a result, a low dc current is required to operate the circuit which in turn consumes very little power.

The transfer function of the bulk-driven current-mode differentiator is as shown below:

$$\left(\frac{I_{out}}{I_{in}}\right)_{Bulk} \cong \frac{-S.C}{g_{mp} + g_{mn}} \qquad (3.17)$$

3.5 Design of Bulk-Driven Differentiator in TSMC 65nm technology

The circuit shown in Figure 20 was designed and simulated in Cadence using the TSMC 65nm CMOS technology. It is assumed that all the transistors are identical and W/L ratios of PMOS and NMOS transistors as 2.6um/130nm and 2.6um/130nm; respectively. The simulation parameters used for the BD differentiator are

V_{DD} = 0.7 V, Vin = 500mV, Fin = 1MHz and C = 0.1pf

The BD differentiator is designed to operate with a supply voltage of $V_{DD} \geq V_{thn} + V_{thp}$ in order to keep the transistors in the saturation region. The circuit in Figure 21 is simulated to measure the threshold voltage of the NMOS transistor and similar procedure is followed for the PMOS transistor as well. The threshold voltages of NMOS and PMOS transistors are 0.339 V and |-0.351| V; respectively.

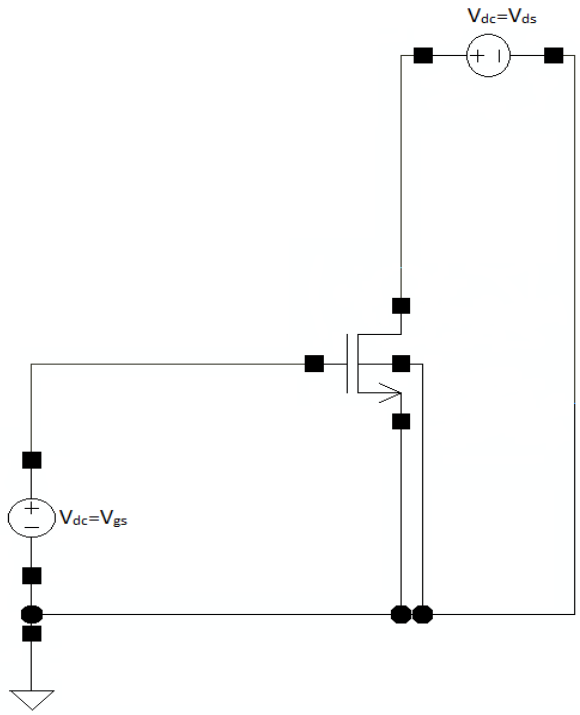

Figure 21 NMOS Configuration to Obtain Threshold Voltage

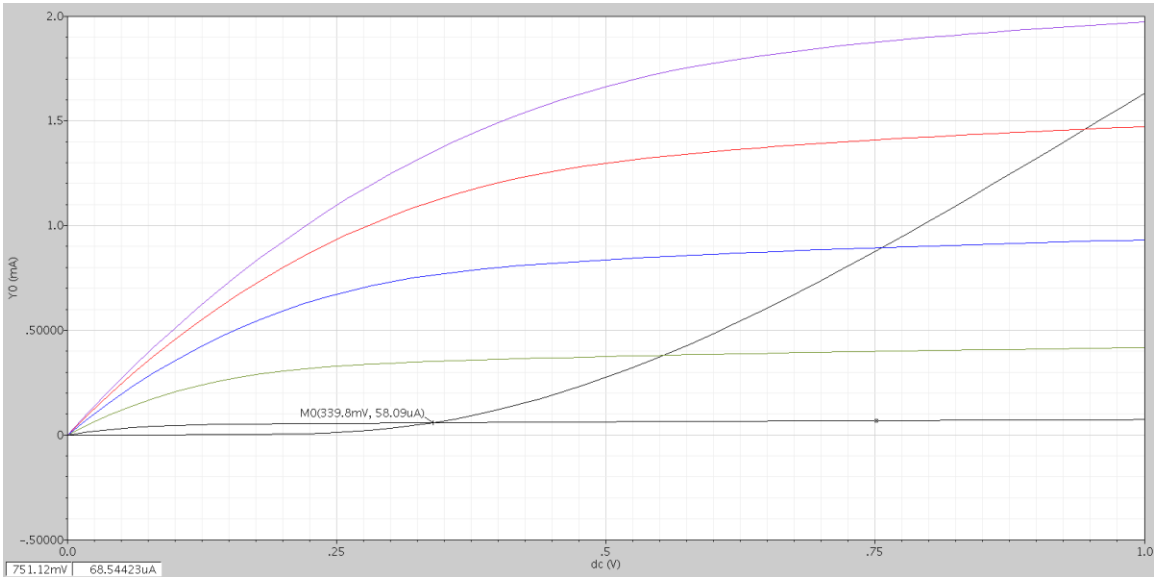

Figure 22 I_{ds} vs V_{th} Plot for NMOS Transistor

The responses of the designed differentiators are verified with a sine wave. The input sine wave is shown in the Figure 23, and Figure 24 and Figure 25 show the magnitude and phase response of the designed bulk-driven differentiator.

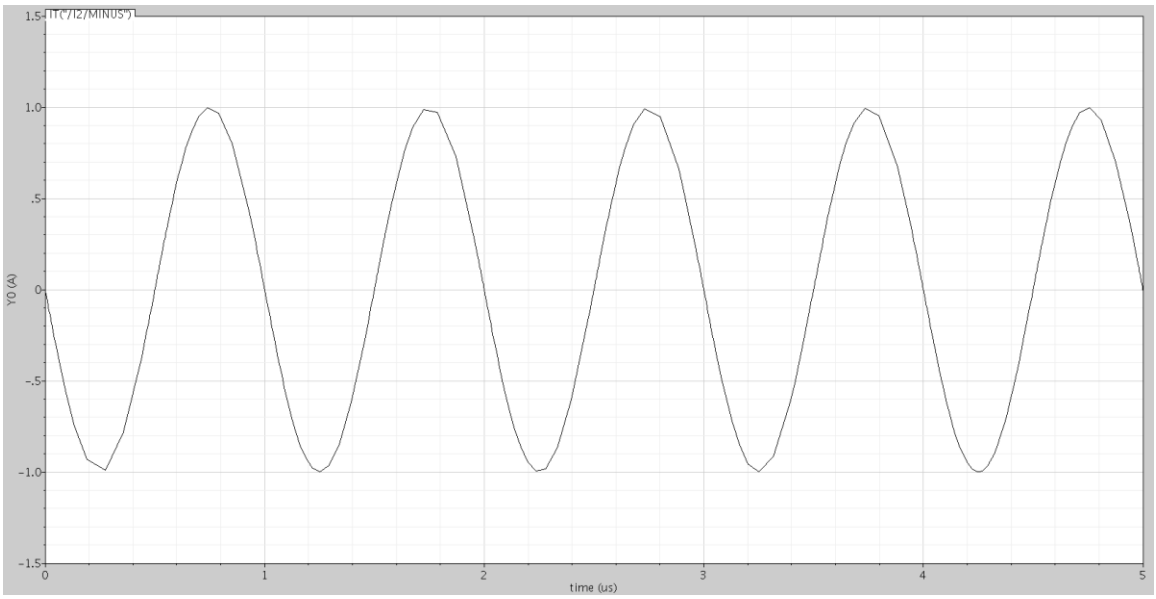

Figure 23 Input Sine Wave for the Differentiator

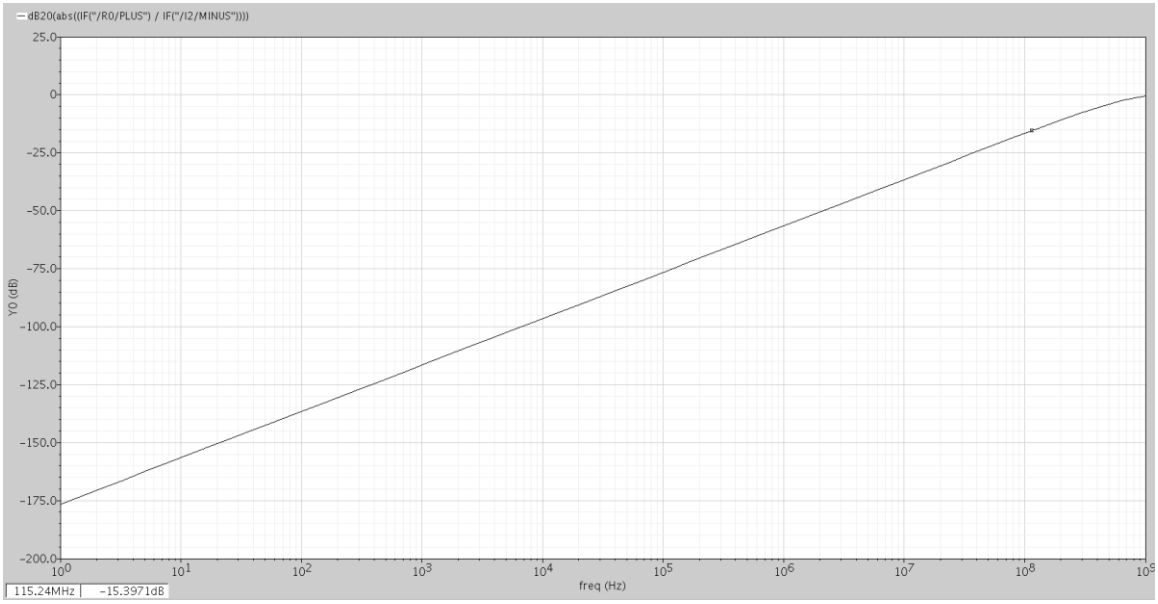

Figure 24 Magnitude Response of the Bulk-Driven Differentiator

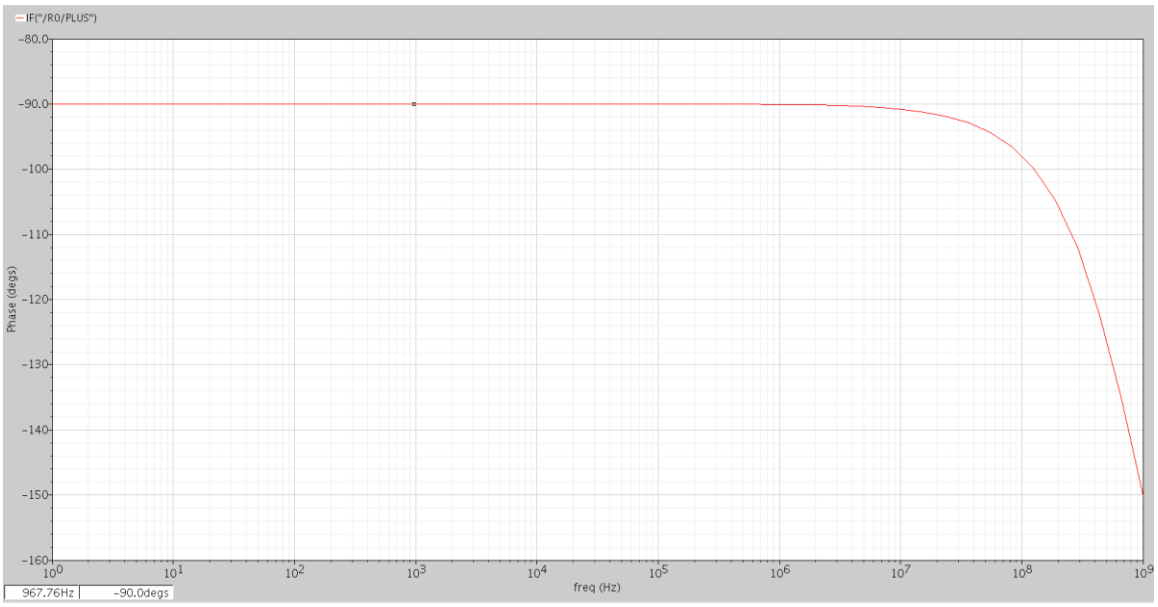

Figure 25 Phase Response of Bulk-Driven Differentiator

From the magnitude response, it is clear that the bulk-driven differentiator works over a frequency range of dc to 1GHz with a slope of 20dB per decade. The resulting simulated transfer function for the frequencies dc to 1GHz is

$$\frac{I_{out}}{I_{in}} = -\beta S = -1.499 * 10^{-9} S \quad (3.18)$$

The transconductance values for the BD NMOS and GD PMOS transistors of the bulk-driven differentiator are 45.12 uS and 22.36 uS respectively. Considering a capacitance of 0.1pF, the value of beta (β) becomes $1.4819*10^{-9.}$ The obtained beta (β) value matches very close to the simulation shown in the Figure 24.

3.5.1 Parameters of Current-Mode Bulk Driven Differentiator

3.5.1.1 SUPPLY VOLTAGE

A bulk-driven current-mode differentiator is designed to improve the power considerations of the analog filter design in scaling CMOS technologies. This circuit exhibits low power dissipation which is achieved by the low supply voltage $V_{dd} \geq V_{tn} + |V_{tp}|$. The V_{tn} and V_{tp} of the bulk-driven differentiator in TSMC 65nm technology are 0.339 V and |-0.351 V| respectively. Hence a supply voltage of 1 V or 0.7 V can be used to operate all the transistors in their saturation region. As the circuit is being designed in the current-mode, a small change in the voltage can produce a substantial difference in the value of current. So, the circuit can be operated efficiently with a small supply voltage.

3.5.1.2 POWER CONSUMPTION

In general, the total power consumption of the circuit depends on the static and dynamic power. In this design, the dynamic power consumption will be negligible as it tends to be very low. The static power consumption is the product of leakage current and the supply voltage. In this design, the static power consumption is due to the leakage current in the transistors along with the consumption due to sub-threshold conduction between source to drain and reverse bias pn-junction between terminals and substrate. In order to measure the static power consumption, a static supply voltage of 0.7 V is used and is shown in the Figure 26.

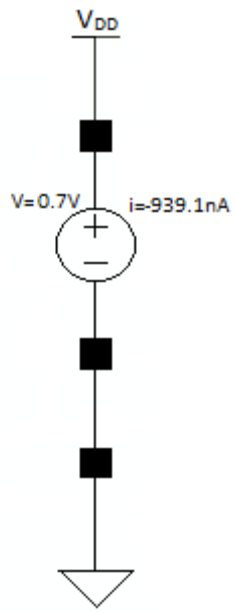

Figure 26 Static Current Measurement from a Supply Voltage of 0.7 V

From the Figure 26, the current drawn by the differentiator circuit is -939.1nA. So the power consumed for the supply voltage of 0.7 V is

$$P = |V * I| = |0.7\ V * -939.1\ nA| = 657.37\ nW.$$

By using the bulk-driven transistor for the designed differentiator, the power consumption of the total circuit is considerably reduced.

3.5.1.3 Power Supply Rejection Ratio

In general, power supply rejection ratio is an important factor for any circuit to maintain its stability at output to eliminate high noise signals. If there is a change in the supply voltage (V_{DD}) of a circuit, then the output varies accordingly. In this circuit, all the transistors are in the saturation region and the transistor operation region operated by the gate or bulk (V_{gs} or V_{bs}) voltage and the supply voltage (V_{DD}). As the PMOS transistor is directly connected to the supply voltage, any change in the supply voltage can drive the transistor in to the cut-off or active regions. The change in supply voltage tends to change

the output voltage. This ratio is generally considered as the power supply rejection ratio (PSRR). The PSRR of the gate-driven and bulk-driven differentiator are shown in the Figure 27.

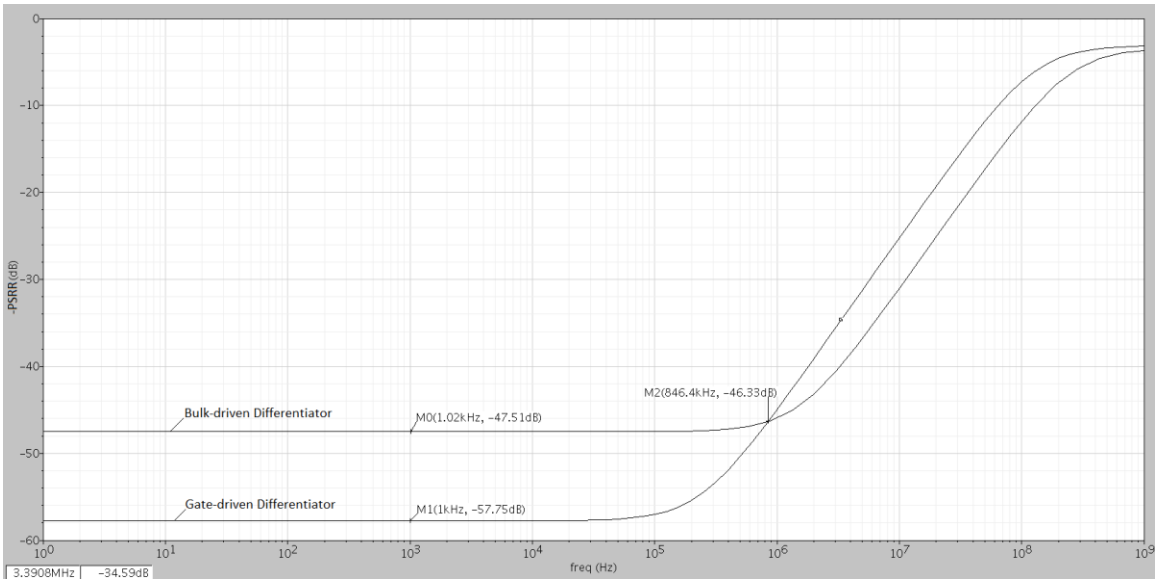

Figure 27 Frequency verses PSRR Plot of Differentiator

Here, the PSRR is measured at the negative terminal of the supply voltage. Hence it is considered as PSRR- which is expressed in "-dB". The "PSRR-" of gate-driven differentiator at 1 KHz is 57.75 dB and that of a bulk-driven differentiator it is 47.51 dB at 1 KHz. The gate-driven differentiator has better PSRR than bulk-driven differentiator. At around 850 KHz, a PSRR value of 46.33 dB is observed for both the differentiators. The differentiator circuit achieves a decent PSRR for both the technologies. The PSRR for the bulk-driven differentiator is 47.51 dB at 1 KHz and 46 dB at 1MHz.

3.5.1.4 NOISE ANALYSIS

The two major sources of noise in CMOSFET are thermal and flicker noise. The thermal noise is also referred as white noise and can occur mostly at higher frequencies whereas flicker noise dominates at low frequencies.

THERMAL NOISE:

The channel thermal noise in the saturation region of MOS transistor is generally referred as

$$(I^2)_{thermal\ noise} = 4.K.T.\gamma.g_m\ [A^2/Hz] \qquad (3.19)$$

Where K is a Boltzmann constant,

T is absolute temperature

g_m is transconductance of the device

γ is complex function of the basic parameter of transistor and bias conditions

By substituting all the values in equation (), the thermal noise of a MOS transistor can be calculated.

FLICKER NOISE:

This is the other dominant source of noise in a MOS transistor that occurs due to the increase in spectral density (1/f) at lower frequencies. It can be referred as

$$(V^2)_{Flicker\ noise} = \frac{K_f}{{C_{ox}}^2.W.L.f} \qquad (3.20)$$

Where K_f is a process dependant parameter of the device,

W and L are width and length of the transistor

C_{ox} is the gate-oxide capacitance per unit area

f is the frequency

The input referred noise of the bulk-driven differentiator is shown in the Figure 28 which is plotted through

cadence.

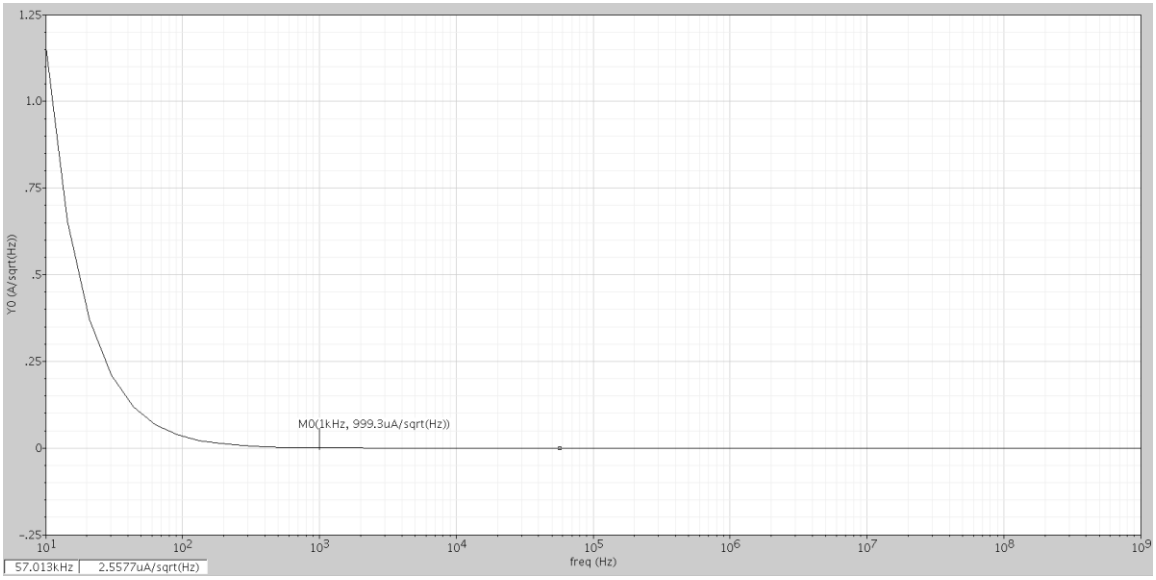

Figure 28 Input referred Noise of Bulk-Driven Differentiator

From all the performance measurements observed, Table 3 shown below is formulated giving the details of designed bulk-driven differentiator:

Table 3 Performance Parameters of Bulk-Driven Differentiator

Process	65nm
Supply Voltage	0.7 V
Gain Bandwidth Product	667.037 MHz
Unity Gain Bandwidth	1 GHz
Power Consumption	657.37 nW
Input Referred noise	999.25 uA/Sqrt(Hz) @ V_{in}=100 mV
Power Supply Rejection Ratio	47.51 dB

CHAPTER 4 DESIGN OF CONTINUOUS-TIME CURRENT-MODE FILTER

4.1 CTCM Gate-Driven Second-Order Building Block

In general, Filter designs are based on first and second order building blocks. Second-order building block is most frequently used in all higher order filter designs with different realization structures. A second-order generalized building block of second-order filter based on [55] is shown in Figure 29 below.

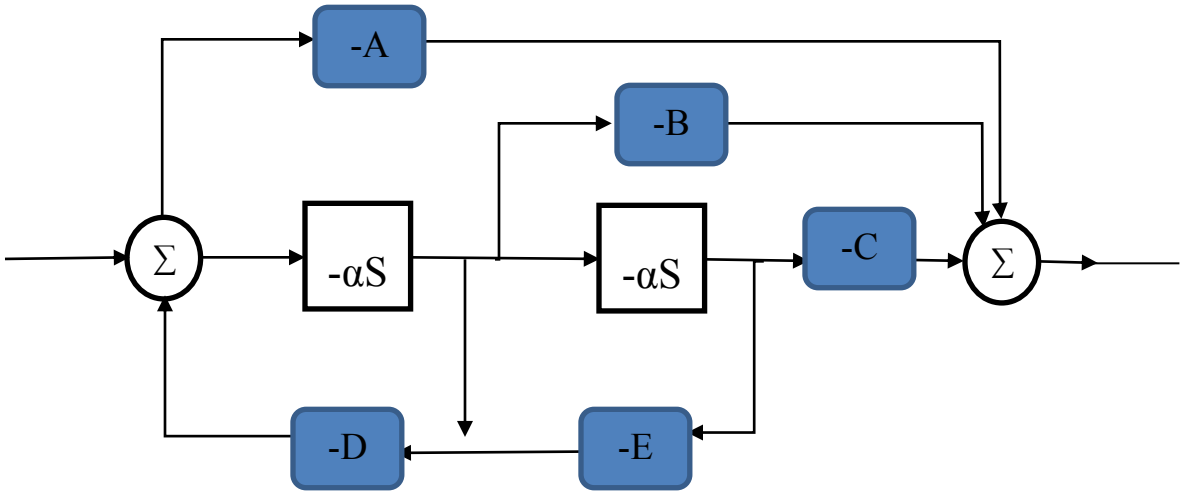

Figure 29 General Second-Order Block Diagram

To generate a desired response, the feedbacks are adjusted according to the functioning differentiator. The block "-αs" in Figure 29 represents the differentiator. In this chapter, we discuss the Chebyshev band pass higher order filter which is second and sixth order. The circuit diagram used for realizing second-order band pass filter is shown in the Figure 30.

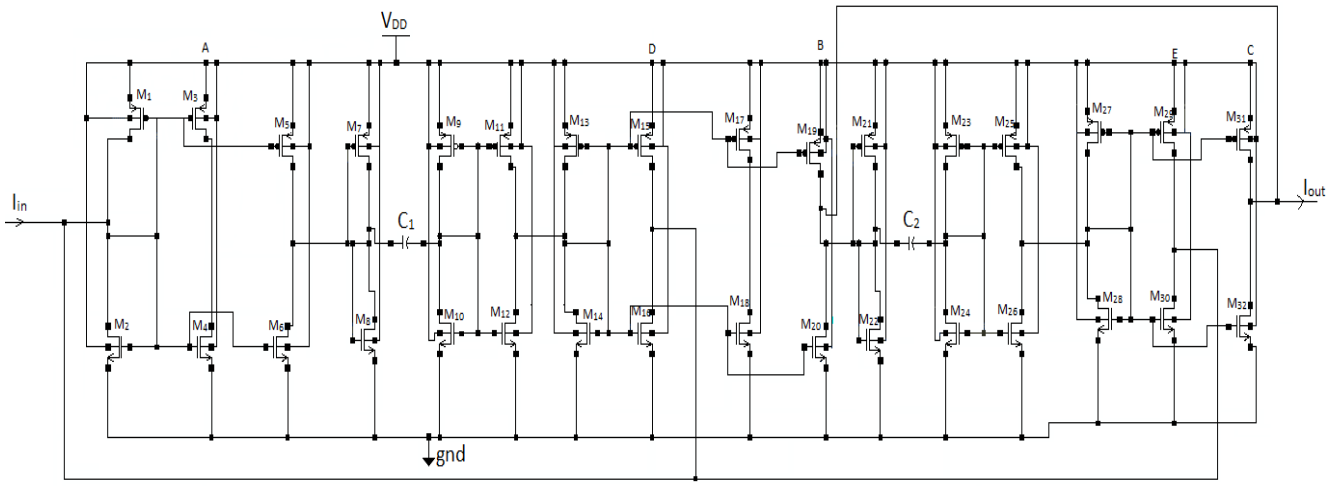

Figure 30 CTCM Gate-Driven Second-Order Band Pass Filter

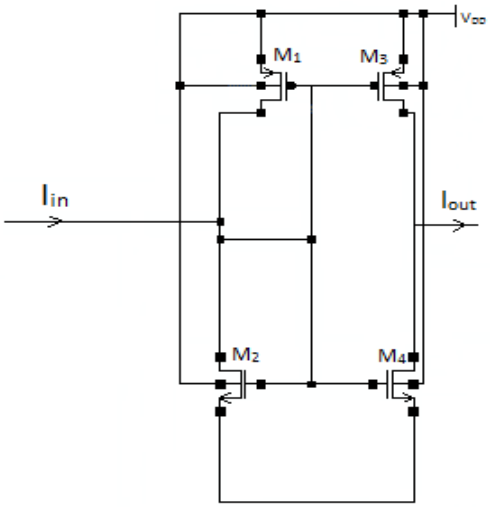

Figure 31 Current Inverting Circuit

The general current inverting circuit with output $I_{out} = -I_{in}$ is shown in the Figure 31. As the coefficients of circuit are negative, a current inverting circuit is used to change the sign of signal to obtain the desired response.

The biquadratic transfer function of the second-order building block is as follows:

$$\frac{I_{out}}{I_{in}} = \frac{-(A + B \propto_1 S + C \propto_1 \propto_2 S^2)}{E \propto_1 \propto_2 S^2 + D \propto_1 S + 1} \qquad (4.1)$$

To realize the Chebyshev band pass filter, the coefficients A and C are made zero. So, the transfer function of the Chebyshev band pass filter can be written as

$$\frac{I_{out}}{I_{in}} = \frac{-B \propto_1 S}{E \propto_1 \propto_2 S^2 + D \propto_1 S + 1} \qquad (4.2)$$

The transfer function used for the design of Chebyshev band pass gate-driven second-order filter design is

$$H_1(s) = \frac{7.4368 \cdot 10^{6} s}{s^2 + 1.5716 \cdot 10^{6} s + 9.0779 \cdot 10^{13}} \qquad (4.3)$$

The parameters in the transfer function are extracted by comparing the equations (4.2) and (4.3) and are displayed in the Table 4.

Table 4 Parameters for the designed Gate-Driven Second-Order Filter

parameter	Value
α_1	$1.04955*10^{-7}$
α_2	$1.04955*10^{-7}$
A	0
B	0.780536
C	0
D	0.16545
E	1

The transistor and capacitor values of the gate-driven second –order band pass filter are displayed in Table 5.

Table 5 Capacitor and Transistor Values for Gate-Driven Second-Order Filter

Device	Value
C_1	16.995pf
C_2	16.995pf
M_1 - M_{14}, M_{17}, M_{18}, M_{21}-M_{28}, M_{31}, M_{32}	2.6um/130nm
M_{15}, M_{16}	430.17nm/130nm
M_{19}, M_{20}	2.0293um/130nm
M_{29}, M_{30}	2.6um/130nm

By substituting all the values in the designed gate-driven second-order filter the magnitude response obtained is as shown in the Figure 32.

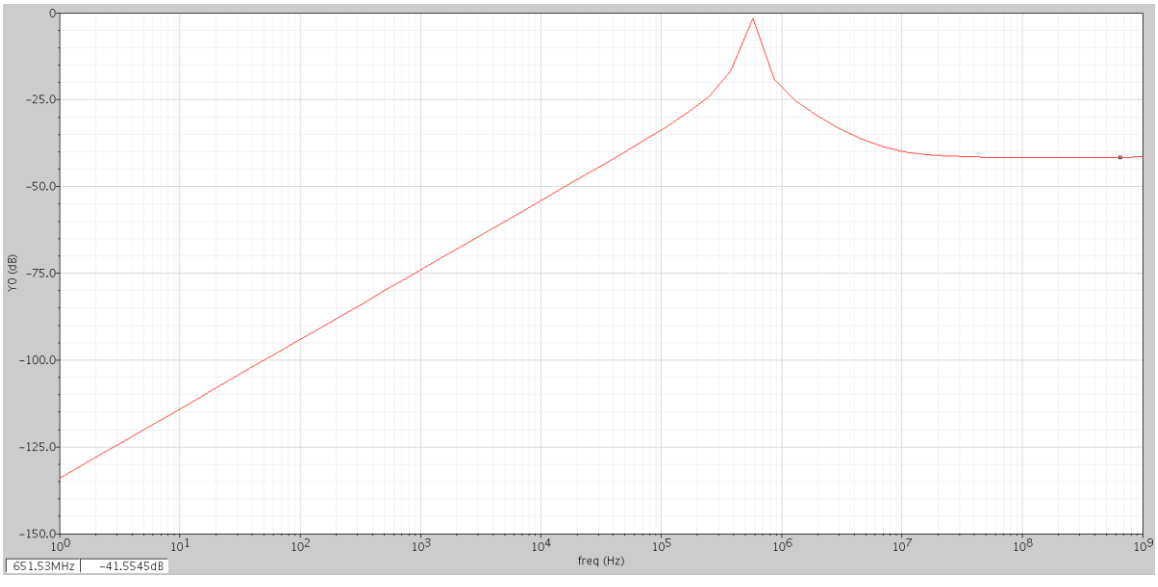

Figure 32 Magnitude Response of Second-Order Band Pass Filter

4.2 CTCM Bulk-Driven Second-Order Filter

The novel bulk-driven current-mode differentiator is used to develop the low power BD second-order structure. From the general second-order block diagram shown in the Figure 29 the conventional gate-driven differentiator is replaced with a bulk-driven differentiator. The circuit diagram used for realizing the CTCM bulk-driven second-order filter is shown in the Figure 33.

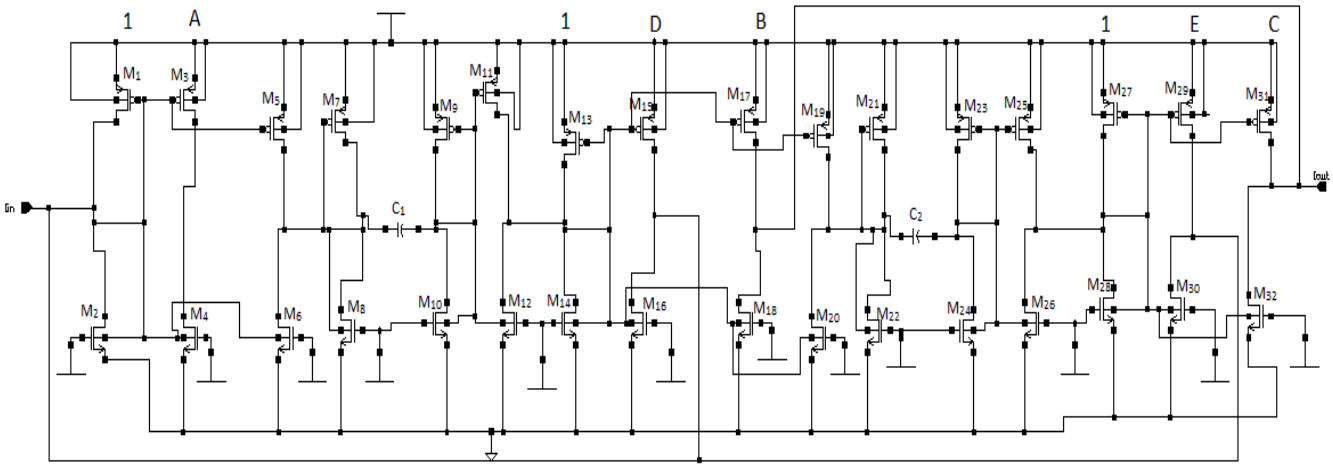

Figure 33 CTCM Bulk-Driven Second-Order Band Pass Filter

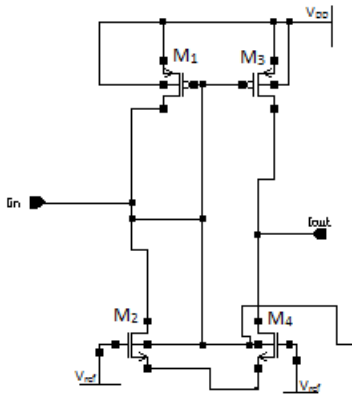

Figure 34 Bulk-Driven Current-Mode Inverting Circuit

Likewise, in the gate-driven filter, a current-mode bulk-driven inverting circuit is used to convert sign of the coefficient values whenever required. In general, normal inverter circuit shown in Figure 31 is used. The major advantage of the bulk-driven inverting circuit is the reduced power dissipation due to the change in the drain current used. The circuit diagram of this bulk-driven inverting circuit is shown in Figure 34. Therefore, the NMOS transistors used in this circuit are designed with the bulk-driven technique.

The transfer function of the CTCM bulk-driven second-order filter is approximated as shown below.

$$\frac{I_{out}}{I_{in}} = \frac{-(A + B\beta_1 S + C\beta_1\beta_2 S^2)}{E\beta_1\beta_2 S^2 + D\beta_1 S + 1} \qquad (4.4)$$

For convenience, the bulk-driven differentiator is represented as [-βS]. For the desired Chebyshev band pass filter response, we should make the A and C coefficients to be zero. The transfer function is further approximated to:

$$\frac{I_{out}}{I_{in}} = \frac{-B\beta_1 S}{E\beta_1\beta_2 S^2 + D\beta_1 S + 1} \qquad (4.5)$$

The transfer function derived for the realization of bulk-driven second-order circuit is approximated to be

$$\frac{I_{out}}{I_{in}} = \frac{2.9984.10^{-8}S}{4.8302.10^{-15}S^2 + 2.9984.10^{-8}S + 1} \qquad (4.6)$$

By comparing equations (4.5) and (4.6), the parameter values are sorted in the Table 6.

Table 6 Extracted Values for Bulk-Driven Second-Order Realization

Parameter	Value
β_1	$1.4577*10^{-10}$
β_2	$1.4577*10^{-10}$
A	0
B	0.5462
C	0
D	$2.857*10^{-3}$
E	1

The transistor and capacitor values for the bulk-driven Chebyshev second-order filter are displayed in Table 7.

Table 7 Transistor and Capacitor Values for Bulk-Driven Second-Order Filter

C_1	9.776pf
C_2	9.776pf
$M_1 – M_{14}$, M_{17}, M_{18}, M_{21}- M_{28}, M_{31}, M_{32}	2.6um/130nm
M_{15}, M_{16}	910nm/130nm
M_{19}, M_{20}	1.42um/130nm
M_{29}, M_{30}	2.6um/130nm

By assigning these to their respective components in the circuit diagram shown in Figure 33, the response of the CTCM bulk-driven Chebyshev second-order filter magnitude response is shown in the Figure 35. The performance comparison table for both gate-driven and bulk-driven second-order filters are shown in the Table 8.

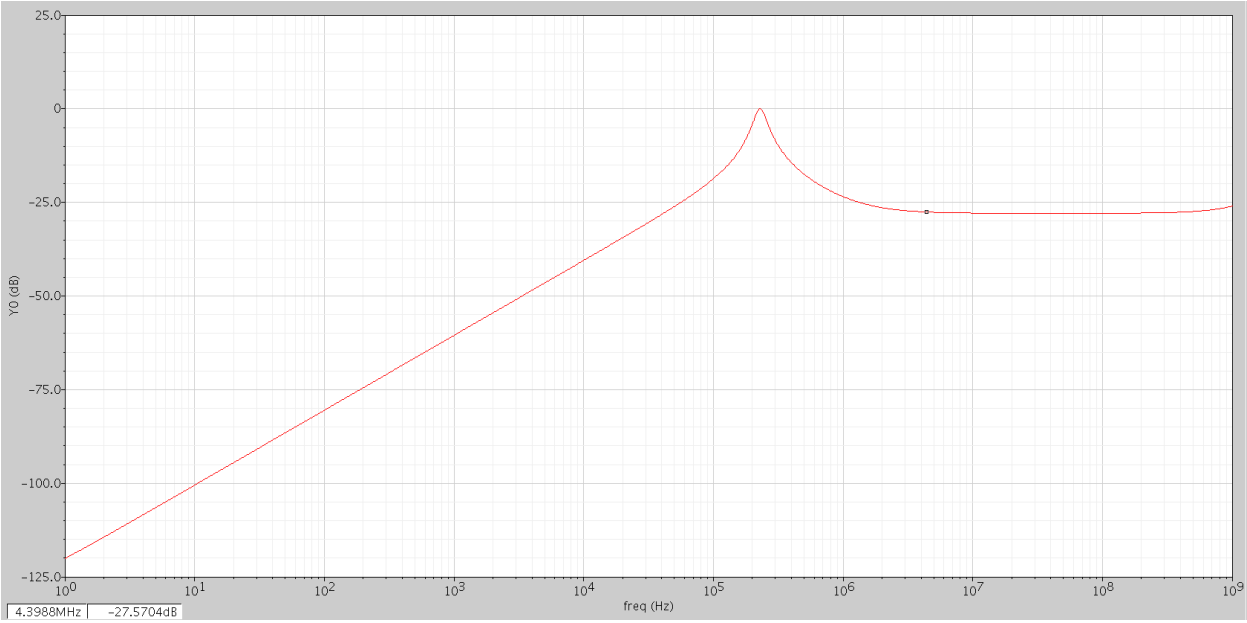

Figure 35 Magnitude Response CTCM Bulk-Driven Second-Order Band Pass Filter

Table 8 Performance Table for GD and BD Second-Order Filters

	Gate-Driven Second-Order	Bulk-Driven Second-Order
Supply Voltage	0.7 V	0.7 V
Lower Stop Band	134 dB	120 dB
Upper Stop Band	43 dB	28 dB
Centre Frequency	575.4 KHz	232.6 KHz
Power Consumption	675.4 uW	122.7 uW

4.3 Cascade Realization of Sixth-order Chebyshev Band-Pass Filter:

To better understand the flexibility of the current-mode differentiator circuit, a sixth-order filter constructed in cascade realization is designed. The Chebyshev band pass response is selected to demonstrate the magnitude response because of the ripple in the band pass. That can be used to verify the order of the circuit and sensitivity levels. The block diagram of the sixth-order stagger tuned Chebyshev band pass filter is shown in the Figure 36.

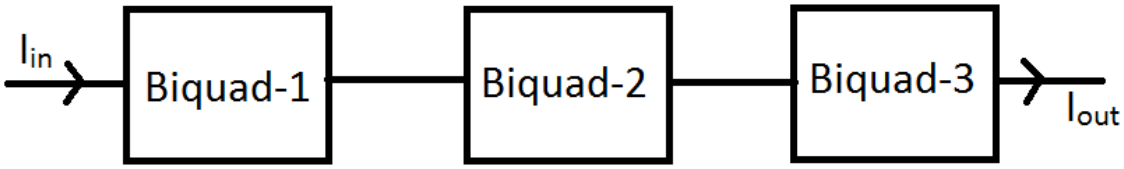

Figure 36 Block Diagram of Sixth-Order Chebyshev Band Pass Filter

In order to design this cascade structure, three second-order blocks placed in order according to the specifications. The sixth-order transfer function that is used for the circuit realization is shown in the equation (4.7)

$$H(s) = \frac{4.113 \cdot 10^{20} s^3}{s^6 + 9.315 \cdot 10^6 s^5 + 6.43 \cdot 10^6 s^4 + 3.721 \cdot 10^{21} s^3 + 1.142 \cdot 10^{29} s^2 + 2.94 \cdot 10^{35} s + 5.607 \cdot 10^{42}} \quad (4.7)$$

From this sixth order equation, we develop three second-order transfer functions by using Geffe algorithm. These transfer function realization procedure is later verified using Mathematica or Matlab. The second-order transfer functions are as follows:

$$H_1(s) = \frac{7.4368 \cdot 10^6 s}{s^2 + 3.0881 \cdot 10^6 s + 3.4838 \cdot 10^{14}} \quad (4.8)$$

$$H_2(s) = \frac{7.4368 \cdot 10^6 s}{s^2 + 4.655 \cdot 10^6 s + 1.7729 \cdot 10^{14}} \quad (4.9)$$

$$H_1(s) = \frac{7.4368 \cdot 10^6 s}{s^2 + 1.5716 \cdot 10^6 s + 9.0779 \cdot 10^{13}} \quad (4.10)$$

The above transfer functions are obtained as per the filter specifications of pass band ripple magnitude (A_P) of 1dB, lower and upper stop bands are 360dB and 80dB respectively. The bandwidth of the filter is considered to be 2MHz.

4.4 Implementation of CTCM Gate-Driven Sixth-Order Chebyshev Filter:

The circuit designed for the CTCM gate-driven sixth-order Chebyshev filter is shown in the Figure 37. It is simulated with TSMC 65nm CMOS technology and an AC analysis is performed for the frequency range of dc to 1GHz.

Comparing the equations (4.8) (4.9) (4.10) with equation (4.2) for each second-order block the parameter values can be extracted. These values for the three gate-driven second-order blocks are shown in the Table 9.

Table 9 Extracted Values for CTCM Gate-Driven Sixth-Order Chebyshev Filter

	Second-order 1	**Second-order 2**	**Second-order 3**
α_1	$5.357*10^{-8}$	7.5103*10-8	1.0495*10-7
α_2	$5.357*10^{-8}$	7.5103*10-8	1.0495*10-7
A	0	0	0
B	0.39843	0.55852	0.78053
C	0	0	0
D	0.16545	0.34961	0.16545
E	1	1	1

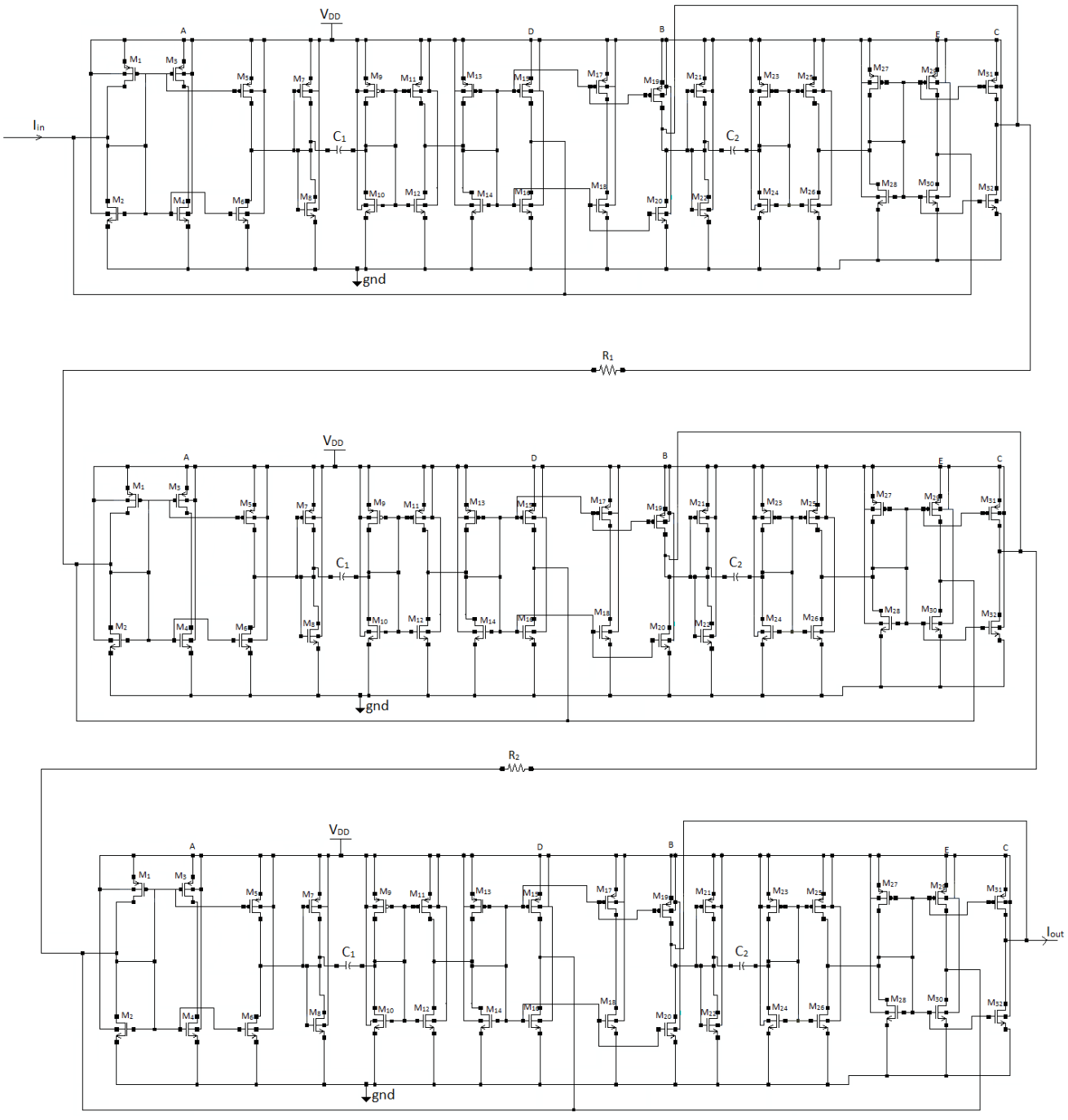

Figure 37 Block Diagram of Sixth-Order Chebyshev Band Pass Filter

The calculated W/L ratios of transistor and capacitor values are shown in Table 10.

Table 10 Transistor and Capacitor Values of CTCM Gate-Driven Sixth-Order Filter

	Second-order 1	**Second-order 2**	**Second-order 3**
C_1	42.058pf	58.775pf	29.995pf
C_2	42.058pf	58.775pf	29.995pf
M_1- M_{14},M_{17}, M_{18}, M_{21}- M_{28}, M_{31}, M_{32}	2.6um/130nm	2.6um/130nm	2.6/130nm
M_{15}, M_{16}	430nm/130nm	910nm/130nm	430nm/130nm
M_{19}, M_{20}	1.035um/130nm	1.452um/130nm	2.029um/130nm
M_{29}, M_{30}	2.6um/130nm	2.6um/130nm	2.6um/130nm

The gate-driven sixth-order filter is simulated with all the calculated values substituted in the band pass filter. The magnitude response for the simulated filter is shown in the Figure 38 and it matches closely to all the specifications mentioned for calculations.

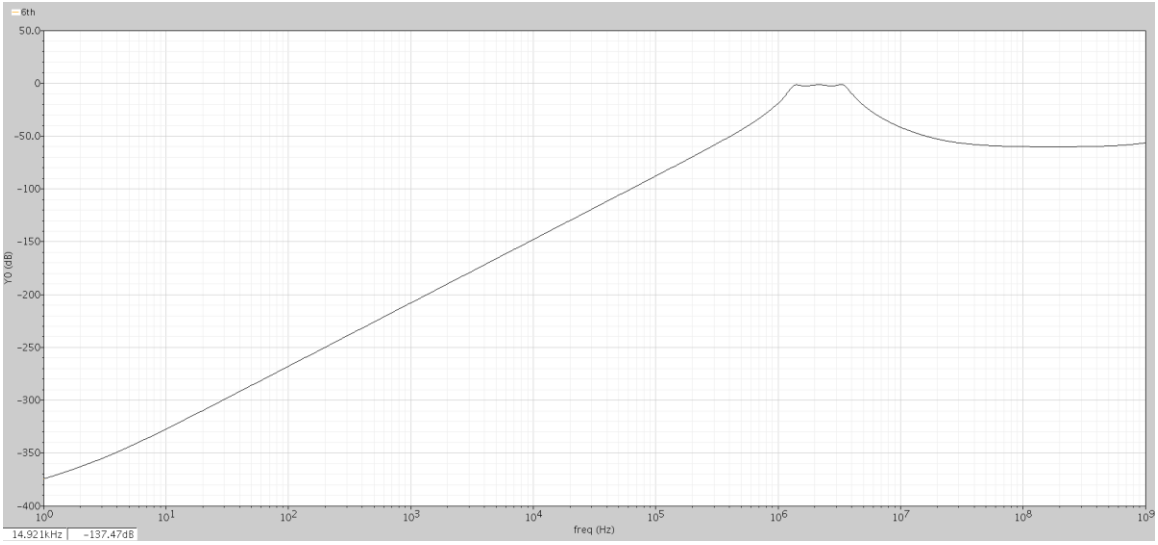

Figure 38 Magnitude Response of CTCM GD Chebyshev Band Pass Sixth-Order Filter

A 1 dB ripple will be present in the design specifications of Chebyshev band pass filter, in the pass band frequency range. The pass band ripple of 1dB is shown in the Figure 39 which also accurately represents the order of the filter. The response shown fluctuates within a range of 1dB and has three ripples. Therefore, the order of the circuit can be identified as n=6.

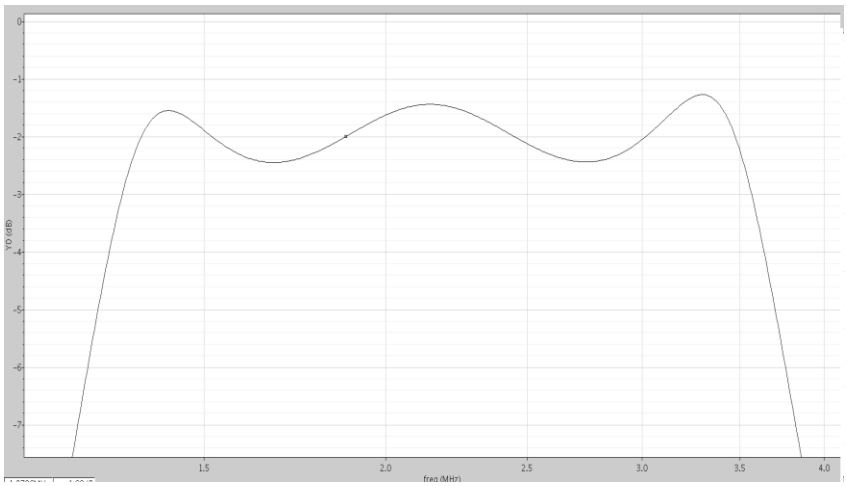

Figure 39 Pass Band Ripple of 1dB for GD Sixth-Order Filter

4.5 Implementation of CTCM Bulk-Driven Sixth-Order Chebyshev Filter:

The circuit diagram for the CTCM bulk-driven Chebyshev sixth-order band pass filter is shown in the Figure 40. In the design, three second-order bulk-driven filter are connected in cascade with very low resistor likewise in the gate-driven design. For better understanding same transfer function is used for both the sixth-order filters. Therefore, the coefficient parameters are identical for both the filters which is shown in Table 9. From these parameters, we derive the transistor and capacitor values accordingly. In bulk-driven filter, there is a change in the capacitor values due to the variation in the transconductance (g_m) of the transistors.

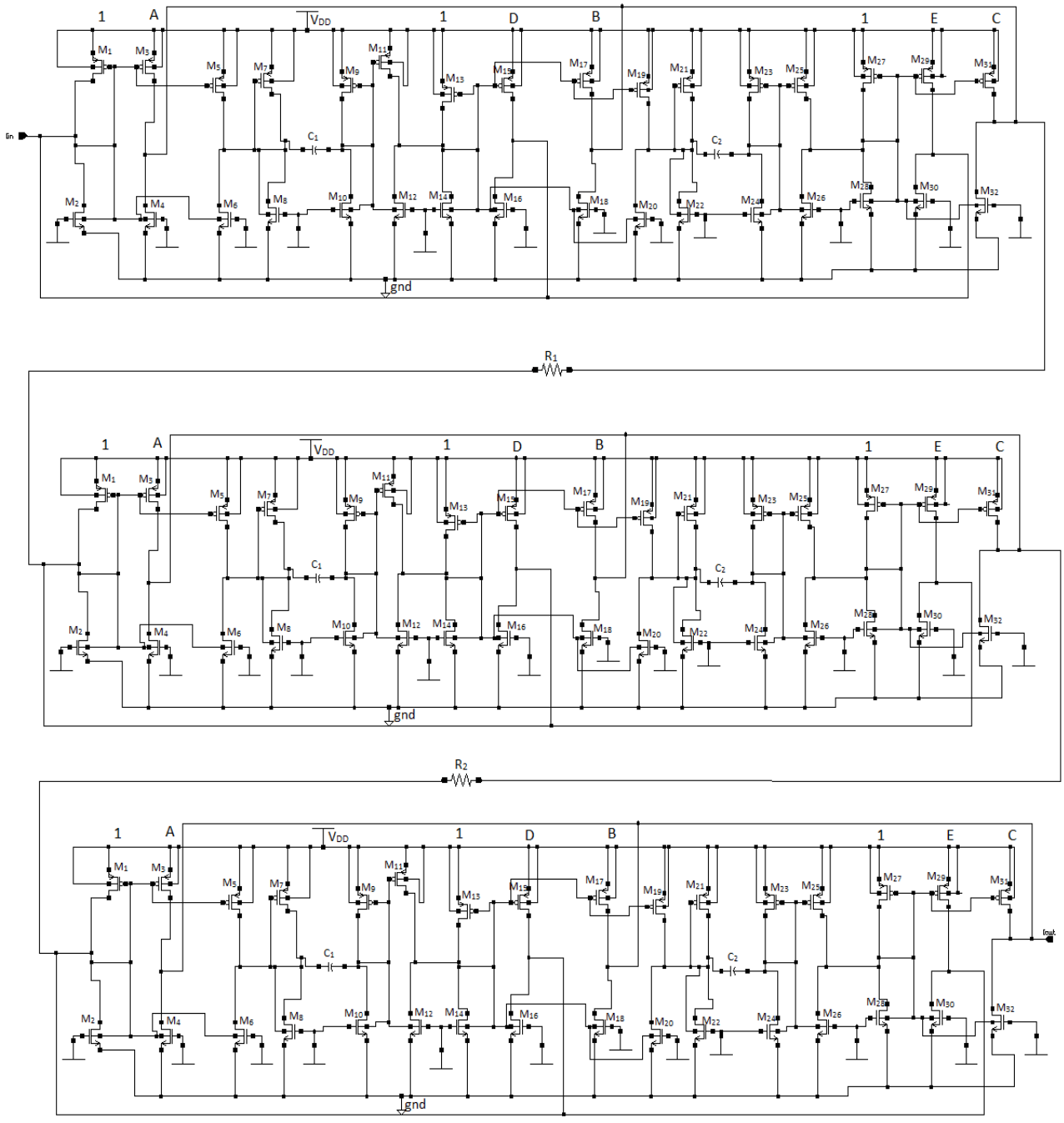

Figure 40 CTCM Gate-Driven Chebyshev Band Pass Sixth-Order Filter

For the three second-order transfer functions, the obtained values for the Chebyshev band pass filter from Table 7 is shown in Table 11.

Table 11 Transistor and Capacitor Values of CTCM Bulk-Driven Sixth-Order Filter

	Second-order 1	**Second-order 2**	**Second-order 3**
C_1	3.058pf	6.775pf	9.995pf
C_2	3.058pf	6.775pf	9.995pf
M_1- M_{14},M_{17}, M_{18}, M_{21}- M_{28}, M_{31}, M_{32}	2.6um/130nm	2.6um/130nm	2.6um/130nm
M_{15}, M_{16}	430nm/130nm	910nm/130nm	430nm/130nm
M_{19}, M_{20}	1.035um/130nm	1.452um/130nm	2.029um/130nm
M_{29}, M_{30}	2.6um/130nm	2.6um/130nm	2.6um/130nm

By substituting all the derived values in the circuit design, the magnitude response of the CTCM bulk-driven sixth-order filter simulated is shown in Figure 41.

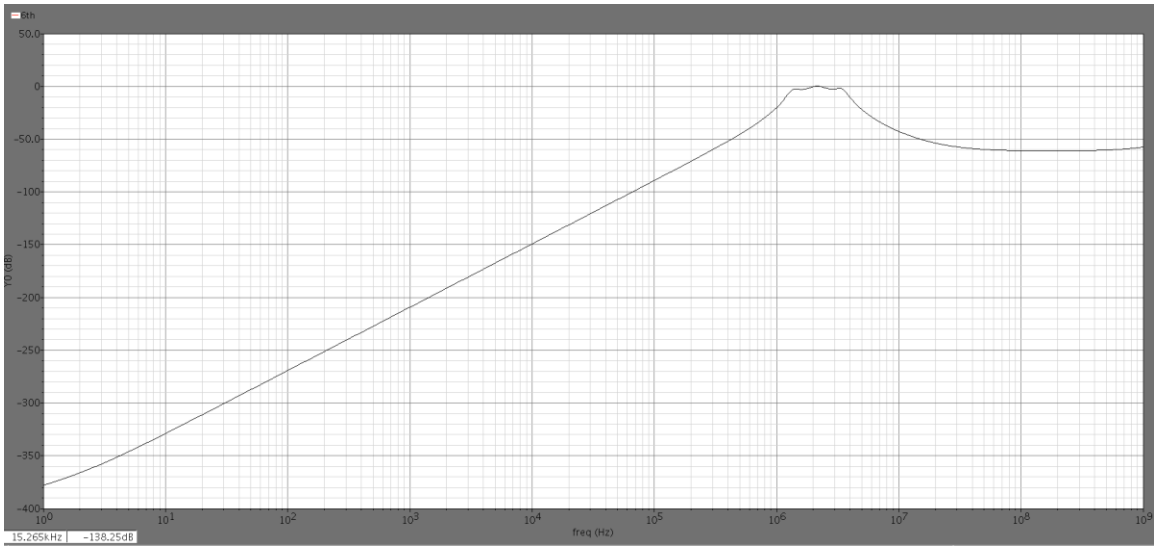

Figure 41 Magnitude Response of CTCM Bulk-Driven Sixth-Order Filter

The pass band ripple for the bulk-driven sixth-order filter is shown in the Figure 42. It clearly shows that it has ripple fluctuating in around 1dB. We can determine the order of the filter to be n=6 from the pass band ripple.

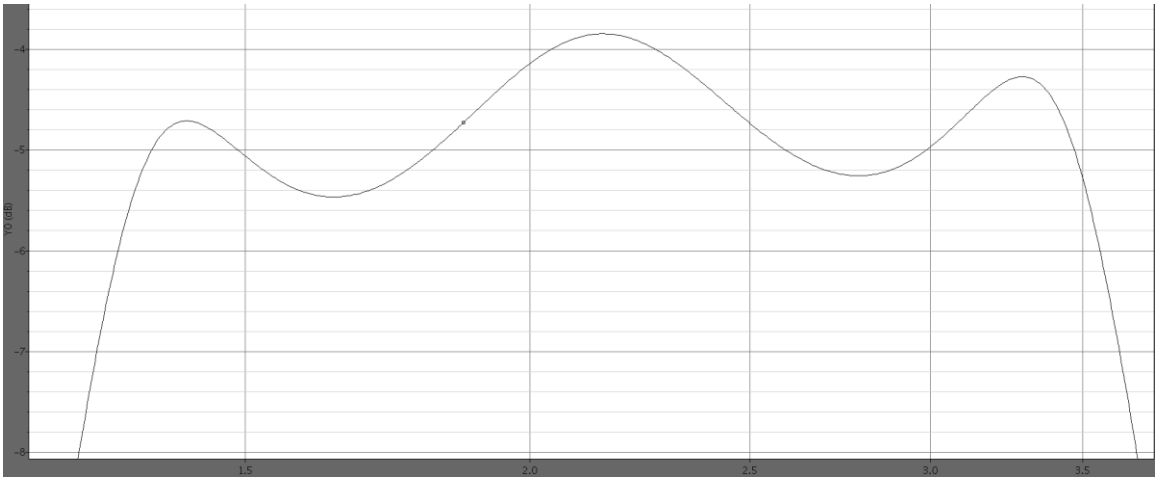

Figure 42 Pass Band Ripple of 1dB for BD Sixth-Order Filter

CHAPTER 5 SIMULATION RESULTS

5.1 Simulating CTCM Differentiator Circuit in Cadence:

DC analysis is one of the primary analyses that are often performed to check the conditions of any analog circuit. This analysis estimates the bias conditions over a range of values through sweeping voltages or current variables, temperature conditions for each and every model parameter all the devices present in a circuit. This analysis provides a better understanding of the voltage or current transfer characteristics (VTC or ITC) of a transistor and thereby a better understanding of the behavioral changes in the devices.

Transient analysis is also another analysis that is extremely important to determine the state of the circuit under signals that are non-well-behaved. A better understanding on the stability of a circuit can be obtained during this analysis if and whether a circuit oscillates while performing this analysis. Effects such as non-linear distortion, intermodulation, saturation, clipping, and oscillations can be modeled through this analysis. The general source waveforms selected for transient analysis are sinusoidal, pulse, exponential, piece wise, linear. Any other kind of waveforms can also be used during this transient analysis based on the circuit conditions. In this design, sine wave as an input with V_{in} = 500 mV is used. The input and output wave forms for the transient analysis performed are shown in the Figure 43.

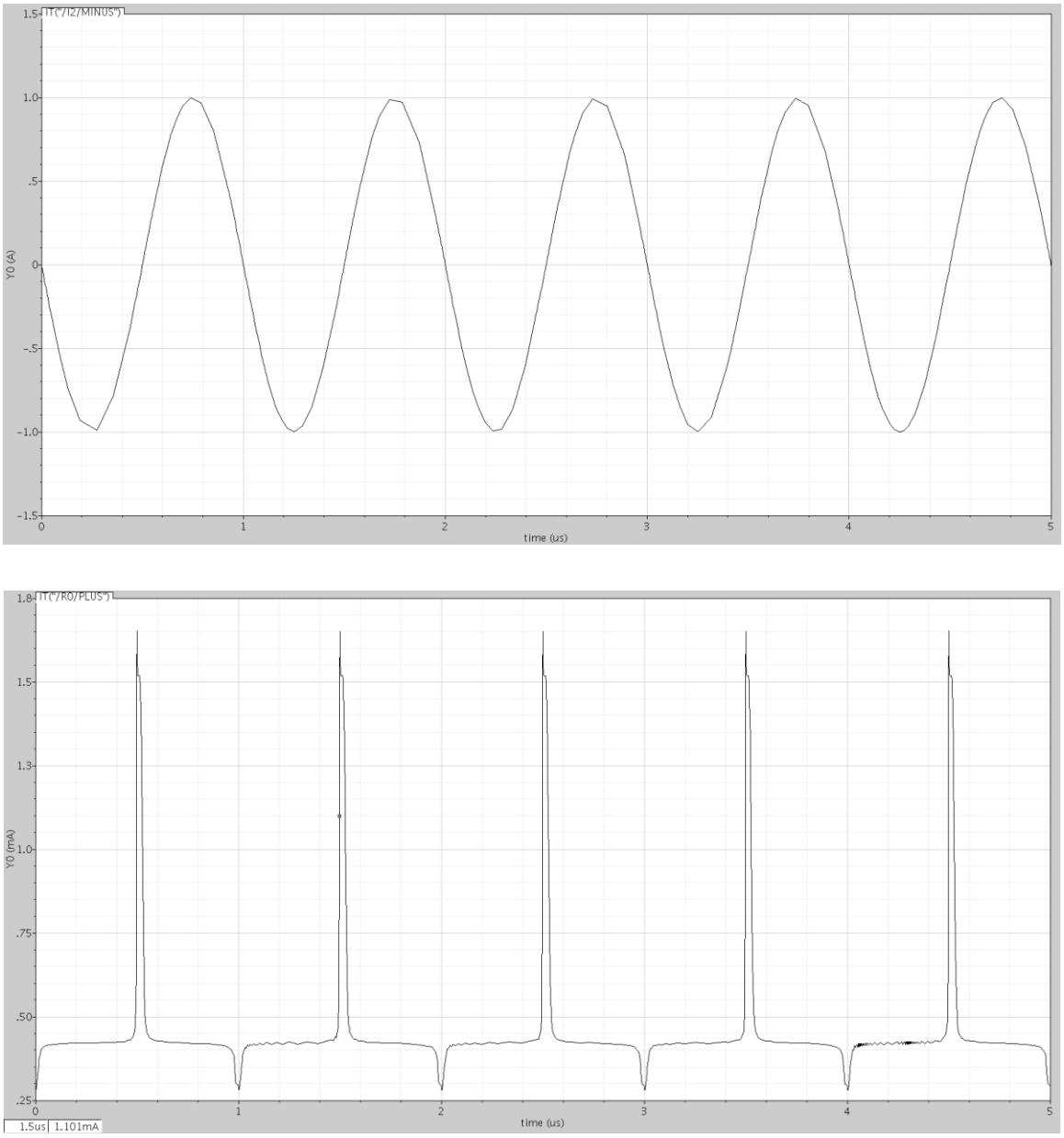

Figure 43 (a) Input Waveform (b) Output Waveform

It is clear from the output wave that the phase shift of the circuit is 90 degrees maintaining the functioning of differentiator. The output wave form shows that the circuit developed can be stable even under non-well-behaved signals.

AC analysis is also very important analysis for any analog filter design. This analysis is performed to simply figure out the behavioral analysis of the circuit when well-behaved ac signals are applied as its inputs. The frequency and phase response of the circuit can be plotted through this analysis. The node voltages and the bias conditions that are to be set are estimated through DC analysis. When an input signal is applied to the circuit, a change in the DC bias points can be seen and the small signal model is dependent on this DC bias point's in-order for the circuit to be stable. The bandwidth, cut-off frequency, gain, dissipation factor etc. for the circuit are obtained from the AC analysis.

5.2 Monte Carlo Analysis

Monte Carlo analysis is a very essential statistical analysis for any filter design. Monte Carlo analysis calculates the response of the filter when the device parameters are changed randomly within the limited tolerance limits of each and every device present in a circuit. It measures the response of the same circuit numerous times by assigning a random value for each and every device within a tolerance level. The purpose of doing this analysis is that the resistors, capacitors or transistors will not have the ideal theoretical values when implemented practically. For example, the resistor of 1KΩ with a tolerance of 1% in reality might produce anywhere between 990Ω to 1010Ω and this is the same case with all the other components. Therefore, Monte Carlo analysis is performed to simulate the same circuit for 100 or 1000 times by varying the values of every component within practical limits to get a better understanding of the circuit. Higher the number of simulations, more accurate the results produced to determine the sensitivity of circuit.

5.2.1 CTCM Gate-Driven Cascade Sixth-Order Chebyshev Band Pass Filter

The sensitivity performance of the designed filter using gate-driven differentiator is determined by performing Monte Carlo simulation in Cadence, and the generated data points are simplified using Microsoft Excel. Assuming all the capacitances are highly correlated with each other a Monte Carlo analysis is performed for 100 runs by randomly changing the values of the devices within their tolerance. The cumulative result obtained for these 100 simulations is shown in the Figure 44.

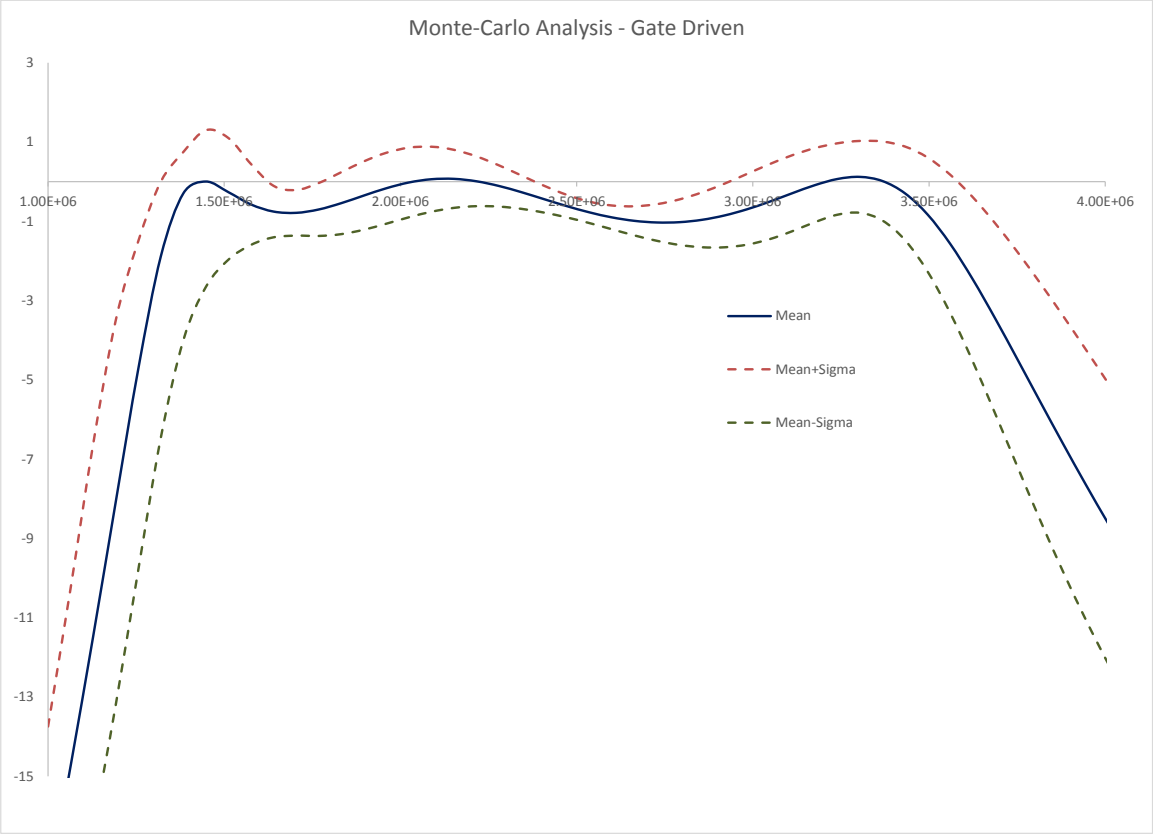

Figure 44 Sensitivity Analysis for CTCM Gate-Driven Sixth-Order Filter

Table 12 Monte Carlo Analysis Values for CTCM Gate-Driven Filter

Frequency (MHz)	Mean (dB)	Mean + Sigma (dB)	Mean – Sigma (dB)
1.19	-8.081	-3.5	-13.2
1.38	-0.2931	0.75	-3.99
1.45	3.93E-03	1.3	-2.65
1.96	-0.165	0.729	-1.059
2.22	0.01	0.63	-0.61
2.60	-0.9	-0.62	-1.35
3.05	-0.50	0.44	-1.44
3.18	-0.08	0.84	-1.02
3.88	-6.60	-3.38	-9.82

It can be seen from the output graph and the tabulated values in Table 12 that the design is sensitive to variations within the device values assigned. The obtained results show that the gate-driven design achieves satisfactory sensitivity report.

5.2.2 CTCM Bulk-Driven Cascade Sixth-Order Chebyshev Band Pass Filter

The Monte Carlo analysis is performed for this circuit with the specifications used for the above design. The accumulated sensitivity analysis for 100 simulations is shown in the Figure 45.

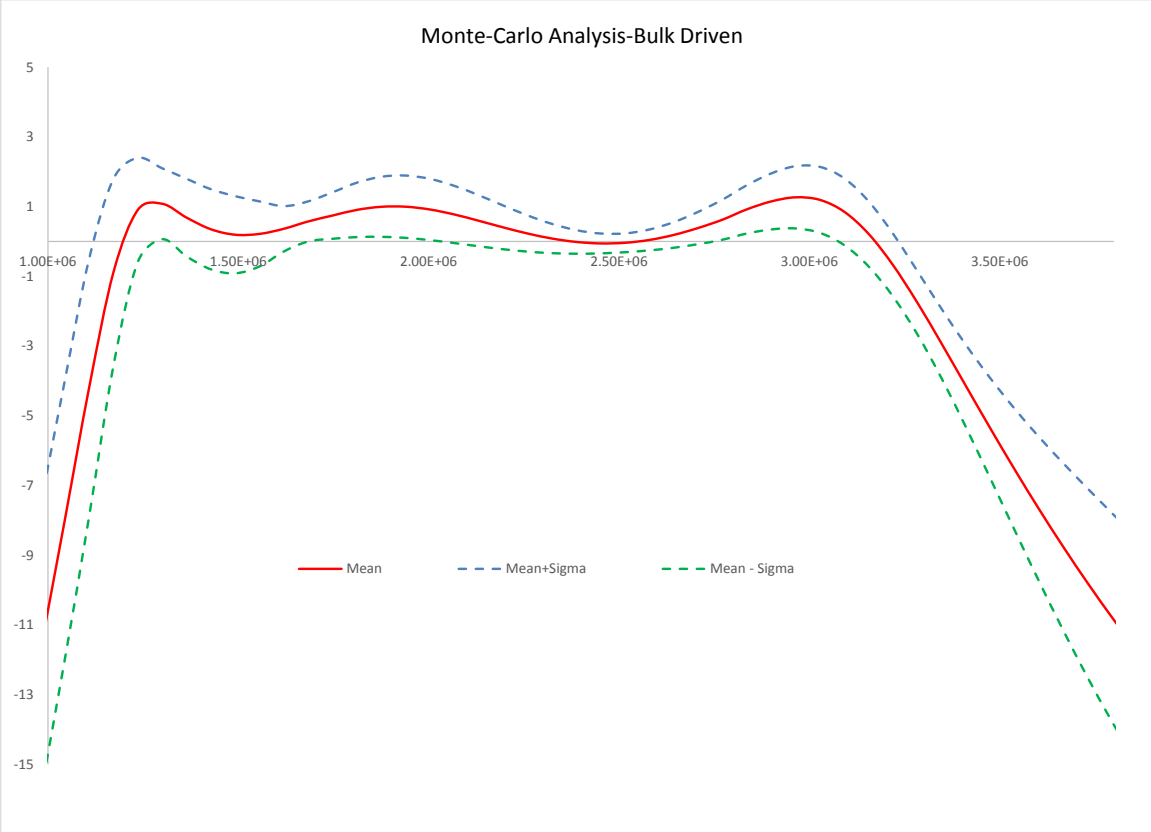

Figure 45 Sensitivity Analysis for CTCM Bulk-Driven Sixth-Order Filter

Table 13 Monte Carlo Analysis Values for CTCM Gate-Driven Filter

Frequency (MHz)	Mean (dB)	Mean + Sigma (dB)	Mean – Sigma (dB)
1.17	-0.87	1.8	-3.55
1.36	0.68	1.8	-0.42
1.56	0.21	1.15	-0.71
1.75	0.74	1.41	0.07
2.0	0.91	1.79	0.03
2.52	-0.03	0.23	-0.3
3.03	1.19	2.14	0.24
3.16	0.21	1.15	-0.71
3.8	-10.79	-7.79	-13.78

From the analysis of both the designed filters, that the sensitivity performance can be seen as nominal. To achieve much better sensitivity performance, the circuit can be designed using Follow the Leader (FLF) or Inverse Follow the Leader (IFLF) feedback methods.

5.3 Tuning

The major disadvantage of the continuous-time higher order filters is the on-chip tuning. It is often very difficult to change the component values with respect to the time and temperature practically once a circuit is designed. So, tuning structure is a must for any analog design before it is manufactured. For the proposed differentiators two types of tuning possibilities exist. The first one is to change the supply voltage (V_{DD}). Any change

in the supply voltage changes the drain current (I_D) of the transistors in the design. But the change in the voltage should be carefully tuned in a way that it produces a change in the input resistance and thereby causing the RC time constant to change. This procedure is often difficult to tune accurately and the least practical way of tuning. The second way is to introduce a small supply voltage only to input transistors at the gate terminal thereby changing the bias conditions accordingly. In this way the input resistance of the circuit can simply be varied resulting required change in the RC time constant. In this procedure, we can tune the circuit easily for the application of any filter design.

CHAPTER 6 CONCLUSIONS

6.1 Summary of thesis

The major motive of this thesis is to design a current-mode analog filter that can be operated at low supply voltage achieving the factors of low power consumption, higher gain, good dynamic range and better sensitivity. Voltage-mode integrators consisting of operational amplifiers are generally used for analog filter designs that often have higher power consumption. Now-a-days, it is difficult to achieve design requirements with all the factors mentioned using voltage-mode integrators. Due to the obvious limitations of voltage-mode integrators, this thesis provided an alternative current-mode differentiator due to its advantages mentioned in chapter 3. As the differentiator designed in current-mode, it is rather a simple circuit with current mirrors and no op-amps and resulted in higher gain, dynamic range, good PSRR and very good power efficiency.

Bulk-driven technique has been used in the design that boosted the power efficiency multiple folds and at the same time made the design more efficient and flexible for rapid scaling in CMOS technologies. Detailed operation of both the GD and BD differentiators were analyzed in different regions and presented in the earlier chapters. An optimized design that works with a low supply voltage of 0.7 V is presented. The supply voltage for the differentiators is set to 0.7 V which is very close to the sum of PMOS and NMOS transistors 0.339 V and |-0.351 V| respectively in TSMC 65nm technology. The GD, BD differentiator achieves a gain of 172.743 dB, 176.483 dB and power consumption of 192.5 uW, 657.37 nW respectively. The PSRR for the GD differentiator is -57.75 dB whereas for BD differentiator we achieved a satisfactory value of 47.51 dB.

A second-order filter using these both gate-driven and bulk-driven differentiators was developed to determine the flexibility and capability of the design. The operation of the filter design and the simulations obtained from TSMC Cadence 65nm technology are presented in chapter 4. The power consumption of gate-driven second-order filter was determined as 675.4 uW and the bulk-driven second-order filter can be operated with a

power consumption of 122.7 uW. The advantages of the GD and BD current-mode differentiators in higher order filter application are presented by designing a sixth-order Chebyshev band pass filter that can operate at low supply voltage compared to the conventional filter designs through the use of integrators.

The sixth-order filter with cascade topology is implemented using the second-order GD and BD differentiator building blocks. A Monte Carlo analysis is performed to check the sensitivity of the transfer function when subjected to physical variation. The sixth-order Chebyshev band pass filter was designed with a pass band of 2 MHz and 1 dB pass band ripple. The upper stop band attenuation is determined as 80 dB and the lower stop band attenuation will be 360 dB and the transfer function is designed with the procedure mentioned in chapter 2. The sensitivity results obtained from Cadence are demonstrated in chapter 5. The power consumption of the total sixth-order GD and BD differentiator circuit is 10.1942 mW and 1.4518 mW respectively which are far better than the conventional designs.

This work titled "**Low-Power and Low-Voltage Bulk-Driven Continuous-Time Current-Mode Differentiator Filters**" has been accepted and published in *18th International Conference on Electrical and Nuclear Engineering (ICENE), 2016, Lisbon, Portugal*.

6.2 Performance Comparison Table

Table 14 A detailed performance comparison of the novel BD-differentiator circuit with other existing designs

Parameter	[This work] GD 2016	[This work] BD 2016	[63] 2014	[65] 2007	[64] 2007	[66] IBF 2004	[66] DBF 2004
Process	65nm	65nm	130nm	180nm	65nm	Spice	Spice
Voltage	0.7 V	0.7 V	1.2 V	2.5 V	1.2 V	1.5 V	1.5 V
Order	6	6	6	7	3	2	2
Pass band	2 MHz	2 MHz	256 MHz	650 MHz	1.1 MHz	135 KHz	150 KHz
F_C	2.5 MHz	2.5 MHz	256MHz	650 MHz	1.1 MHz	205 KHz	204 KHz
Gain	0-64 dB*	0-64 dB*	0-60 dB	NA	0-50 dBA	NA	0-28 dB
PC	10.19 mW	1.45 mW	46mW~ 55mW	370 mW	12.3 mW	325 mW	12.24 mW

GD – Gate-Driven, BD – Bulk-Driven, IBF – Integrator Based Filter, DBF – Differentiator Based Filter, F_C – Cut-off Frequency, PC – Power Consumption

* To demonstrate the gain of the circuit, the following response is shown in the Figure 46.

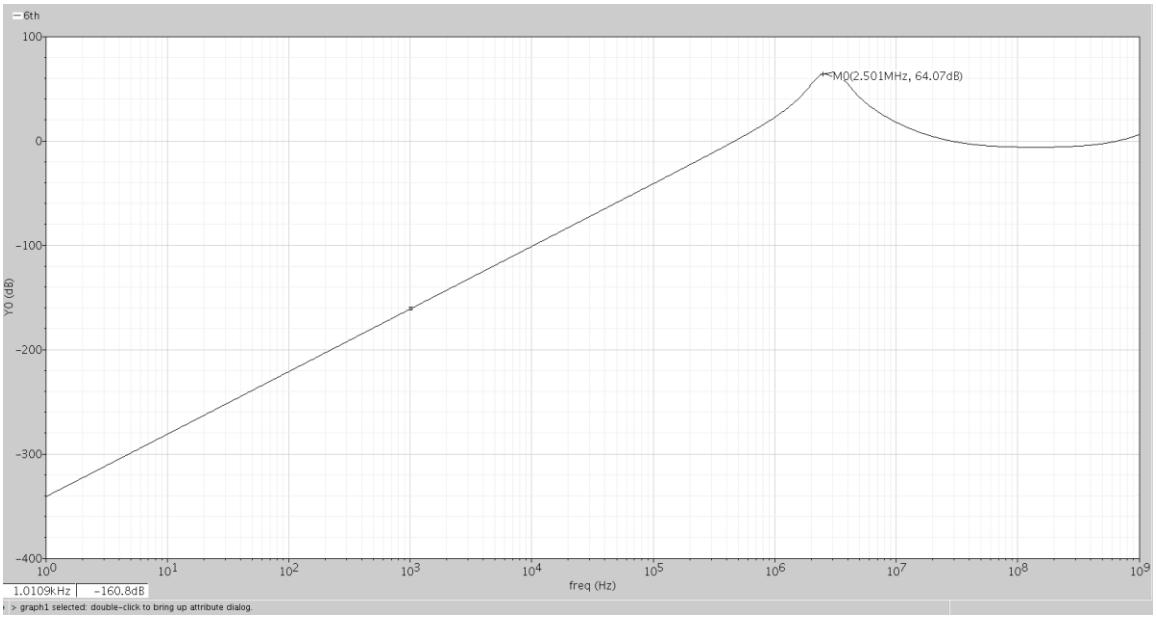

Figure 46 Magnitude Response Measuring Gain of the Circuit

6.3 Future work

One of the major disadvantages of bulk-driven circuits is that they exhibit large noise factors. In this research work, the noise of the BD circuit is higher compared to GD circuits. So, the noise factors present in BD MOSFET circuits needs to be analyzed with a detailed understanding of noise mechanism in Nano-scale BD circuits, for example contributions from aspects such as leakage currents and flicker noises etc. and an optimized design with noise suppression can be introduced.

As the current designs demand low supply voltage, the supply voltage can further be minimized beyond 0.7 V through the use of dynamic threshold voltage MOSFET (DTMOS) transistor. As reported in [56], [57], DTMOS transistors are used to increase ICMR of the circuits even under smaller supply voltages. In order to implement this transistor to Nano-scale technologies, the characteristics and the detailed behavior of the DTMOS transistor in different regions should be examined. Moreover, BD techniques can be implemented with the combination of other LVLP techniques such as self-cascode, floating-gate, quasi floating-gate etc. A BD self-cascode structure [58] and BD

quasi floating-gate structure [59] are currently under investigation to be applied in LVLP applications.

The designed filters in this thesis are partially sensitive to component variations as presented in chapter 5 and the reason being the cascade topology used. This limitation can potentially be addressed through designing the filter with different multiple loop feedback (MLF) [60], [61] methods that can definitely improve the sensitivity performance. The most popular MLF methods being proposed through this work are Follow-the-Leader (FLF) [62] and Inverse Follow-the-Leader (IFLF) topologies. These proposed designs using FLF and IFLF methods are shown in Figure 47 and Figure 49

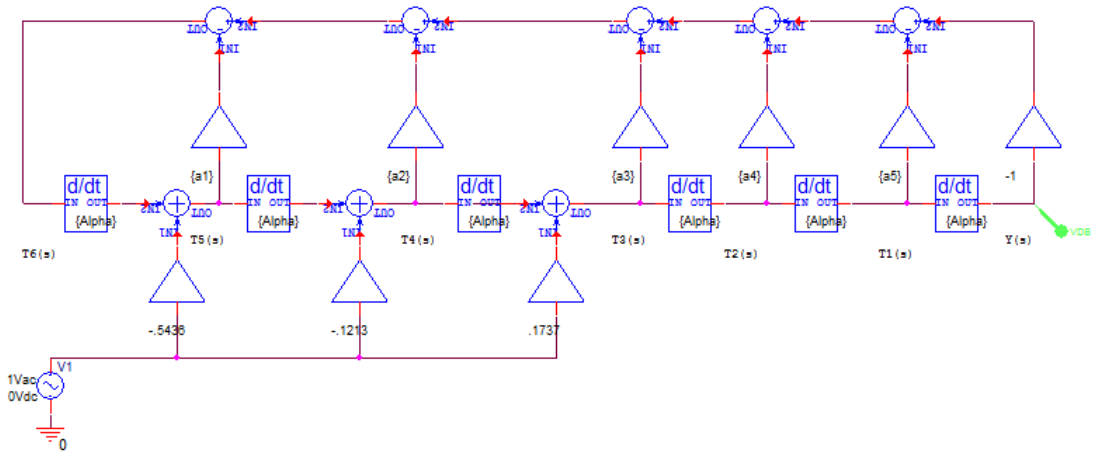

Figure 47 Sixth-Order FLF with Input Distribution Topology Using Differentiators

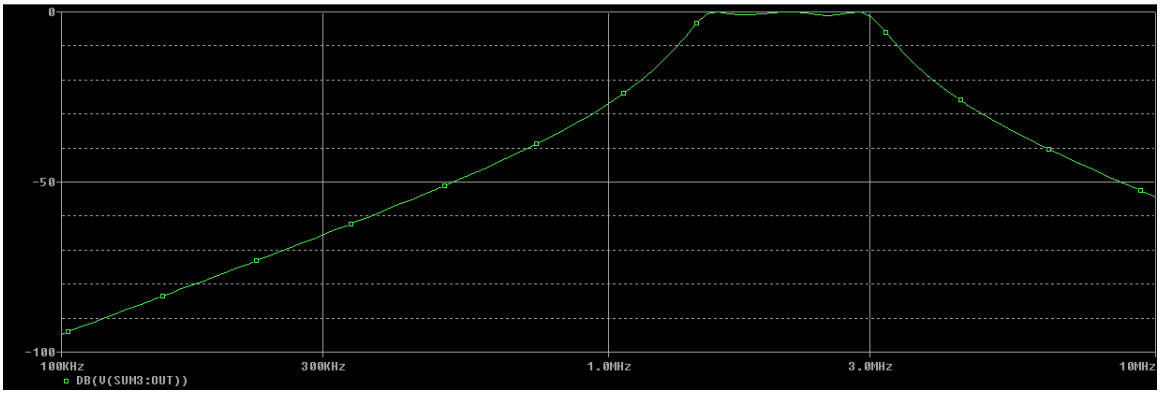

Figure 48 Magnitude Response for Sixth-Order Chebyshev Band Pass Filter for FLF Topology using Differentiators

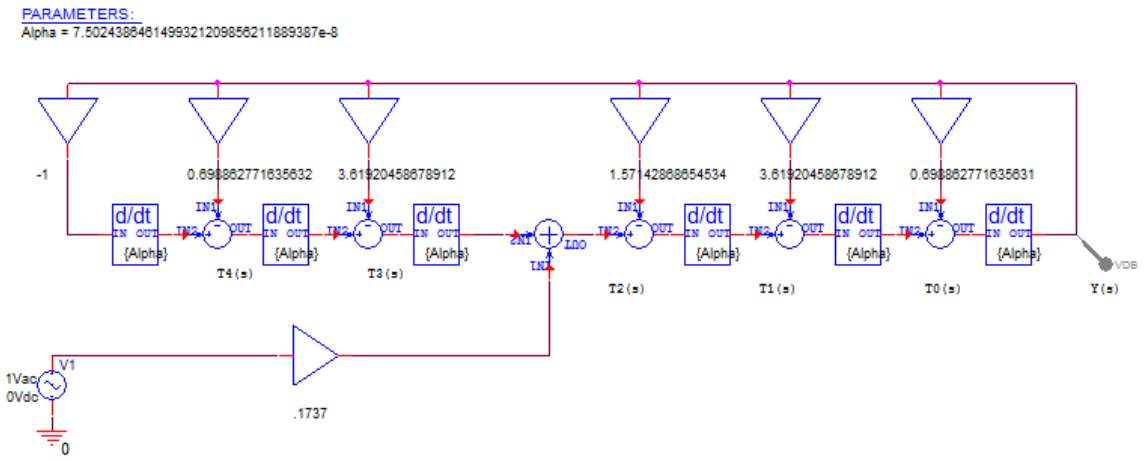

Figure 49 Sixth-Order IFLF with Input Distribution Topology Using Differentiators

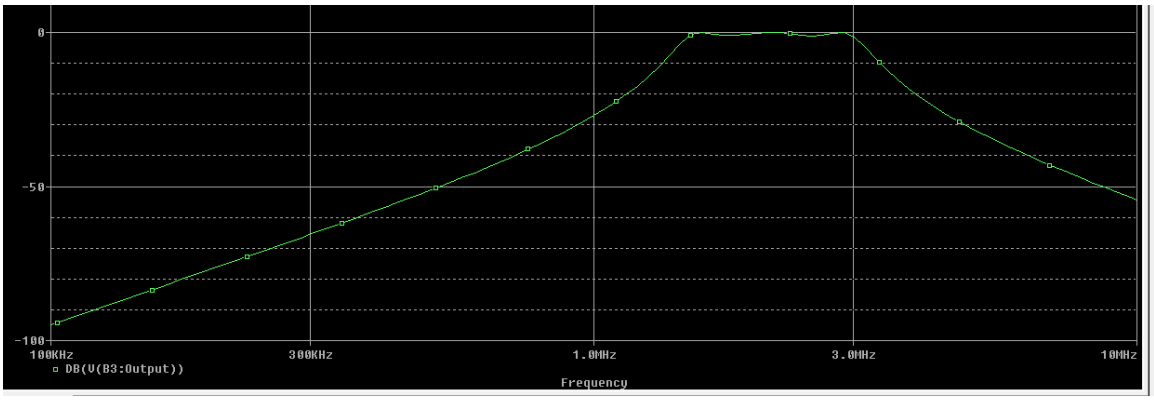

Figure 50 Magnitude Response for Sixth-Order Chebyshev Band Pass Filter for IFLF Topology using Differentiators

These proposed topologies using differentiator are designed using Spice software and the values for the architecture are realized using the same sixth-order chebyshev band pass transfer function mentioned in chapter 4. The simulated magnitude response graphs from Spice are shown in Figure 48 and Figure 50. These designs can be further realized and investigated in transistor level simulations that can earn very positive and accurate results.

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