# A Self-Healing Technique Using ZTC Biasing for PVT Variations Compensation in 65nm CMOS Technology

by

Hamidreza Nateghi

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# DEDICATION

*This Thesis is dedicated to my lovely parents, Gholamreza and Hoda, to my older brother, Alireza, and to my beautiful wife, Najmeh for their endless support, inspiration, encouragement and love.*

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# ABSTRACT

This thesis proposes a digital oriented self-healing technique in 65nm CMOS technology for current sources by biasing the current reference transistor in the vicinity of the Zero Temperature Coefficient (ZTC) point. This method, utilizes MOSFET self-heating in order to determine bias point position with respect to the ZTC point and converge the bias point to the vicinity of the ZTC point. As the result, process, voltage, and temperature are compensated for significantly. The ZTC point existence in 65nm scale has been proven to exist below the nominal supply voltage. A circuit level modeling of the effect of self-heating and current change with temperature is proposed in this work to allow the simulation of the circuit using transient analysis in the Spectre simulator environment. The proposed self-healing circuit is applied to current sources biasing two common analog and digital applications and the simulation results of the self-healed applications are discussed.

# LIST OF ABBREVIATIONS USED

| | |
|---|---|
| ZTC | Zero Temperature Coefficient |
| PVT | Process Voltage Temperature |
| CMOS | Complementary Metal Oxide Semiconductor |
| IC | Integrated Circuit |
| OCV | On-Chip Variation |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| DC | Direct Current |
| MC | Monte Carlo |
| TIA | Transimpedance Amplifier |
| AC | Alternative Current |
| DAC | Digital to Analog Converter |
| SOI | System On Insulator |
| LHP | Left-Hand Plane |

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# 1. Chapter One: Introduction

## 1.1 Motivation

In recent decades, the majority of Integrated Circuits (ICs) have been manufactured using CMOS technology because of low power consumption and better noise margin in comparison with other technologies. Also, since most fabrication facilities use CMOS process, it is considered a cheap fabrication technology [1].

As the pace of Integrated Circuit scaling follows Moore's law, CMOS technology is being scaled down [2] in order to increase speed, reduce supply voltage, and keep power consumption at an acceptable level. Nevertheless, despite integration in digital circuits, this evolution has not been very beneficial in analog circuits [3]. Since scaling down comes with reducing channel length in CMOS technology, complexity in ICs has increased and many inevitable complicated issues have risen. One of the most critical problems is that devices in submicron or further technologies will have higher variation sensitivity. The variation of some parameters throughout a single chip is On-Chip Variation (OCV). These variations consist of process, voltage and temperature variations. Therefore, they are also called PVT variations. Because of variations throughout manufacturing conditions, there are resulting process variations. Voltage supply variations cause variation in saturation current and hence in propagation delay. Also when a circuit or chip is operating, power consumption in MOSFET due to leakage, short circuit and switching varies temperature through the chip [1]. PVT variations impact

different characteristics of analog circuits which depend on the application of the circuit. For example, output resistance of a current mirror [4] or delay in a current-starving inverter is highly dependent on these variations.

So far, different techniques and implementations have been proposed in order to compensate for process, voltage and temperature variations. Some of these papers have proposed ideas to compensate for all of these variations for specific applications [16]. Some of these circuits have been designed only to compensate for temperature variations by using biasing circuits that provide constant voltage, current or transconductance in a specified temperature range and they are almost temperature-independent [5]. There are also techniques that compensate for temperature variations by biasing a transistor in the vicinity of its Zero Temperature Coefficient (ZTC) point [11]. Although research has been done in order to minimize variations of MOSFET characteristics owing to MOSFET Self-Heating [17], transistors were still sensitive to ambient temperature variation. In [6] and [7] only process variations are compensated for requiring trimming, calibration or self-tuning. There are also process compensation designs in which feedback loops have been used. However, accuracy of direct current (DC) references in the feedback loops is very important, since they take advantage of highly accurate references at the input of comparator blocks in order to enhance accuracy of parameters of circuits [8]. On the other hand, there are proposed circuits to generate constant biasing sources independent of both temperature and process variations [9]. But even having constant sources does not guarantee that once they are connected to the biased circuit, they will keep their constant values. Recently, methods of process and temperature compensation have been published, in which adaptive biasing is used in a way that biasing circuit variations and

some of the biased circuit's parameters are compensated for mutually and do not necessarily have a constant magnitude [10]. Yet, it might be needed to design a specific adaptive biasing circuit for every specific application.

In this Thesis, a technique of PVT variation compensation has been proposed in order to design a supply and temperature independent current source with a closed-loop feedback for self-healing. To compensate for temperature and supply variations, the biasing circuit is designed in a way that the transistor DC point is converged to the vicinity of the ZTC point. The circuit has a feedback loop to keep the bias point close to the ZTC point. The calibration loop uses ambient temperature variations' sign due to MOSFET self-heating as the signal for calibrating the current (or voltage) source. Keeping the biasing point at the vicinity of the ZTC point does not compensate for process variations of the power source, but significantly degenerates them.

## 1.2 Objective

Based on the literature review and discussion about the recent techniques which are suggested to compensate for PVT variations as much as possible, and also considering their pros and cons, the goals of this thesis are:

- To study the existence of the ZTC point in 65nm CMOS technology similar to what has been done in previous technologies and using this inherent property of MOSFETs in this technique.
- To propose a PVT compensation technique making it possible to have dynamically calibrated current sources for a wide range of low voltage analog/digital applications.

- To analyze the accuracy of the circuit and its relation with the components' parameter to be able to reduce the ZTC biasing error.
- To design a simple model for MOSFET while considering the impact of self-heating on ambient temperature and transistor bias point.
- To integrate this technique in analog and digital applications such as current-starved inverters and current mirrors and compare the simulation results with the uncompensated applications.

## 1.3 Contributions

The contributions in this thesis are mentioned below:

- The existence of the ZTC point in 65nm scale has been proven to exist below the nominal supply voltage.
- A digital oriented self-healing technique for current sources is proposed in 65nm CMOS technology by biasing the current source transistor in the vicinity of the Zero Temperature Coefficient (ZTC) point.
- A circuit level modeling of the effect of self-heating on the ambient temperature is proposed in this research.
- A Verilog-A block for current change with temperature is proposed in order to allow the simulation of the circuit using transient analysis in the Spectre simulator environment.
- The process variations degeneration with biasing a current source transistor in the vicinity of the ZTC point has been proven.

## 1.4 Organization

This Thesis is organized as follows:

In chapter II, PVT variations are introduced. Power sources and their importance in low voltage integrated circuits are discussed. Then, self-heating phenomenon and Zero Temperature Coefficient (ZTC) in MOSFETs are explained. Finally, there is a review of some recent PVT compensation methods.

In chapter III, the designed circuit is illustrated. The technique functionality, along with mathematical equations from which models are derived are discussed.

In chapter IV, self-healing circuit is applied to two common applications. The simulation results are shown and compared, and the efficiency of the proposed technique is discussed.

Chapter V contains conclusion and considerations for future works on this technique helping later designs to be more accurate, more efficient and to have less power consumption.

# 2. Chapter Two: Sources and MOSFETs

## 2.1 PVT in CMOS Technology

### 2.1.1 Process Variations

PVT variations have always been an issue in IC design. In ITRS 2011 [20], it is mentioned that one of the key problems that designers are facing is the increase of variability of design-related parameters due to shrinking of feature sizes. This variability comes from variation of fabrication parameters or from intrinsic atomic nature.

Through manufacturing process, relative fluctuations increase in transistor dimensions since reducing absolute deviation is not as easy as shrinking the feature sizes.

Variations in Length (L) and Width (W) of a transistor affect transistor drive current because the current is proportional to W/L. Channel length fluctuations change threshold voltage, consequently shifting the drive current. Also, channel variations across the width are random [30].

There are other features which their variations increase through the fabrication process by shrinking feature sizes. For example, carrier concentration change in channel shifts threshold voltage. In recent technologies, mismatch in integrated circuits has increased due to random dopant fluctuation. Also in technologies below 30nm, gate oxide thickness ($t_{ox}$) variation significantly affects threshold voltage [30].

It is common to categorize process variations into global and local variations. Global variations parameters change equally for all transistors, such as oxide thickness or

dopant concentration. In contrast, local variations, also known as mismatch, affect each transistor differently. Variation of physical parameters through the fabrication process leads to variation of electrical parameters like $V_{th}$ or $C_g$ which will affect both analog and digital circuits' performance.

#### 2.1.1.1 Global Variations

There are different analyses for global and local variations. Monte Carlo (MC) analysis and corner analysis are typically used to evaluate the impact of global variations. Since Monte Carlo simulations are computationally thorough and hence they are time-consuming and hardly applicable for large designs, corner simulations are used instead. The corners represent extreme cases. Process fluctuations increase the drive current of a transistor in a fast corner and it slow it down in a slow corner. In addition to fast and slow corners, there are also cross corners which have NMOS with maximum speed and PMOS with minimum speed and vice versa. Although cross corners are not very critical in digital circuits, they are usually very critical in analog circuits. Figure (2-1) shows a basic current mirror circuit designed in 65nm technology.

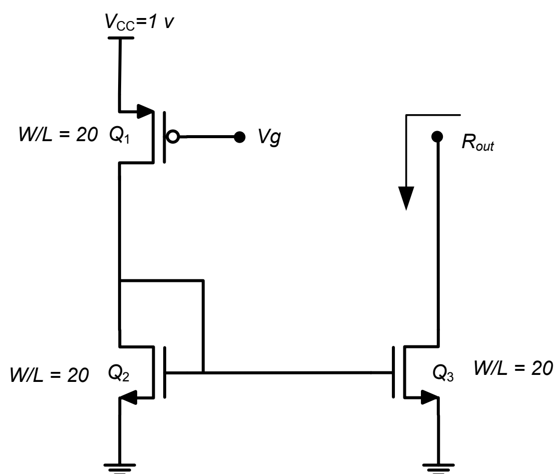


Figure 2-1) Schematic of a typical current mirror

In Figure (2-2) and Table (2-1), simulation results of the Monte Carlo Analysis and the Corner Analysis have been plotted respectively to show process variations impact on the circuit parameters of current mirror in Figure (2-1).

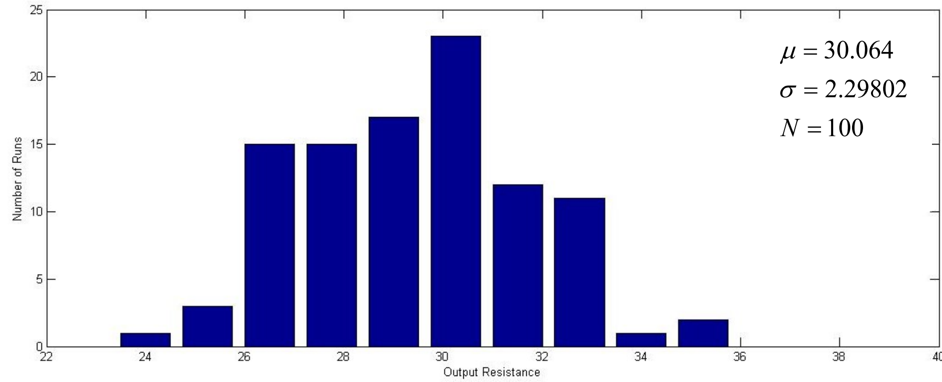


Figure 2-2) Monte Carlo analysis: Histograms of the current mirror output resistance

Table 2-1) Corner analysis: Current mirror output resistance in different corners

| Corner | SS | FS | TT | SF | FF |
|---|---|---|---|---|---|
| Output Resistance ($k\Omega$) | 38.97 | 31.33 | 29.72 | 28.45 | 23.17 |

#### 2.1.1.2 Local Variations

Local variations are increasing due to technology scaling in CMOS technologies. The reason is with decreasing transistor dimensions, the standard deviation of threshold voltage $\sigma_{\Delta V_T}$ and current factor $\sigma_{\frac{\Delta K}{K}}$ ($K = \mu_n C_{ox} \frac{W}{L}$) are increasing since we know that:

$$\sigma_{\Delta V_T} = \frac{A_{\Delta V_T}}{\sqrt{WL}} \qquad (2\text{-}1)$$

$$\sigma_{\Delta V_T} = \frac{A_{\frac{\Delta K}{K}}}{\sqrt{WL}} \qquad (2\text{-}2)$$

$A_{\Delta V_T}$ and $A_{\frac{\Delta K}{K}}$ are matching parameters coming from a particular process and manufacturing line.

### 2.1.2 Voltage Variations

Fluctuations in supply voltages are mainly caused by IR drop and di/dt noise where IR drop is due to the current flow over the parasitic resistance of power grid, while $d_i/d_t$ noise is caused by parasitic inductance in combination with capacitance and resistance of power grid and IC package.

The voltage bounce $\Delta V_{IR}$ is determined by Ohm's law and it can be written as:

$$\Delta V_{IR} = R_{grid} \times i_{(t)} \tag{2-3}$$

And voltage bounce $\Delta V_{\frac{di}{dt}}$ can be defined as [30]:

$$\Delta V_{\frac{di}{dt}} = L_{Parasitic} \times \frac{di}{dt} \tag{2-4}$$

The sum of both effects can lead to voltage drop or voltage overshoot.

Offsets in a voltage regulator as another source of fluctuations can cause deviations from nominal supply voltage, which can be either caused by voltage regulator inaccuracy or by voltage reference circuit.

Figure (2-3) illustrates output current variations of current mirror depicted in Figure (2-1) due to temperature change for different supply voltages, which shows that output current thermal sensitivity is changing with supply voltage variations.

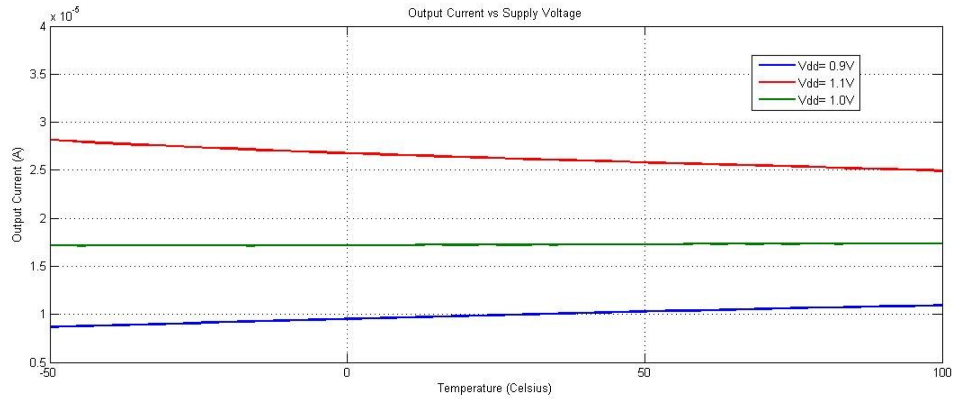


Figure 2-3) Current mirror output current variation with temperature for different supply voltages

### 2.1.3 Temperature Variations

The dissipated power changes the temperature of a chip due to thermal conductivity that causes temperature variations. Ambient temperature changes also lead to changes in chip temperature. Since threshold voltage and carrier mobility in MOSFET are highly temperature dependent, circuit performance is influenced by temperature variations.

Increase in temperature usually slows down circuits as a result of reduced carrier mobility and increased internal resistance. However, for low $V_{DD}$, since circuits are operated in temperature inversion, the impact of threshold voltage exceeds mobility degradation and, as a result, circuit speeds up by increasing temperature (Figure 2-4).

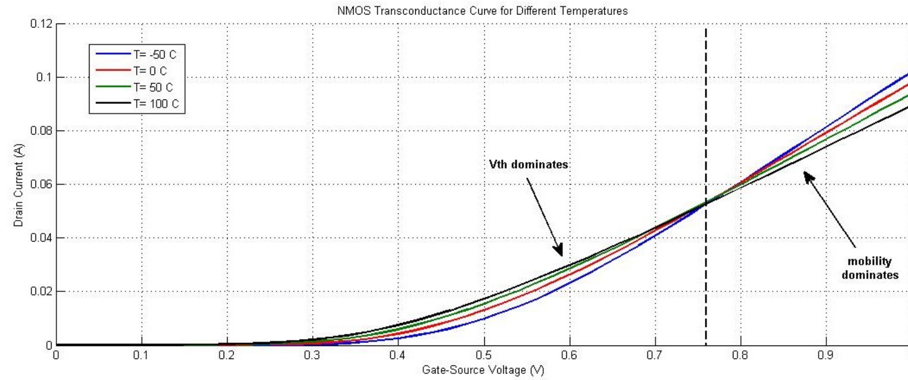


Figure 2-4) NMOS transconductance curve for different temperatures

Since for low $V_{DD}$, threshold voltage dominates and for high $V_{DD}$, Carrier degradation does, there is a point called the Zero Temperature Coefficient (ZTC) in which voltage and current of transistors are independent of temperature. In next section, the ZTC point and its characteristics are explained. The figure below (Figure 2-5), shows the output resistance variations of the current mirror from Figure (2-1) due to temperature change with different gate voltages.

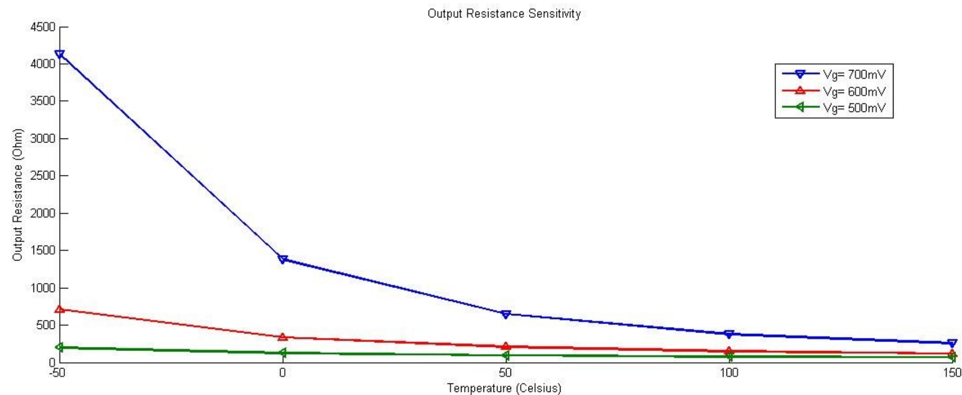


Figure 2-5) Current mirror output resistance variation with temperature for different gate voltages

Each kind of variation has a different time constant. The shorter the time constant of a variation, the more challenging the voltage and current adaptation. Figure (2-6) categorizes PVT variations based on their time constants [30].

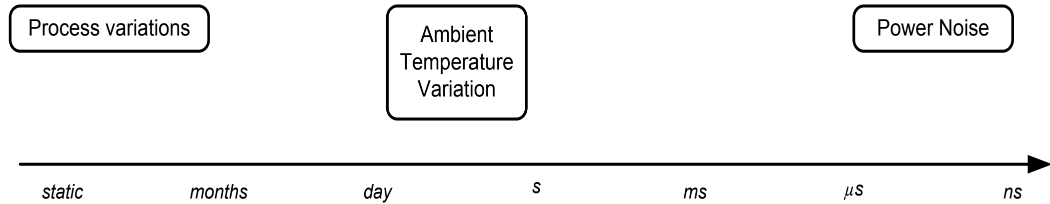


Figure 2-6) Temporal classification of PVT variations

## 2.2 Power Sources

Circuits are unable to operate properly without biases and references. Both Power consumption and speed are affected by power sources [12]. Thus, appropriate design of power sources is very important. Generally there are two kinds of power sources: current sources and voltage sources:

### 2.2.1 Current Source

Simply, a current source, or a current reference, can be defined as a source of constant current which current value is independent from the load it is connected to. Usually in analog circuits, current in circuits result from the mirroring of one or more current references. Most of the blocks in a circuit use at least one current reference. Since current controls the transconductance of a transistor, it can be said that current references impact both static and dynamic properties of circuits. Therefore, designing current references with the required accuracy and PVT variations' independency is one of the most important parts of any integrated circuit.

So far, there are many different configurations suggested in order to have a current reference as accurate and independent as possible. Mentioned in [12], the simplest technique to have a current reference is to use a load resistor generating the desired

current based on Ohm's law, which will be injected into a diode connection, providing a useful voltage for current mirroring (Figure 2-7).

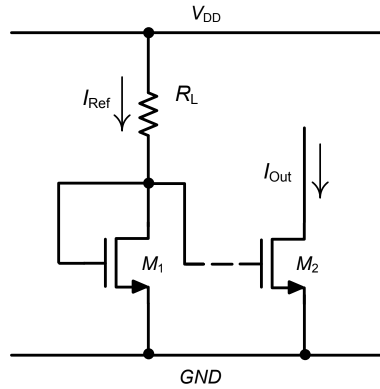


Figure 2-7) Load resistor as a current reference

Current generated through this method generally has a very poor accuracy. It can be written as:

$$\left(\frac{\delta I_{ref}}{I_{ref}}\right)^2 = \left[\frac{\delta(V_{DD} - V_{GS_1})}{V_{DD} - V_{GS_1}}\right]^2 + \left(\frac{\delta R_L}{R_L}\right)^2 \qquad (2\text{-}5)$$

In (2-5), $V_{DD}$, $V_{GS}$ and $R_L$ are dependent on PVT variations. Also, since resistor is power consuming in integrated technologies and it is not used much, with a very simple modification, the resistor can be replaced by a PMOS transistor shown below:

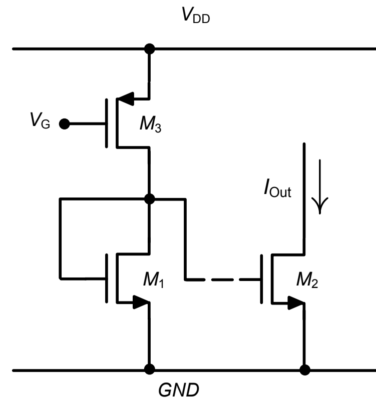


Figure 2-8) Biased PMOS as a current reference

By applying enough voltage to the gate of the transistor $M_3$, constant current flows through the transistor and it will function as a current reference. Yet, because of PVT dependency of MOSFET characteristics, it cannot be a very accurate current reference.

### 2.2.2 Voltage Source

There are many ways to have voltage sources or voltage references in analog circuits. By having a supply voltage typically with two connecting pins as $V_{DD}$ and GND, many schematics have been proposed to implement a voltage reference as accurate as possible with minimum PVT dependency. The simplest voltage reference is a fraction of the supply voltage generated by a voltage divider. But the voltage reference will be essentially dependent on the power supply which is not desired. Another simple voltage reference, which achieves this feature, is to use the voltage across a diode-connected

transistor biased by a current reference. Here, the dependency of the voltage reference is as a result of possible non-ideal behavior of the current reference [12].

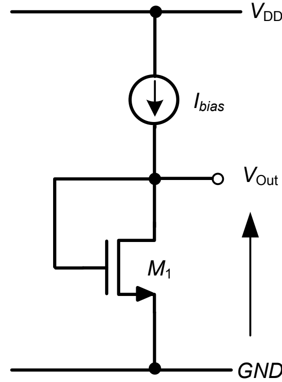


Figure 2-9) Diode-connected transistor as a voltage reference

In Figure 2-9, $I_{bias}$ can be replaced by a PMOS transistor, which is biased by applying voltage to the gate (Figure 2-10). If transistor PVT variations are compensated, there will be an accurate current reference resulting in a PVT independent voltage reference with high accuracy.

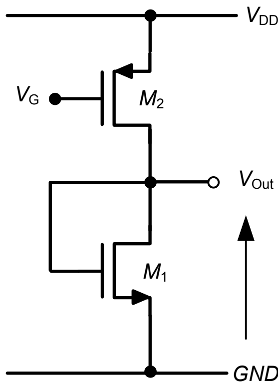


Figure 2-10) PMOS as $I_{bias}$ in Figure (2-9)

So far, it has been explained why current and voltage references are vital in analog circuits. Based on their definition, function and their simple circuits shown above

(Figure 2-8, Figure 2-10), if there is a way to have a current reference designed to the ideal as much as possible, a very accurate and independent voltage and current source can be achieved.

In [9], the author has proposed a constant current reference that compensates for all PVT variations. In this design, process variations have been compensated by benefiting physical relationship of $V_{th}$ and $\mu_n C_{ox}$. Based on this relationship, and the fact that in most of the possible variations increase of one is along with decrease of the other, a circuit has been designed for reference current which has four design parameters, three of which are PMOS transistors aspect ratio $\alpha$ , $\beta$ , $\gamma$ and one is $V_{gs}$ (Figure 2-11).

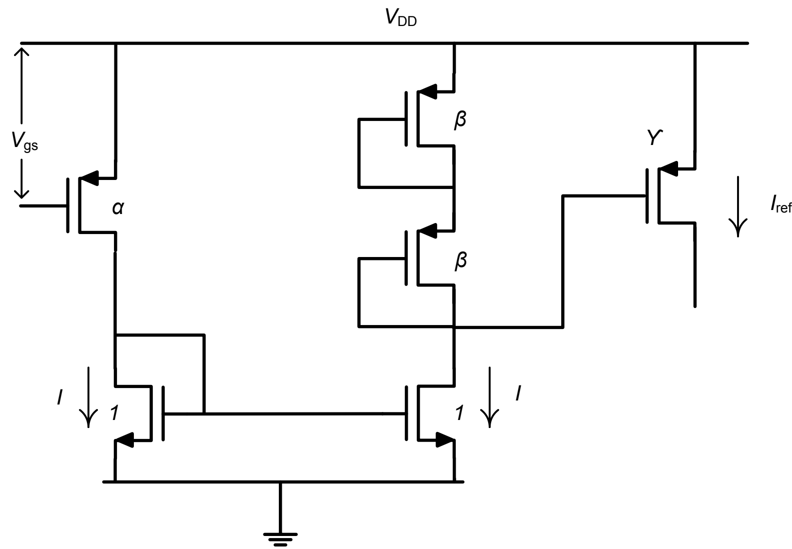


Figure 2-11) Reference current circuit in [9]

In this design, aspect ratios need to be calculated accurately. These calculations are complicated and obtained values are different than physical ones. Also their values should be fixed in order to compensate for process variations, but their values for temperature compensation are different, particularly, usually two $\beta$ values with process

and temperature compensations are far apart [9]. Hence, there is a tradeoff between process and temperature compensations. To compensate for power supply variations, $V_{gs}$ needs to be constant. Also, since reference current is dependent on this voltage, a constant $V_{gs}$ is necessary. Though, the circuit generating this gate-source voltage is not "resistorless" (Figure 2-12) and $V_{gs}$ depends on the ratio of two resistors that highly depend on process variations.

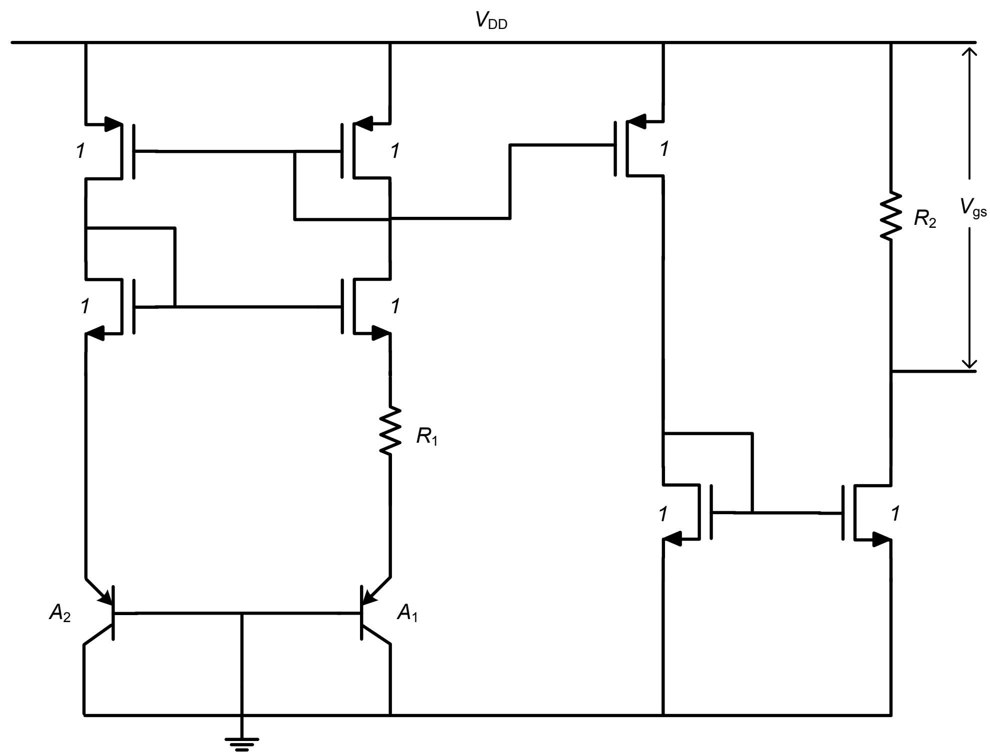


Figure 2-12) $V_{GS}$ generating circuit in [9]

## 2.3 Zero Temperature Coefficient (ZTC) Point

Each transistor has a transconductance curve that changes with temperature [13]. For any MOSFET, the relation between $I_D$ and $V_{GS}$ in the saturation region is approximately explained by using (2-6):

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (2\text{-}6)$$

Where, $\mu_n$ is the mobility of electrons, $C_{ox}$ is gate oxide capacitance per unit area, $W$ and $L$ are channel width and effective channel length respectively, and $V_{th}$ is the threshold voltage [14]. When a MOSFET operates as a current source, it should be in the saturation region. Since Threshold voltage and also Mobility change with temperature variations, (2-6) is temperature dependent. Their dependency is approximated by the following equations [11]:

$$V_{th}(T) = V_{th}(T_0) + \alpha_{VT}(T - T_0) \quad (2\text{-}7)$$

Here, $\alpha_{VT}$ is a negative constant and $T_0$ is the reference temperature. The next equation is written as follow:

$$\mu_n(T) = \mu_n(T_0)\left[\frac{T}{T_0}\right]^{\alpha_\mu} \quad (2\text{-}8)$$

In (2-8), $\alpha_\mu$ is also a negative constant. By plugging (2-7) and (2-8) into (2-6), there is a point in which mobility and threshold voltage variations compensate for each other mutually in any temperature. Consequently, voltage and current values of this point are:

$$I_D = I_{ZTC} = \frac{\mu_n(T_0)}{2}C_{ox}(\frac{W}{L})(\alpha_{VT}T_0)^2 \quad (2\text{-}9)$$

$$V_{GS} = V_{ZTC} = V_{th}(T_0) - \alpha_{VT}T_0 \quad (2\text{-}10)$$

Referring to (9-2) and (2-10), if a transistor is biased at ($I_{ZTC}$, $V_{ZTC}$), temperature variations are compensated and the current of the transistor can be used as a temperature independent current reference ($M_3$ in Figure (2-8) and $M_2$ in Figure (2-10)). This bias point is called the Zero Temperature Coefficient (ZTC) point, shown in Figure (2-13) for a typical NMOS transistor with W/L=20 using TSMC 65nm technology.

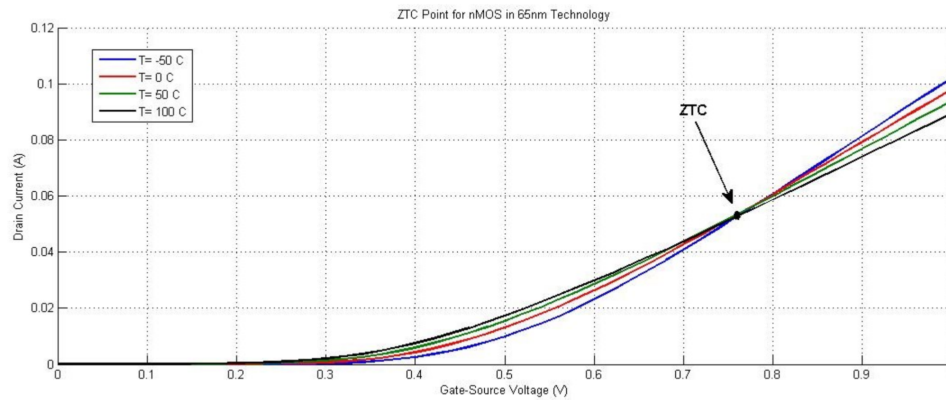


Figure 2-13) ZTC point simulated for NMOS in 65nm technology

Multiple simulations have shown that a MOSFET in 65nm technology has a unique ZTC points below nominal voltage. Also, the Monte Carlo analysis simulations have proven that for every single MOSFET transistor, the ZTC point changes with process variations (Figure 2-14). Therefore, although the current or voltage of the ZTC point can be used as a temperature independent source, it is still sensitive to process variations.

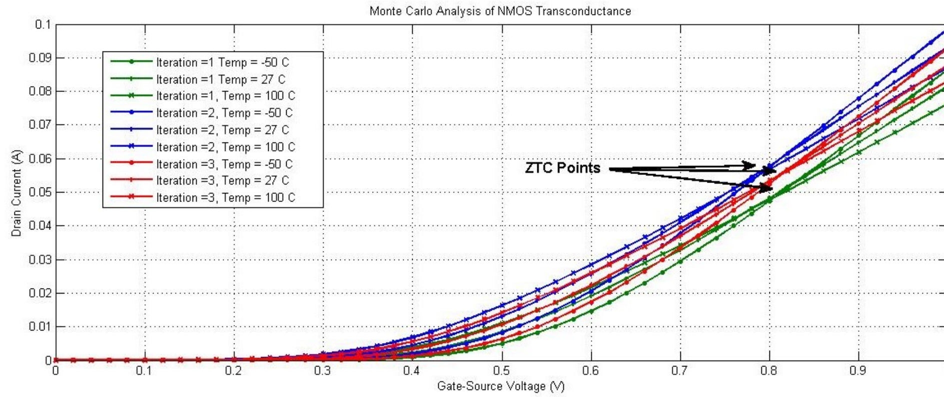


Figure 2-14) Monte Carlo analysis of NMOS transconductance for different temperatures

It is possible to change $V_{ZTC}$ and $I_{ZTC}$ by using unconventional biasing structures or by changing MOSFET bulk-source voltage ($V_{BS}$). As a result, based on the application and the desired current value, by proper scaling, different current references can be achieved.

There is a very useful feature of the ZTC point in MOSFETs. Figure (2-15) shows that if MOSFET is driven in a DC point other than the ZTC point, the direction of $I_D$ variations on both sides of the ZTC point with respect to temperature variations are opposite if $V_{GS}$ is kept constant. Similarly, the direction of $V_{GS}$ on both side of the ZTC point are opposite if $I_D$ is constant [15]. Considering this fact, drain current variations of a MOSFET can be used in a feedback loop to converge the MOSFET bias point to the vicinity of the ZTC point.

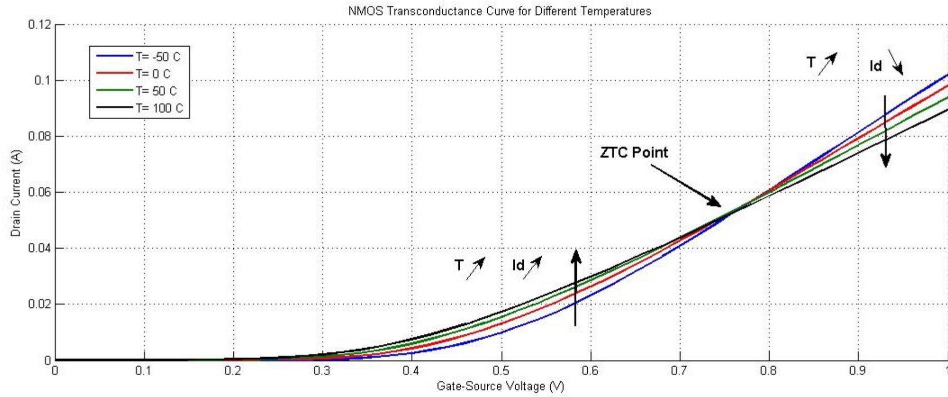


Figure 2-15) $V_{GS}$ versus $I_D$ plot for an NMOS at different temperatures

In [11], a 1 V current reference with temperature and process compensation in 180nm CMOS technology has been proposed. In the paper, drain current of a MOSFET in the saturation region (Eq. (2-11)) has been considered as a current reference (Figure 2-16). The output transistor has been biased at the vicinity of the ZTC point in order to compensate for temperature variations. Proper sizing of the output transistor, $M_4$, allows the circuit to operate in the vicinity of the ZTC point. Though, it needs to find ($V_{ZTC}$, $I_{ZTC}$), which is approximated by transistor level simulations or calculated using (2-9) and (2-10), it still does not guarantee that at this biasing point the transistor is in the vicinity of the ZTC point after the fabrication, since the ZTC point varies with process variations.

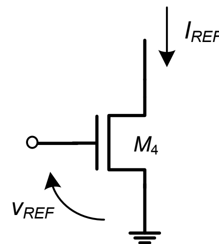


Figure 2-16) Output transistor as a current reference in [11]

To compensate for process variations, $V_{ref}$ is being generated by a circuit in a way that $V_{ref}$ variations are positively correlated to the variations of $V_{th}$ and thus, ($dV_{ref}$ - $dV_{th}$)

is as small as possible. But transistor width $W_4$ and Length $L_4$ have to be several times larger than the minimum size allowed by the technology [11] and yet, $I_{ref}$ remains dependent on changes in $C_{ox}$ and $\mu_n$ (Eq. (2-12)).

$$I_{ref} = \frac{\mu_n C_{ox}}{2} \frac{W_4}{L_4} (V_{ref} - V_{th4})^2 \quad \text{`(2-11)}$$

$$\frac{dI_{ref}}{I_{ref}} = \frac{d(\mu_n C_{ox} W_4 / L_4)}{\mu_n C_{ox} W_4 / L_4} + 2 \frac{(dV_{ref} - dV_{th4})}{(V_{ref} - V_{th4})} \quad (2\text{-}12)$$

The $V_{ref}$ generating circuit (Figure 2-17) is not “resistorless”, meaning that it is highly sensitive to both temperature and process variations.

Figure 2-17) $V_{ref}$ generating circuit in [11]

The circuit also needs trimming to have a proper ratio between two resistors, $R_1$ and $R_2$, and this ratio is obtained from the complicated equation below:

$$\frac{R_2}{R_1} = -\frac{q}{k\ln(N)}\left(\alpha_{VT} + \left[\frac{2I_{D7}}{\mu_n(T_0)T_0^2C_{ox}(W_7/L_7)}\right]^{1/2}\right) - 1 \tag{2-13}$$

Where $M_7$ is a transistor in the transimpedance differential amplifier (TIA) circuit.

## 2.4 MOSFET Self-Heating (SH)

Due to their thermal resistance, active devices dissipate power when they start conducting charges. The dissipated power is called Self-Heating [22]. Reduction and scaling the device dimensions when they enter the nanometer scale, increases current and power density in them. It also reduces thermal conductivity of Si from the bulk value [18]. Since self-heating increases device temperature, it can affect analog devices' performance drastically such as; threshold voltage shift, mobility reduction, device reliability reduction, timing errors and delayed signals [18]. Being able to model self-heating and its effects is important in circuit design and it helps designers to generate equivalent circuits considering self-heating effects.

In order to model self-heating, a thermal resistance ($R_{th}$) is used to quantify active device heat resistance and temperature-power relation. Also, the device time dependency is modeled with a thermal capacitance ($C_{th}$), which shows the ability of the device to store heat. In [19], an approach is shown, in which it is possible to calculate $R_{th}$ analytically. In addition to analytical and numerical approaches for modelling self-heating, there are methods for experimental characterization of self-heating. Two of most recent ones are Pulsed *I-V* method, which characterizes self-heating in time domain, and the AC conductance technique, which is a frequency domain approach to characterize self-heating. Both methods have been studied on SOI MOSFETs in 130nm technology.

Pulsed *I-V* has two related techniques. One is the Hot Chuck Characterization which has much better accuracy mentioned in [18]. $R_{th}$ extracted from this technique equals to $0.20K.mW^{-1}$. From the AC conductance technique, it has been resulted that $R_{th} = 0.22K.mW^{-1}$ and since frequency domain techniques measure thermal impedance $Z_{th}$, thermal capacitance ($C_{th}$) can be calculated using AC conductance technique where $C_{th} \cong 25pJ.K^{-1}$. Thus, $\tau_{th}$ of the RC-network is estimated within 100-500ns range, depending on the method used. Also, in [22] the impact of technology scaling of $R_{th}$ versus gate length has been presented, where it is possible to approximate $R_{th}$ value in the self-heating model for FinFET transistors in 65nm technology.

$C_{th}$ is measured by using device simulation, which shows 100ns for time constant [21]. In [22], a self-heating equivalent circuit has been proposed for FinFETs. This circuit is electro-thermal coupling based; the dissipated power is applied to the model circuit changing the ambient temperature and the new temperature impacts transistor parameters (Figure 2-18).

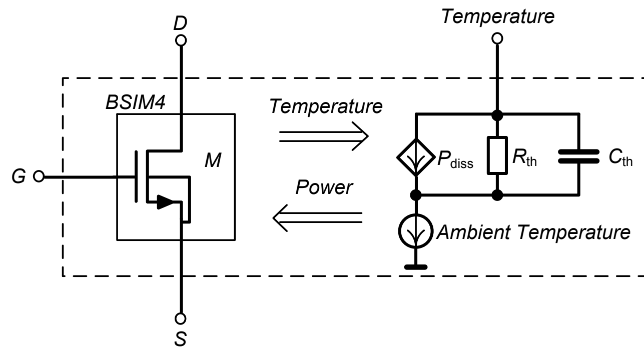


Figure 2-18) Self-heating equivalent circuit in [22]

This model is used for the MOSFET transistor in this thesis with a few modifications in order to model the self-heating. Circuit suggested in [22] cannot model

self-heating properly because of incorrect connections, since current sources need to be parallel and the sum of both currents passes the RC-network. The correct model is shown in Figure (2-19).

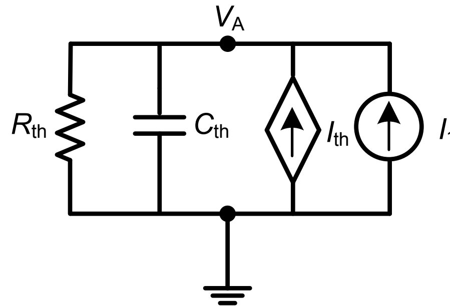


Figure 2-19) Self-Heating characterization circuit for MOSFETs

In this model, voltage at node $V_A$ represents the ambient temperature. $I_1$ is the current proportional to the room temperature and $I_{th}$ is the current proportional to the temperature change due to MOSFET self-heating. The latter equals to the MOSFET drain current $I_D$. When there is no power consumption in a typical MOSFET transistor, the dependent current source is open circuit and current is zero. In this condition, the voltage at node $V_A$ is room temperature. The moment that transistor conducts current, the current $I_{th}$ increases proportional to the dissipated power in MOSFET. As a result, voltage at $V_A$ starts changing, which represents the ambient temperature affected by the transistor self-heating. The RC-network has the same time constant as the ambient temperature variations.

There are not many articles that have used self-heating in field-effect transistors specifically SOI MOSFETs in order to reduce PVT variations. In [17] two different methods have been discussed in order to minimize output characteristics variations of MOSFETs due to self-heating. However, ambient temperature shifts are not considered in

the modeling. There is no available article on studying self-heating as an advantage in order to design a self-healing circuit.

These introductions are led to the following chapters where the idea of a self-healing circuit is explained by a flow chart followed by a block diagram representing the circuit major components. A model of the original circuit is designed in order to predict circuit behavior in Spectre simulator and internal circuit of each component is shown along with the corresponding equations. The self-healing technique is applied to the current references of two common applications and the simulation results are compared with the uncompensated applications as well as with the results of the other techniques.

# 3. Chapter Three: Self-Healing Circuit

## 3.1 Circuit Algorithm

The objective of this research is to propose a technique to self-bias a current reference in the vicinity of the ZTC point independent of PVT variations. In order to have such a self-biased current source, different analog and digital blocks have been used in the primary design. This technique is using a self-heating sensor to model ambient temperature changes, so the transistor drain current would change accordingly. This sensor consists of a sample and hold block that samples the current in two different time intervals and compares them through a comparator. A feedback loop along with the sensor completes this technique to self-bias the current reference transistor in the proper vicinity.

The first step to have an idea about the purpose of this technique is to create a flow chart diagram, which depicts the functionality of the technique. the algorithm has been shown in Figure (3-1).

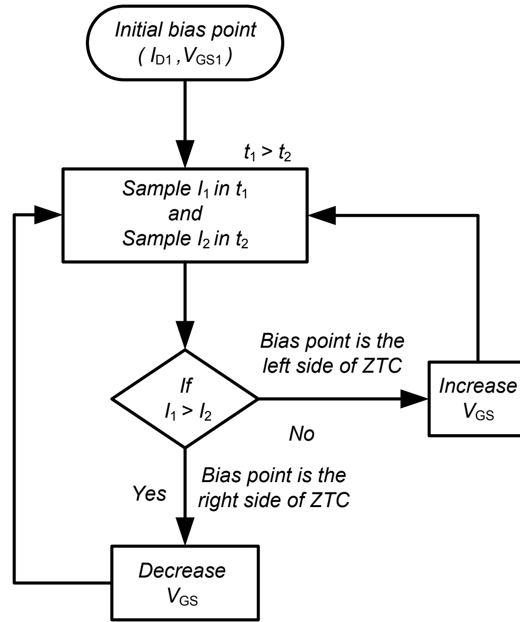


Figure 3-1) Self-Healing Circuit Algorithm

Having the figure plotted before in chapter two (Figure 3-2), the flow chart can be explained based on MOSFET current and voltage behavior at different temperatures.

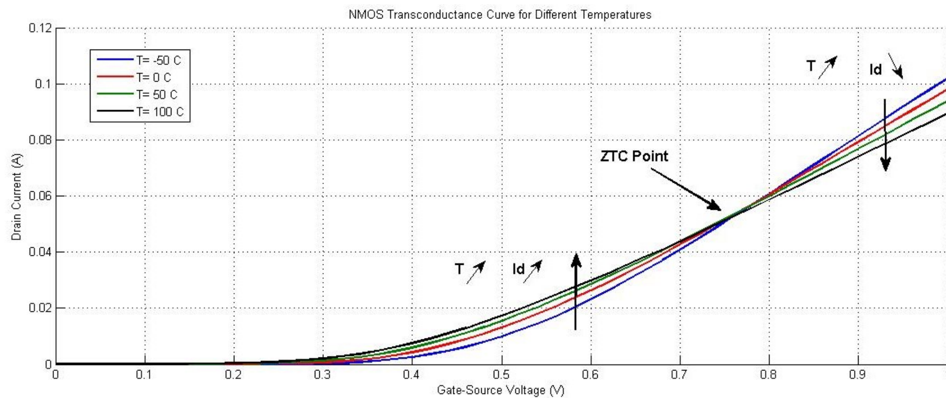


Figure 3-2) $V_{GS}$ versus $I_D$ plot for an NMOS at different temperatures

The algorithm starts with an initial bias point, which is on the transistor transconductance curve and it is either on the left side or the right side of the ZTC point. At this point, current and voltage change with temperature in a way that if the transistor gate-source voltage is fixed, then the current will increase or decrease. Now, if the bias

point is on the right side of the ZTC point, the current changes opposite of the temperature, while if it is on the left side, they both change positively. After initial biasing, current change direction needs to be determined. This is being achieved by sampling the drain current at two different time intervals $t_1$ and $t_2$. One ($t_1$) after the transistor conducts current ($I_1$) and one ($t_2$) when the current is affected by temperature change ($I_2$). Since the moment that current starts flowing through the MOSFET, the transistor begins dissipating power in the form of heat, the temperature always increases and thus, the ZTC localization is only based on the current change direction. By comparing the sampled currents ($I_1$ and $I_2$), it is possible to estimate the biasing point position with respect to the ZTC point. From figure (3-2) it is clear that if current decreases, the sampled current at $t_2$ is less than the sampled current at $t_1$ ($I_2 < I_1$) and therefore, the bias point is on the right side of the ZTC point and in order to shift it towards the vicinity of ZTC point, the gate-source voltage should decrease. The other situation is when $I_2$ is greater than $I_1$ ($I_2 > I_1$). So, current is increasing with temperature rise and the bias point is located on the left side of the ZTC point. Consequently, the gate-source voltage increases to move the bias point toward the vicinity of the transistor ZTC point.

Before designing a circuit which can satisfy the logic in the flow chart depicted in Figure (3-1), there is an issue in the simulation tools that needs to be taken care of. Simulation tools do not take into account the self-heating effect and they are also unable to change the transistor current affected by temperature. Thus, both the self-heating effect and the current change need to be modelled in the simulation environment. The whole

model is called "self-heating sensor", which consists of two major blocks; the self-heating equivalent circuit and the drain current estimator block.

## 3.2 Circuit Block Diagram

A simple block diagram of the self-healing circuit is shown below:

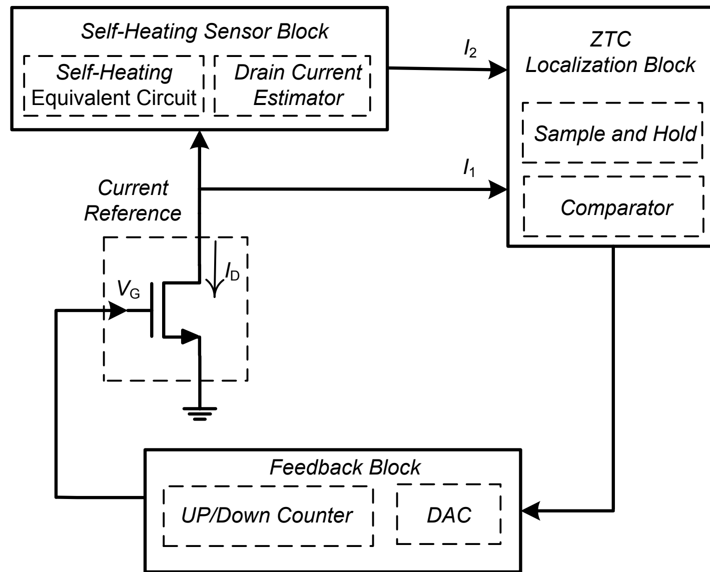


Figure 3-3) Self-healing circuit block diagram

As it is illustrated in the block diagram Figure (3-3), the simulation model of the technique is comprised of three blocks: the self-heating sensor block, the ZTC localization block and the Feedback block. The self-heating sensor block senses the ambient temperature affected by the self-heating, and changes the drain current accordingly in order to have $I_2$ at the output. The ZTC localization block compares two currents $I_1$ and $I_2$ by sampling and applying them to a comparator inputs, so it can localize the bias point with respect to the ZTC point and the feedback block uses an up/down counter and a Digital to Analog Converter (DAC) in order to change $V_{gs}$ voltage based on the ZTC localization block output signal.

The final self-healing circuit model, designed in simulation environment, has been demonstrated in Figure (3-4).

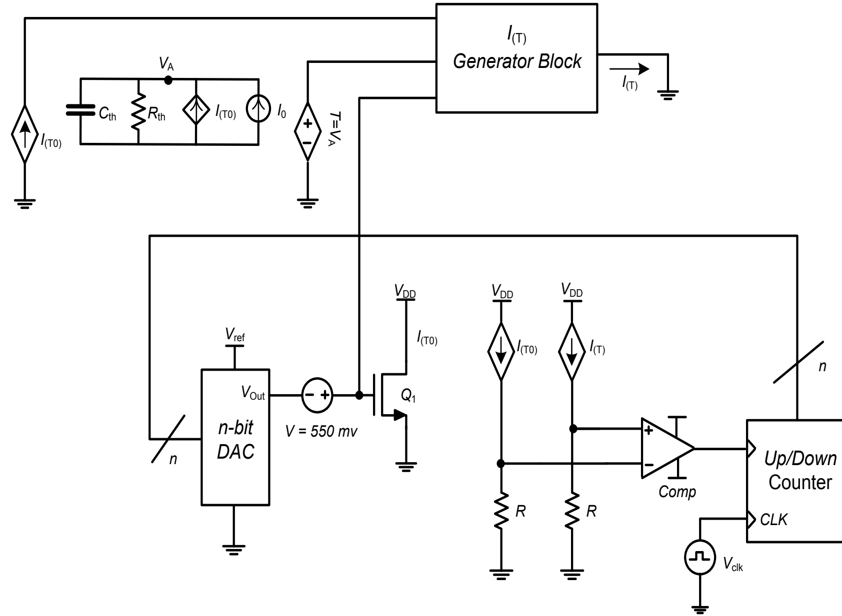


Figure 3-4) A model of self-healing circuit considering self-heating effects

Figure (3-5) shows the original self-healing circuit schematic, designed for fabrication where there is no need to model the physical effects of the self-heating and the drain current change.

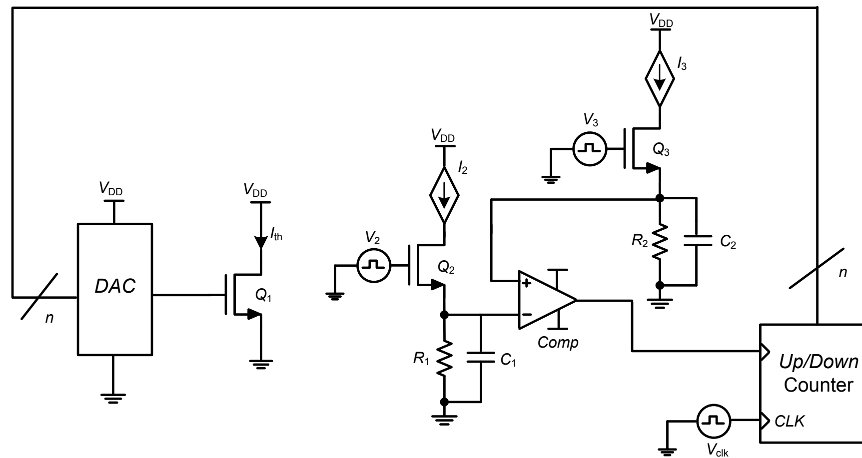


Figure 3-5) Self-healed current source circuit

To simulate the circuit in the AMS Cadence Environment, it is necessary to model the self-heating of an NMOS in 65nm technology using an equivalent circuit. As it is discussed in chapter two, the circuit below models the MOSFET self-heating and the output voltage $V_A$ equals to instantaneous ambient temperature affected by the self-heating.

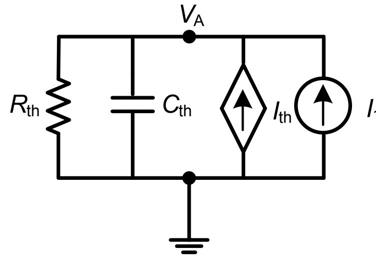


Figure 3-6) Self-Heating equivalent Circuit

Values of $R_{th}$ and $C_{th}$ in the circuit in Figure (3-6) have been approximated using data in [18]. The next part explains how the components in the self-heating sensor block work.

## 3.3 Self-Heating Sensor

### 3.3.1 Self-heating Equivalent Circuit

The circuit in Figure (3-7) is the equivalent circuit for characterizing the transistor $Q_1$ (Figure 3-4) self-heating, making it possible to change the temperature dynamically through the transient analysis simulations in Spectre simulator.

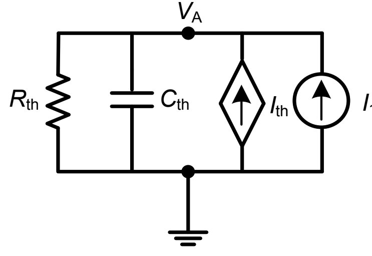


Figure 3-7) MOSFET self-heating equivalent circuit

The current $I_{th}$ in Figure (3-7) is equal to the drain current of the transistor $Q_1$. Absorbed power by the transistor $Q_1$ can be calculated by $P_{dc} = V_{DD} * I_D$, and since nominal supply voltage for MOSFETs in 65nm technology is 1 Volt, the dissipated power is proportional with the drain current ($P_{dc} \propto I_D$). $I_{th}$, $I_2$ and $I_3$ (Figure 3-5) are all current-controlled current sources. The simplest way to implement these components in fabrication process is to use simple current mirrors with current gain equal to one ($A_I$ = 1). It means that all of these current sources copy the exact value of the drain current of the transistor $Q_1$ at any moment.

In the circuit in Figure (3-7), voltage at node $V_A$ equals to the ambient temperature. Considering the circuits' thermal capacitance:

$$V_A = R_{th}(I_1 + I_{th}) * \left(1 - e^{\frac{-t}{\tau_{th}}}\right) \tag{3-1}$$

As discussed before, the temperature change time constant is about 100ns; $\tau_{th} = R_{th} * C_{th} \cong 100ns$. Therefore, by choosing proper pulse width for the pulse generators $V_2$ and $V_3$ in the circuit with the pulse width many times greater than 100ns, the transient part of the ambient temperature change is negligible and for $t \to \infty$ it can be written as:

$$V_{A(steady)} = R_{th}(I_1 + I_{th}) \tag{3-2}$$

When the transistor $Q_1$ is not biased, no current is being conducted and $I_{th}=0$ and voltage at node $V_{A(steady)} = I_1 * R_{th} = 300^\circ K$ (room temperature is $27^\circ C$ or $300^\circ K$). But when the current flows through the transistor $Q_1$, the ambient temperature will change accordingly and the temperature difference equals to $R_{th} * I_{th} = R_{th} * I_D$.

Also, to be able to do a transient analysis, the MOSFET current affected by the new ambient temperature also needs to be modeled in the Spectre simulation Environment with a drain current estimator block.

### 3.3.2 Drain Current Estimator Block

Since the current source output transistor is being biased in the saturation region, thus:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{3-3}$$

Where $\mu_n$ and $V_{th}$ are temperature dependent and they can be written as following equations in terms of T:

$$V_{th}(T) = V_{th}(T_0) + \alpha_{VT}(T - T_0) \tag{3-4}$$

$$\mu_n(T) = \mu_n(T_0)\left[\frac{T}{T_0}\right]^{\alpha_\mu} \tag{1-5}$$

By substituting (3-4) and (3-5) in (3-3), it yields:

$$I_D = \frac{C_{ox}}{2}\left(\frac{W}{L}\right)\mu_{n(T_0)}\left[\frac{T}{T_0}\right]^{\alpha_\mu}\left[V_{GS} - \left[V_{th(T_0)} + \alpha_{VT}\left(T - T_0\right)\right]\right]^2 \tag{3-6}$$

Where T is in Kelvin (K) and $T_0$ is the reference temperature, which is $300^o$ K (room temperature).

Assuming that the drain current at the room temperature is:

$$I_{D(T_0)} = \frac{\mu_{n(T_0)} C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th(T_0)})^2 \qquad (3\text{-}7)$$

By simplifying (3-6) along with substituting (3-7) in (3-6), the final equation can be expressed as below:

$$I_{D(T)} = \left[\frac{T}{T_0}\right]^{\alpha_\mu} [I_{D(T_0)} + \frac{\mu_{n(T_0)} C_{ox}}{2} \left(\frac{W}{L}\right) [\alpha_{VT}{}^2 (T - T_0)^2 - 2 * V_{GS} * \alpha_{VT} (T - T_0) + 2 * V_{th(T_0)} * \alpha_{VT} (T - T_0)]] \qquad (3\text{-}8)$$

Now that the drain current equation is obtained, by defining a block in Spectre simulator with $I_{D(T_0)}$, T and $V_{GS}$ as the inputs and $I_D$ as the output (Figure 3-8), it is possible to perform a transient analysis on the final model (Figure 3-4) of the whole circuit which functions as the original circuit plotted in Figure (3-5) .

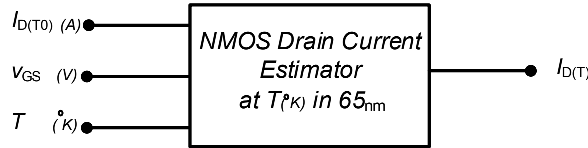


Figure 3-8) Transistor Drain current estimator block at T (0 K)

Before defining the block shown in Figure (3-8), the Parameters in (3-8) need to be specified. As mentioned earlier, $T_0=300^o$ K. It is feasible to measure $\mu_{n(T_0)} C_{ox}$, $\alpha_{VT}$, $\alpha_\mu$ and $V_{th(T_0)}$ by simulating an NMOS transistor biased in different DC points, in which L=650nm and $\frac{W}{L} = 2$. The channel length modulation is not considered, since L is large enough.

By sweeping the gate-source voltage and plotting the transconductance curve of the NMOS (Figure 3-9), it is noted that For $V_{GS_1} = 500\,\text{mV} \rightarrow I_{D_1} = 16.98\,\text{uA}$ and for $V_{GS_1} = 600\,\text{mV} \rightarrow I_{D_1} = 35.87\,\text{uA}$. Thus:

$$\frac{I_{D_2}}{I_{D_1}} = \left( \frac{V_{GS_2} - V_{th(T_0)}}{V_{GS_1} - V_{th(T_0)}} \right)^2 \tag{3-9}$$

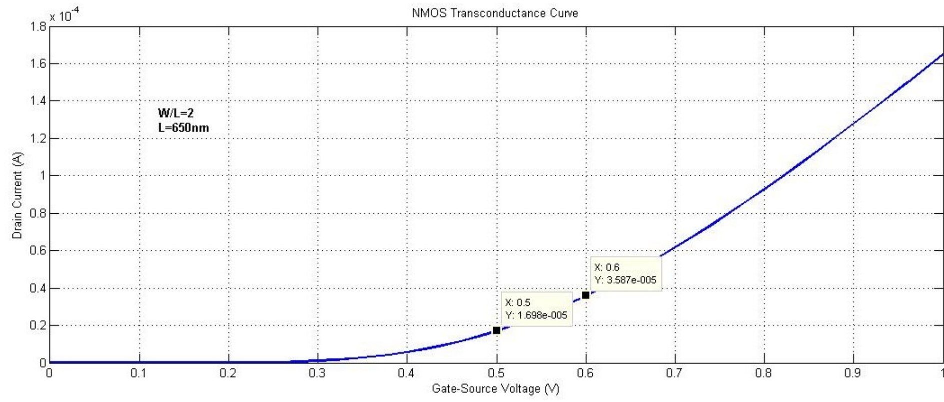


Figure 3-9) NMOS transconductance curve with L=650nm

Therefore, $V_{th(T_0)} = 280\,\text{mV}$. Consequently, it is also obtained that $\mu_{n(T_0)} C_{ox} = 3.5 * 10^{-4} \left( \frac{A}{V^2} \right)$. By plotting transconductance curve of the transistor in different ambient temperatures, $V_{ZTC}$ and $I_{ZTC}$ are approximated to $V_{ZTC} = 590\,\text{mV}$ and $I_{ZTC} = 33.6\,\text{uA}$. Using (2-10), It is calculated that $\alpha_{VT} = -1.03 \left( \frac{mV}{{}^0K} \right)$. In [11] and [23] $\alpha_{\mu} = -2$ for the NMOS transistors. Now all of the parameters in (3-8) are calculated, the equation can be rewritten as:

$$I_{D(T)} = \left[\frac{300}{T}\right]^2 [I_{D(T_0)} + (3.71*10^{-10})(T-300)^2 + (7.21*10^{-7})(T-300)V_{GS} - (2.0188*10^{-7})(T-300)] \quad (3\text{-}10)$$

The simulation and analytical results of this equation are in good agreement (Table 3-1). This equation is coded using Verilog-A programming language and is embedded in the block shown in Figure (3-8). The code has been added in Appendix I.

Table 3-1) Simulation and analytical results of (3-10)

| Gate-Source Voltage $V_{GS}$ (mV) | Drain Current at $T_0$=27°C $I_D(T_0)$ (uA) | Ambient Temperature T(°C) | Drain Current at T (uA) (Simulation) | Drain Current at T (uA) (Analytical) |
|---|---|---|---|---|
| 500 | 16.98 | 50 | 17.85 | 17.96 |
| 600 | 35.87 | 75 | 35.52 | 35.52 |
| 700 | 61.64 | 100 | 55.26 | 55.45 |

Before showing the simulation results and comparing them with other works, it is necessary to explain the major blocks of the original circuit shown in Figure (3-5) and to evaluate the standard deviation of the circuit based on the standard deviation of each block.

## 3.4 Circuit Analog/Digital Blocks

The self-healing circuit is composed of three major blocks:

### 3.4.1 Sample and Hold Circuit

Calibrating the transistor $Q_1$ as the current reference starts with the localizing the initial DC point relative to the ZTC point. In Figure (3-10), transistors $Q_2$ and $Q_3$ are switches, sampling the transistor $Q_1$ current at two different time intervals. The identical RC-networks connected to their sources store those currents as two voltage values. It has been mentioned before that the direction of the drain current variations on two sides of

the ZTC point is opposite when the MOSFET gate-source voltage is constant. Thus, a voltage greater than the transistor $Q_1$ threshold voltage is applied to the gate terminal. The moment current starts flowing through the transistor, the ambient temperature is $T_1 = 300^{\circ} K$. At this moment the pulse generator $V_2$ generates a voltage pulse that turns on the transistor $Q_2$ for a very short time ($t_1$). The current $I_2$ passes the transistor $Q_2$ and charges the capacitor $C_1$. The pulse generator $V_2$ pulse width is wide enough allowing the transistor $Q_2$ source voltage to reach to the steady state value ($t_1 > 5\tau_1, \tau_1 = R_1 C_1$), which has been applied to the comparator negative input ($V^-$). While the transistor $Q_1$ starts conducting, it also dissipates power, which increases the ambient temperature to $T_2$ ($T_2 > T_1$). Due to the self-heating, the transistor $Q_1$ current changes with the temperature to $I_3$. Same as $V_2$, $V_3$ also generates a voltage pulse, which turns on the transistor $Q_3$ for the time interval $t_2$ ($t_2 = t_1$), so the current $I_3$ passes the switch transistor $Q_3$ and charges the capacitor $C_3$ connected to the comparator positive input ($V^+$). RC-networks connected to the comparator are identical, meaning that $R_1 = R_2, C_1 = C_2$.

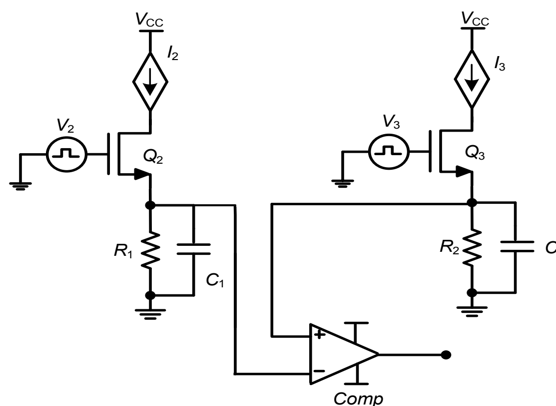


Figure 3-10) Sample and hold circuit

Two different scenarios may happen:

a) If $I_3 > I_2$, it means that the transistor $Q_1$ bias point is on the left side of the ZTC point and since:

$$V^- = R_1 I_2 e^{-\frac{t_1}{R_1 C_1}} \tag{3-11}$$

And:

$$V^+ = R_2 I_3 e^{-\frac{t_2}{R_2 C_2}} \tag{3-12}$$

Then, $V^+ > V^-$ and the comparator output signal is high.

b) If $I_3 < I_2$, it determines that the bias point is on the right side of ZTC point and therefore, $V^+ < V^-$ and the comparator output signal becomes low.

Since comparators are not ideal, they have a parameter called the input offset voltage or $V_{Offset}$. This voltage is the differential voltage needed to be applied to the comparator inputs in order to toggle the output. Generally, it limits the resolution of the comparators [24]. The circuit accuracy depends on the comparator $V_{Offset}$ value.

### 3.4.2 Up/Down Counter

The comparator output signal is applied to an up/down counter (Figure 3-11). The clock signal has a specific frequency and delay making sure that the correct input signal is applied to the counter. Depending on the counter input signal, after each clock pulse, the counter output binary number increments or decrements.

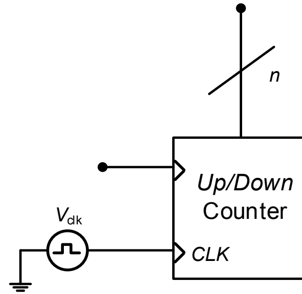


Figure 3-11) Up/Down Counter

The number of up/down counter bits is arbitrary but counter and DAC need to have the same number of bits.

### 3.4.3 Digital to Analog Converter (DAC)

The binary number on the counter output is the digital number on a Digital to Analog converter (DAC) (Figure 3-12).

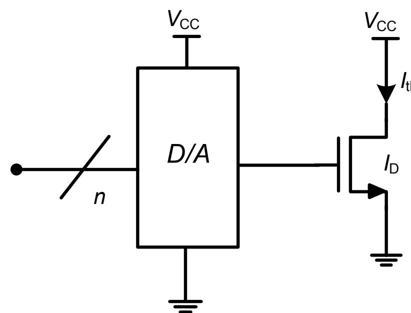


Figure 3-12) Digital to Analog Converter

The DAC resolution is the number of output levels the converter is designed to produce without errors. The binary number is converted to the corresponded voltage level on the DAC output, which is applied to the transistor $Q_1$ gate. This new gate voltage shifts the transistor $Q_1$ bias point toward the vicinity of the ZTC point. Based on the comparator output, the DAC output may increase or decrease one level for every

up/down counter clock pulse. The decrement and increment are always in the direction of convergence to the ZTC point. Circuit accuracy also depends on the DAC resolution.

## 3.5 Circuit Timing Diagram

There are two pulse generators and one clock pulse generator in the proposed circuit. To have a better understanding of the circuit functionality, the timing diagram below illustrates some of the voltages in the time domain for two clock pulses (Figure3-13). These voltages are $V_2$, $V_3$, $V^+$, $V^-$, $V_{clk}$, $V_{in(counter)}$ and $V_{GS(Q1)}$.

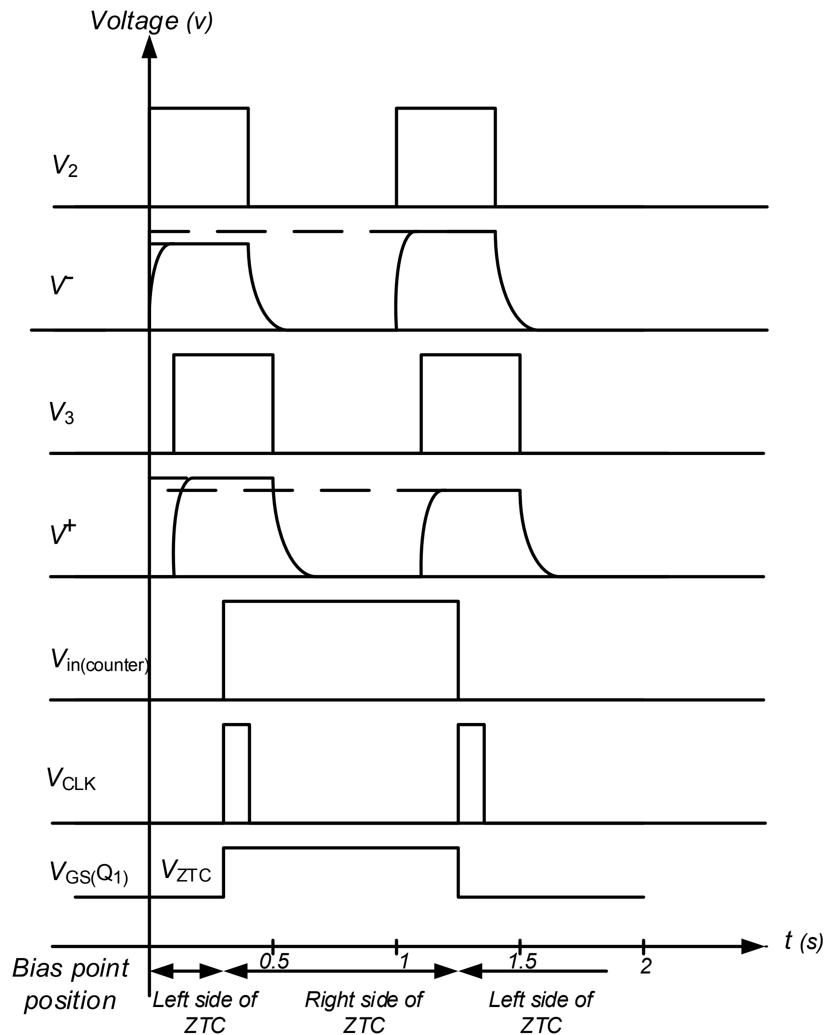


Figure 3-13) Timing diagram of some voltages in the self-healing circuit

## 3.6 Circuit Accuracy

There are two uncorrelated parameters that determine the accuracy of the self-healing circuit. The comparator input offset voltage ($V_{Offset}$) and the DAC resolution.

The comparator input offset voltage is the minimum differential voltage needed to be applied to the inputs, so the output would toggle. This voltage can be represented by a voltage source series to one of the inputs of an ideal comparator [24]. The standard deviation (σ) of the comparator offset voltage in 65nm technology differs in various designs. In different research, σ=22mV at 1.2V nominal voltage supply, 47mV at 0.6V [25], or 26mV at 1V [26]. Another offset-corrected comparator has the standard deviation of 35mV at 1V nominal power supply [27]. In [28], 100 Monte Carlo runs of a comparator in 65nm technology represents the standard deviation of σ=10.5mV.

The digital to analog converter resolution depends on the number of input bits. For every DAC, the resolution is calculated by $\frac{1}{2^N}$, in which $N$ is the number of input bits. In all of the simulations, an 8-bit DAC with $V_{ref}$=1.0V has been used. Therefore, the resolution is about 0.0039 and minimum output level is 3.9mV. Having this information, it is possible to find the standard deviation of the self-healed current source.

$$V_{ZTC} = V_{GS_1} + \varepsilon_{offset}(t) + \varepsilon_{DAC}(t) \tag{3-13}$$

$$\varepsilon_V = \varepsilon_{offset}(t) + \varepsilon_{DAC}(t) \tag{3-14}$$

According to [29], the mean squared error equals to the sum of the variance and the squared bias, and since two errors are uncorrelated, thus:

$$\sigma_V{}^2 = \sigma_{offset}{}^2 + \sigma_{DAC}{}^2 \tag{3-15}$$

Therefore:

$$\sigma_V = \sqrt{\sigma_{offset}{}^2 + \sigma_{DAC}{}^2} \tag{3-16}$$

From [28], it is assumed that $\sigma_{offset} = 10.5mV$. Since the standard deviation in a DAC equals to minimum level at the output, $\sigma_{DAC} = 3.9mV$. Having these values, the gate-source standard deviation is:

$$\sigma_V = \sqrt{(\frac{105}{10000})^2 + (\frac{39}{10000}{}^2)} = 11.2mV \tag{3-17}$$

Since the current source output current is the drain current of an NMOS, in order to find the standard deviation of output current, the transconductance equation of MOSFETs is used:

$$I_D = g_m * V_{GS} \tag{3-18}$$

Since the MOSFET operates in the saturation region and the ZTC point is located in this region, by differentiating of (3-3) in terms of $V_{GS}$:

$$\frac{\partial I_D}{\partial V_{GS}} = g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \tag{3-19}$$

As it is discussed, the simulation results show that for an NMOS with $\frac{W}{L} = 2$, the voltage and the current of the ZTC point are $V_{ZTC} = 590mV$ and $I_{ZTC} = 33.6uA$. Using the estimated values, $g_m = 217uS$. And Since:

$$\sigma I_D = g_m * \sigma V_{GS} \tag{3-20}$$

Therefore,

$$\sigma I_D = 2.43uA \tag{3-21}$$

This is the standard deviation of the self-healed current source output current. These values show that due to the effect of the temperature variations, $V_{bias}$ is $590mV \pm 1.9\%$ and $I_{ref}$ is $33.6uA \pm 7.23\%$.

The idea of a self-healing technique was started with a flow chart algorithm defining the circuit functionality. This flow chart later was illustrated by a simple block diagram, showing the main components of the circuit. Each block was introduced and their parameters were specified using either simulations or other research works. A model of the circuit was designed in the simulation environment in addition to the original circuit. The model was capable of having the self-heating effect on the temperature and also on the transistor drain current in Spectre simulator. The components were introduced thoroughly and the accuracy of the circuit was derived. Analytical results have shown very promising accuracy. The simulations in next chapter show the circuit performance while it is connected to two common analog and digital applications and the results are compared with the uncompensated applications and with the results of the other methods.

# 4. Chapter Four: Simulations and Results

The proposed self-healing circuit is explained thoroughly in the chapter three and the functionality of this technique is discussed. A simple block diagram is presented for the circuit based on the defined algorithm. Each block is discussed in the transistor level and is substituted by the proper components. The final design is shown in Figure (3-5). Also, since the self-heating effect on the ambient temperature and the ambient temperature change effect on the transistor current is not included in spectre simulator, a self-heating sensor block is defined using Verilog-A programming language to be able to simulate the final circuit in the Spectre simulation environment. This model of the original circuit is presented in Figure (3-4). The model is plotted again in Figure (4-1). After studying the performance and the accuracy of the designed circuit, it is applied to an NMOS transistor as a simple current source in order to self-bias the current source in the vicinity of the ZTC point. The self-healed current reference biases two different applications and the simulation results are compared with the uncompensated applications and also with the results derived from other methods.

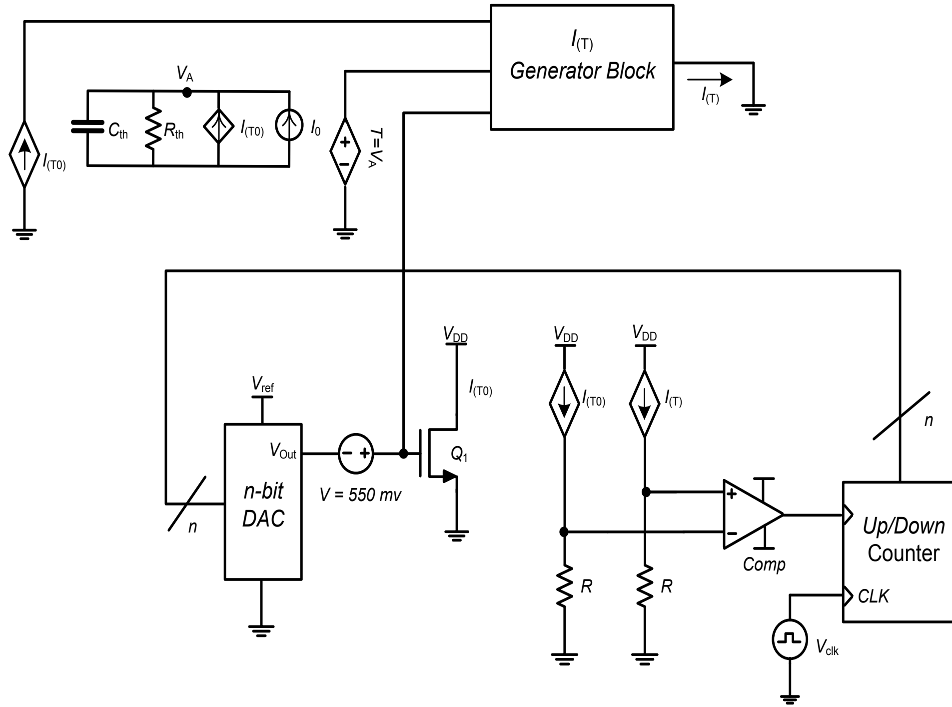


Figure 4-1) Self-healing circuit model in Spectre simulation environment

Proper pulse signals are applied to the designed model and the transient analysis is done for 25ms in order to converge the current source output transistor bias point to the vicinity of the ZTC point. Figure (4-2) and Figure (4-3) are the input voltage and the output current of the transistor $Q_1$ respectively.

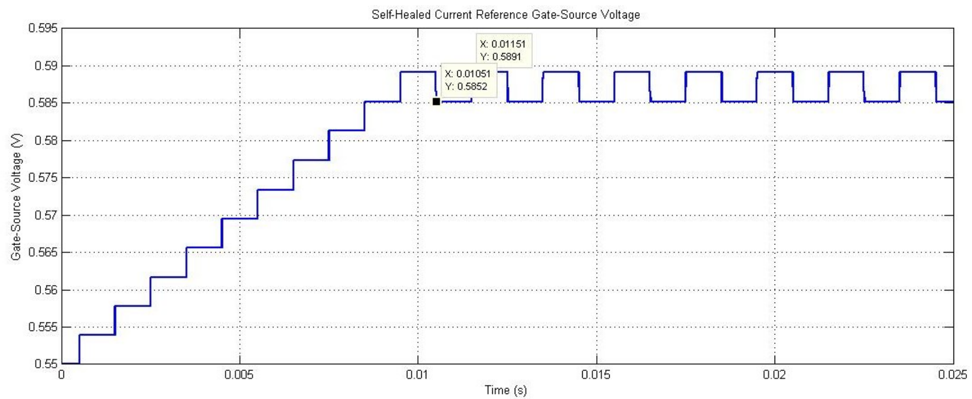


Figure 4-2) $V_{GS}$ of the self-healed current reference

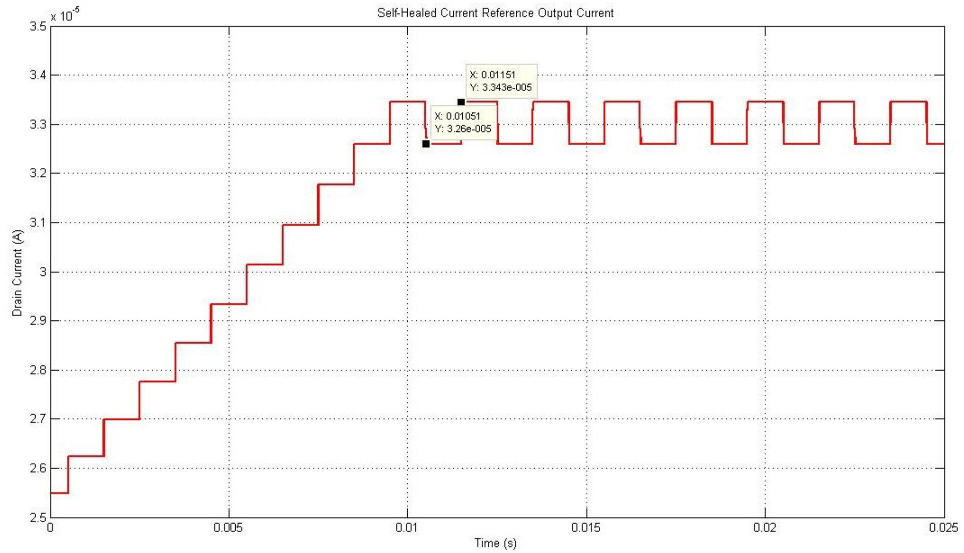


Figure 4-3) $I_D$ of the self-healed current reference

In the transient analysis, the transistor $Q_1$ is initially biased with 550mV at the gate terminal in order to make sure that it conducts current in the saturation region. As it is illustrated in Figure (4-2) and Figure (4-3), after 10 clock pulses, the transistor bias point reaches to the vicinity of the ZTC point. The gate-source voltage changes 4mV for each clock pulse, since an 8-bit DAC with $V_{ref}$= 1V has been used. The $V_{GS}$ oscillates between 584mV and 589mV while the drain current is changing between 32.6uA and 33.45uA. Both transistor current and voltage are in the vicinity of the transistor ZTC point, which have agreements with the simulation results discussed in the chapter three.

Now that it is demonstrated that the self-healing circuit converges the current source MOSFET bias point to the vicinity of the ZTC point, this self-healed current reference is applied to two common applications and the PVT variations are measured and compared with the uncompensated applications and also with the other similar methods.

## 4.1 Basic Current Mirror

A basic current mirror is plotted in Figure (4-4).

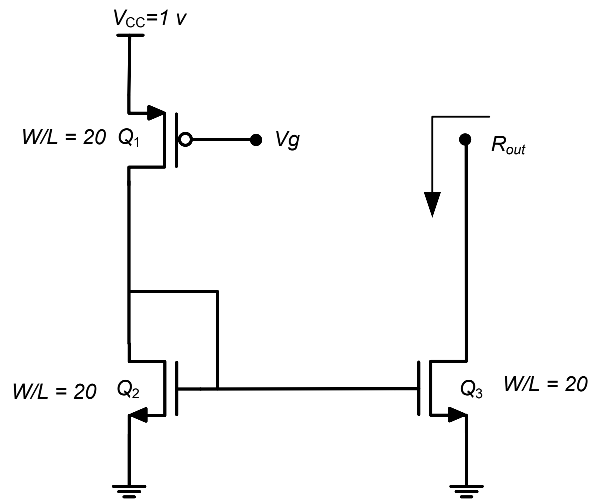


Figure 4-4) Basic current mirror schematic

This current mirror is biased with a PMOS transistor as the current source. The current source transistor ZTC point is obtained by sweeping the gate voltage and plotting the transconductance curve at different temperatures (Figure 4.5).

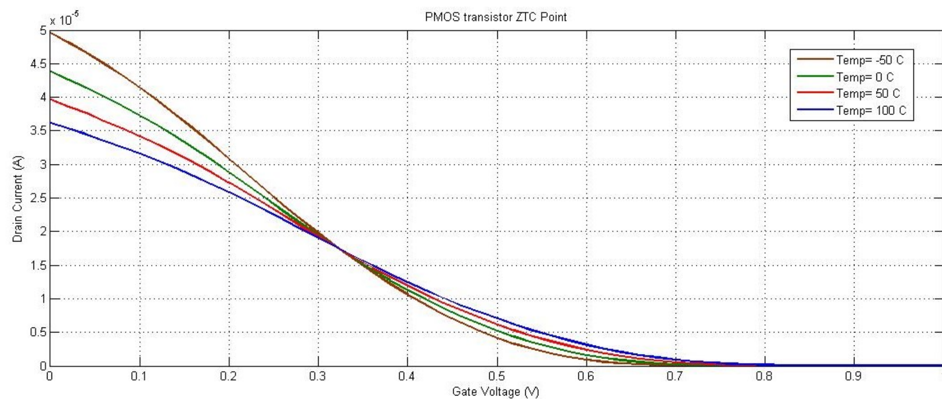


Figure 4-5) ZTC point of basic current mirror PMOS current reference

Figure (4-6) shows the current mirror output current ($I_{out}$) for different bias points in the temperature range of -$50^0$ C to $100^0$ C.

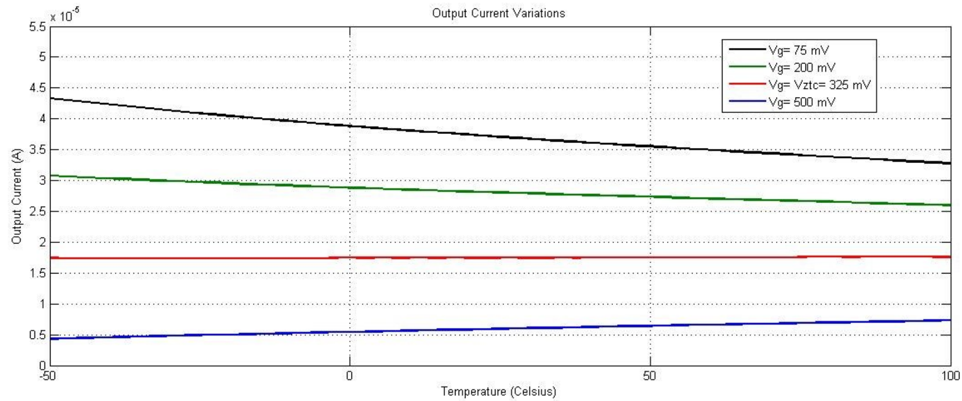


Figure 4-6) Output current for different bias points

The output current variation ( $\Delta I_{out}$ ) of the current mirror due to the temperature variations biased by the self-healed current source is compared with the current mirror biased in other DC points. Table (4-1) represents the output current variation for different bias points in the mentioned temperature range. The nominal output current ($I_0$) is the current at T= $27^0$ C ($300^0$ K).

Table 4-1) Current mirror output current relative error for different bias points

| $V_G$ (mV) | $\Delta I_{out}(\mu A)$ | $\frac{\Delta I_{out}}{I_0}\%$ |
|---|---|---|
| 75 | 10.57 | 28.61 |
| 200 | 4.8 | 17.15 |
| **325 ($V_{ZTC}$)** | **0.15** | **0.86** |
| 500 | 2.96 | 49.49 |

Below, Table (4-2) shows the output current variation due to the voltage supply variations when the current mirror is connected to the self-healed current source and also when the current source is not compensated.

Table 4-2) basic Current mirror output current variation to Supply voltage variation ratio

| $V_{DD}$ (V) | $I_{out}$ ($\mu A$) (compensated) | $I_{out}$ ($\mu A$) (uncompensated) | $\frac{\Delta I_{out}}{\Delta V_{DD}}$ ($\mu S$) (compensated) | $\frac{\Delta I_{out}}{\Delta V_{DD}}$ ($\mu S$) (uncompensated) |
|---|---|---|---|---|
| 0.9 | **16.71** | 10.09 | **7.4** | 73.6 |
| 1 | **17.45** | 17.45 | **-** | - |
| 1.1 | **17.94** | 26.55 | **4.9** | 91 |

Process variations effect on the current mirror output current is also studied. For this purpose, the output current variation is measured in three different process corners of Slow-Slow (SS), Fast-Fast (FF) and Typical-Typical (TT) while the current source is self-healed and biased in the vicinity of the ZTC point and also when $V_G$ is constant and the output current changes due to process variations. The output current variations ($\Delta I_{out}$) of the current mirror in those corners and the relative errors are demonstrated in Table (4-3).

Table 4-3) Basic current mirror output current relative error in different process corners

| Process Corner | $I_{out}$ ($\mu A$) (calibrated) | $I_{out}$ ($\mu A$) (uncalibrated) | $\frac{\Delta I_{out}}{I_{nominal}}\%$ (calibrated) | $\frac{\Delta I_{out}}{I_{nominal}}\%$ (uncalibrated) |
|---|---|---|---|---|
| FF | **18.28** | 21.66 | **4.76** | 24.12 |
| TT | **17.45** | 17.45 | **-** | - |
| SS | **16.52** | 13.76 | **5.33** | 21.14 |

The results in Table (4-3) shows that although keeping a current source transistor biased in the vicinity of the ZTC point does not compensate for process variations, it degenerates them significantly, especially in the TT to FF corners as if there is a resistor connected to the transistor source terminal and the bias point moves on a line with the

negative slope on the transconductance plot instead of moving vertically when $V_{gs}$ is kept constant (Figure 4-7).

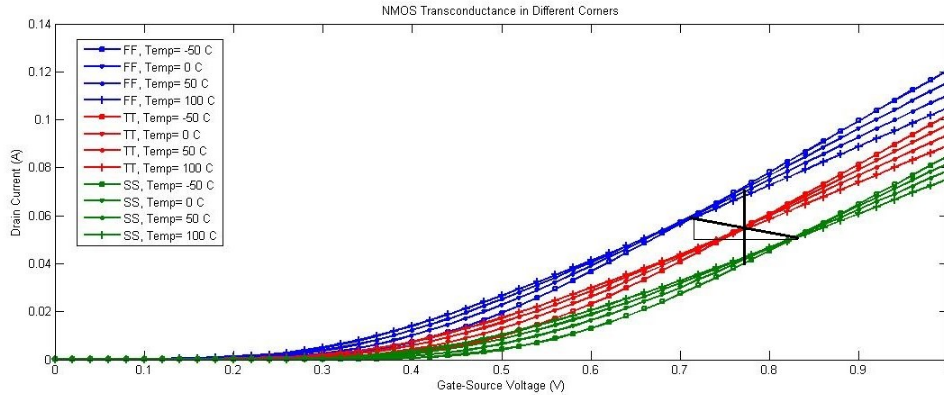


Figure 4-7) NMOS transconductance curves in tt, ff and ss corners

In this case, it is clear in Figure (4-7) that with biasing the current reference MOSFET at the vicinity of the ZTC point instead of forcing $V_{bias}$ to be fixed at a constant voltage, not only the temperature variations are compensated and the temperature sensitivity is not changing with process variations, but also the output current deviation due to process variations decreases significantly.

It was obtained in chapter two that by considering only the effect of temperature variations on a self-healed MOSFET transistor, the output current of the 1 V current source equals to $33.6^{\mu A} \pm 7.23\%$. In [11] a current reference in 180nm technology has been designed and fabricated. The output current considering both process and temperature variations is $144.3^{\mu A} \pm 7\%$ which is more suitable for the higher power applications. Although the current variation is due to temperature and process variations and not only temperature variations, the seal-healed current source proposed in this report is less complicated while the accuracy is promising. Also this technique is digital oriented

and despite the circuit suggested in [11], the proposed circuit is possible to be fabricated in newer technologies.

## 4.2 Current-Starved Inverter

For the second application, a current-starved inverter is biased by an NMOS transistor as the current source. The circuit is plotted in Figure (4-8).

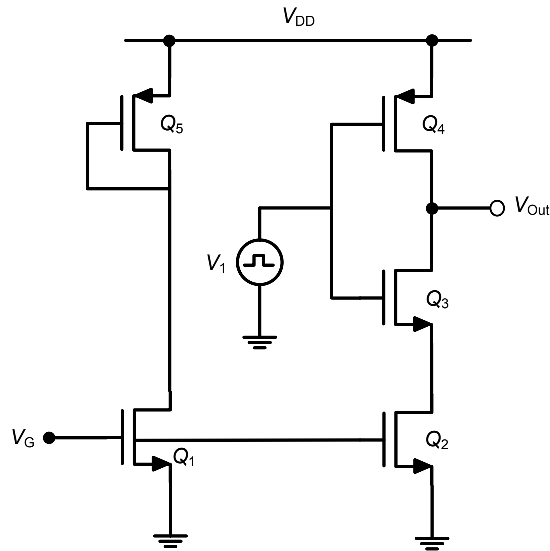


Figure 4-8) Current-starved inverter biased by a MOSFET current reference

The inverter delay has been studied when the current source is self-healed and also when it is biased in other DC points. The delay variations in the temperature range of $0^0$ C to $60^0$ C for different bias points is shown in Figure (4-9).

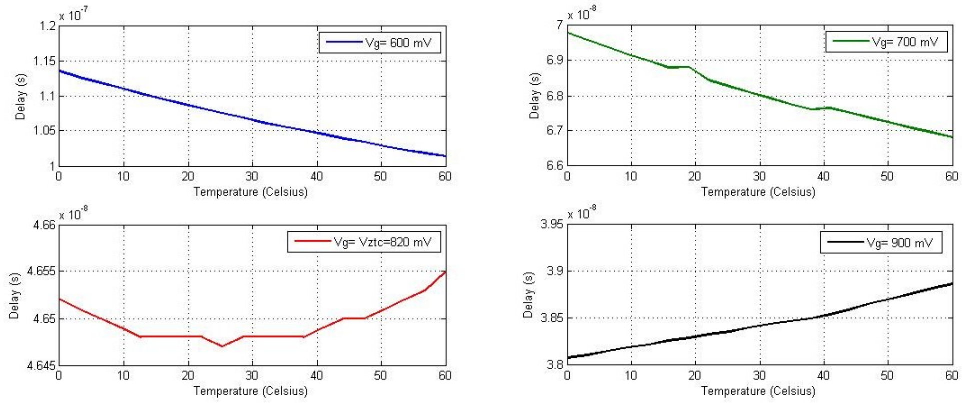


Figure 4-9) Inverter delay for different bias points

Table (4-4) represents the inverter delay for different bias points in the mentioned temperature range. The nominal delay ($Delay_0$) is the delay at T= $27^0$ C or $300^0$ K.

Table 4-4) Inverter delay relative error for different bias points

| $V_G$ (mV) | $\Delta Delay$ (ns) | $\frac{\Delta Delay}{Delay_0}$ % |
|---|---|---|
| 600 | 12.12 | 11.3 |
| 700 | 2.98 | 4.4 |
| **820 ($V_{ZTC}$)** | **0.072** | **0.15** |
| 900 | 0.8 | 2.1 |

Since the supply voltage variation does not change the gate-source voltage of the current source transistor, it is not possible to compensate for the supply voltage variations by ZTC biasing of the inverter in Figure (4.8). Yet, this problem can be solved by having a PMOS current source to bias the inverter instead of an NMOS current source (Figure 4.10).

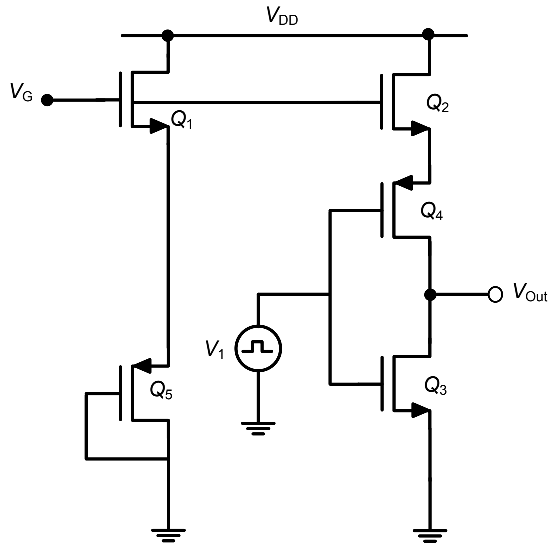


Figure 4-10) An inverter biased with a PMOS current reference

Table (4-5) represents the inverter delay due to the voltage supply variations when the current reference in Figure (4.10) is self-healed and also when it is not compensated.

Table 4-5) Inverter delay variation to Supply voltage variation ratio

| $V_{DD}$ (V) | Delay (ns) (compensated) | Delay (ns) (uncompensated) | $\frac{\Delta Delay}{\Delta V_{DD}}(\frac{ns}{V})$ (compensated) | $\frac{\Delta Delay}{\Delta V_{DD}}(\frac{ns}{V})$ (compensated) |
|---|---|---|---|---|
| 0.9 | **39.67** | 54.07 | **49.8** | 193.8 |
| 1 | **34.69** | 34.69 | **-** | - |
| 1.1 | **32.26** | 24.57 | **24.3** | 101.2 |

Same as the current mirror output current in previous part, the inverter delay is calculated in different process corners while the current reference is constantly biased in the vicinity of the ZTC point and when the DC point is not tracking the ZTC point changes due to process variations, meaning that the gate voltage is constant and only the output current varies. The results has been shown in Table (4-6).

Table 4-6) Inverter delay relative error in different process corners

| Process Corner | Delay (ns) (compensated) | Delay (ns) (uncompensated) | $\frac{\Delta delay}{Delay_{nominal}}\%$ (compensated) | $\frac{\Delta delay}{Delay_{nominal}}\%$ (uncompensated) |
|---|---|---|---|---|
| FF | **47.39** | 39.86 | **1.96** | 14.24 |
| TT | **46.48** | 46.48 | **-** | - |
| SS | **66.04** | 84.39 | **42.1** | 81.56 |

The results show that the process variations are degenerated significantly when the current source is being biased in the vicinity of the ZTC point.

# 5. Chapter Five: Conclusion and Future Works

Many different methods have been suggested in order to compensate for PVT variations in CMOS circuits. Some of them are capable of compensation process, voltage supply and temperature variations all together, while most of them can only compensate for one or two of these variations.

The method suggested in this report offers a simple way to self-heal an output MOSFET transistor as a current reference in 65nm technology by biasing the transistor dynamically in the vicinity of the ZTC point where current and voltage of a MOSFET are independent from temperature variations. Ambient temperature change due to self-heating phenomenon has a very important role in the self-healing circuit. Because of the dynamical nature of the self-healing circuit, the current reference output current is also independent from voltage supply changes. It has also been studied that although ZTC biasing of a MOSFET does not compensate for process variations, those variations are degenerated significantly.

This circuit has been designed and also modelled in the Cadence Virtuoso Schematic environment. The simulation results show that the initial bias point of the current reference transistor is converged to the ZTC point and it remains in the ZTC point vicinity after "tracking". Analytical study of the circuit error shows acceptable error in the output current due to temperature variations. The self-healing circuit is connected to a

MOSFET current reference once when it is biasing a basic current mirror and again when it is biasing a current-starved inverter. Output current changes of the current mirror and delay in the inverter decreased surprisingly due to PVT compensation of the self-healing circuit.

Potential future works, which can be done on this research, are mentioned below:

1. Power consumption and power efficiency of this circuit can be estimated by calculation and simulation in order to make it even more suitable for lower voltage applications.
2. Self-Heating phenomenon has not been studied enough in CMOS technology especially in 65nm. Thus, The $R_{th}$ and $C_{th}$ values for self-heating model are not very accurate. Approximating ambient temperature change due to MOSFET current power dissipation could also be studied.
3. Other methods can be used to modify this circuit in order to degenerate process variations as much as possible and also to make it a "resistorless" design.
4. Since the results in this report come from simulations and calculations and there is no fabricated sample, later results will be more solid if the self-healing circuit is fabricated and tested under laboratory standards to have a better conclusion of performance and efficiency of this type of current references.

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# APPENDIX I

Drain Current Estimator Model:

```
`include "discipline.h"
`include "constants.h"



module amp1(tempin, idin, vgin, iout);
input tempin;
input idin;
input vgin;
output iout;
electrical tempin, idin, vgin, iout;
parameter real alphau = -2;
parameter real alphavt = -1.03m;
parameter real ucox = 350u;
parameter real aspect_ratio = 2;
parameter real room_temp = 300;
parameter real vt = 280m;

  analog
    I(iout) <+
pow(V(tempin)/room_temp,alphau)*I(idin)+(ucox/2)*aspect_ratio*pow(V(tempin)/room
_temp,alphau)*(pow(alphavt,2)*pow(V(tempin)-room_temp,2)-
2*V(vgin)*alphavt*(V(tempin)-room_temp)+2*vt*alphavt*(V(tempin)-room_temp));

endmodule
```