DIFFERENTIAL CODE-SHIFTED REFERENCE IMPULSE-RADIO ULTRA-WIDEBAND RECEIVER: SIGNAL STRENGTH ADJUSTMENT AND IMPLEMENTATION

by

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DEDICATION

This thesis is dedicated to my family and friends for their love and support.

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ABSTRACT

IR-UWB is a wireless system, which sends information data with pulses that have rapid rising and falling time and very short duration of nanosecond or less. However, due to varying communication channel conditions, amplitude of the received signal is not at a constant level. Therefore, automatic signal strength adjustment is required to equalize the impact of variations of the channel conditions.

In this thesis, two approaches based on automatic gain control technique are proposed. The first design is a feed-forward automatic gain control system working at baseband. The second design is a feedback automatic gain control system operating at radio or microwave frequency. The corresponding simulation and implementation results are provided to validate the designs. The proposed designs present signal strength controls for impulse-based transceiver systems which are not often addressed in the literature.

It is found that the first design does not work well in reality due to the fact that it essentially operates in the baseband and has no impact on the strong or weak signals right after the receiver antenna. The second design functions quite well and presents a dynamic range of 179mV to 1.062V. As a result, it is the choice of this thesis work.

LIST OF ABBREVIATIONS AND SYMBOLS USED

ADC	Analog-to-digital converter
ADS	Advanced Design System
AWGN	Additive white Gaussian noise
BER	Bit error rate
BPF	Band-pass filter
BW	Bandwidth
CSG	Control signal generator
CSR	Code-shifted reference
DCSR	Differential code-shifted reference
DVGA	Digital variable gain amplifier/attenuator
ECG	Electrocardiogram
EIRP	Equivalent isotopic radiated power
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
FPGA	Field-programmable gate array
FSR	Frequency-shifted reference
GCPW	Grounded coplanar waveguide
HDR	High-data-rate
HDTV	High-definition television
IR	Impulse-radio
ISI	Inter-symbol interference
LDR	Low-data-rate

LNA	Low noise amplifier
MB-OFDM	Multi-band Orthogonal Frequency Division Multiplexing
MBOA	Multiband OFDM Alliance
MPCs	Multipath components
MRC	Maximum ratio combining
OOK	On-off keying
PC	Personal computer
PCB	Printed circuit board
PLL	Phase-locked loop
PRF	Pulse repetition frequency
PRT	Pulse repetition time
PSD	Power spectral density
QPSK	Quadrature phase shift keying
RF	Radio-frequency
SNR	Signal-to-noise ratio
SMA	Sub-Miniature-A
SMT	Surface mount technology
TFI	Time-Frequency Interpolation
TR	Transmit reference
UWB	Ultra-wideband
VGA	Variable gain amplifier
VHDL	Very-high-speed integrated circuit hardware description language

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CHAPTER 1 INTRODUCTION

1.1 MOTIVATION

In wireless communication technology, narrowband systems have played a leading role at least in the past many decades. However, they use limited bandwidth and therefore have limited transmission capacity. With the increasing popularity of mobile communication systems and devices such as mobile phone and Wi-Fi gears, requirement of high transmission capacity and quality becomes very significant. Although many narrowband schemes have been developed to address the issue, they still could not keep pace with the requirement.

As an attempt to break narrowband technology's limitation, ultra-wideband (UWB) technology has been reintroduced to wireless communications recently. Although UWB scheme was already invented in 1960s for military radar, the Federal Communications Commission (FCC) released this technology from military only to commercial use at the specific bandwidth and power level in 2002. By transmit data stream over an ultra-wide range of frequency from DC to GHz, UWB system can achieve high data-rate from hundreds of Mbps to even several Gbps. Due to its potential low power, low cost, low complexity and low interference characteristics, UWB systems have attracted great attention for industrial and research purpose.

As one of the mainstream UWB techniques, the impulse-radio (IR) UWB is a UWB system that sends information data with pulses with rapid rising and falling time and very short duration of nanosecond or less. Among the signaling schemes developed for

the IR UWB transmission, transmit reference (TR) and frequency-shifted reference (FSR) are two most remarkable schemes of IR-UWB; they send a reference pulse that is shifted either in the time domain or in the frequency domain. However, difficulty or high cost to implement them in hardware is their main disadvantage.

Recently, code-shifted reference (CSR) scheme has been introduced by our research group. It shifts the reference pulse from the data pulses by code, which overcomes the technical difficulties faced by the previous schemes and makes the transceiver system easier to implement; it can achieve even better performance than the previous schemes. To further improve the performance and reduce the power consumption, the differential code-shifted reference (DCSR) has been developed. Although the transceiver implementation of DCSR had been completed by our group previously, there are still challenges in signal strength adjustment or automatic gain control at the receiver side in order to equalize channel condition changes. This thesis focuses on solving the issue by proposing the designs, fabricating the circuit and performing the bit error rate (BER) test.

1.2 THESIS OUTLINE

At the beginning of Chapter 2, this thesis briefly introduces the history of UWB, followed by the definition and regulations in the next subsections. Then, different types of UWB transmission are enumerated in the next section. Because this thesis focuses on IR-UWB, only the advantages of IR-UWB are presented. At the end of this chapter, the applications and main challenges are indicated respectively.

In Chapter 3, different IR UWB signaling schemes are described for effective signal detection and recovery. Rake receiver, as an ideal choice to recover UWB signal, is the first one discussed. Then, transmit reference (TR), frequency-shifted reference (FSR), code-shifted reference (CSR) and differential code-shifted reference (DCSR) scheme are presented. Last, a performance comparison among these schemes is shown in this chapter.

Chapter 4 introduces the structure and implementation of the current DCSR IR-UWB transceiver system. The existing gain control scheme in DCSR receiver is also discussed in this chapter.

Chapter 5 proposes two designs for automatic signal strength control, which form the main contribution of this thesis. The first design is a feed-forward automatic gain control circuit working at baseband. The second design is a feedback automatic gain control circuit operating at radio frequency. The simulation and implementation results are provided.

Chapter 6 is the last chapter of this thesis where the conclusion is presented. Potential future work is also indicated in this chapter.

CHAPTER 2 BACKGROUND OF UWB

2.1 OVERVIEW OF UWB

Most people treat UWB as a "new" developed technology with which they are able to enjoy a high download speed when surfing internet or transfer files recently. However, this technology was given the birth as a spark gaps electromagnetic wave generator in 1893 by Heinrich Hertz [1]. In 1901, Gugliemo Marconi invented spark gaps equipment and successfully transmitted Morse code over the Atlantic Ocean wirelessly [2]. Although it was the first wireless communication, due to its limitation on techniques of the time, this pulse-based transmission was gradually replaced by radio technology that is based on sinusoidal continuous waves of narrowband.

The pulse-based transmission reemerged and caught the attention when Gerald F Rose obtained the first UWB communication patent in 1973 [3]. However, the applications of the UWB focus were mainly for impulse radars and other special uses. It is not until 1990s, the alliance of companies started to form to make effort to commercialize UWB technology for public uses [1].

In February of 2002, Federal Communications Commission (FCC) issued the First and Order Report, authorizing frequency band, the power level, application categories for UWB communication, and releasing the technology for unlicensed commercial uses [4].

2.2 UWB DEFINITION AND REGULATIONS

2.2.1 UWB DEFINITION

According to FCC's definition, UWB system is a radio system whose signal has a -10dB fractional bandwidth (B_f) greater than 20% of its center frequency (f_c) or a -10dB absolute bandwidth (BW) greater than 500MHz, as shown in Equation (2.1) and Equation (2.2):

$$B_f = \frac{BW}{f_c} = 2\frac{f_h - f_l}{f_h + f_l} > 20\% \qquad (2.1)$$

$$BW = f_h - f_l > 500MHz \qquad (2.2)$$

where f_h is the high frequency bound, and f_l is the low frequency bound at which points the spectral power of the signal has a decrease of 10dB from its highest value, as shown in Figure 2.1 [4].

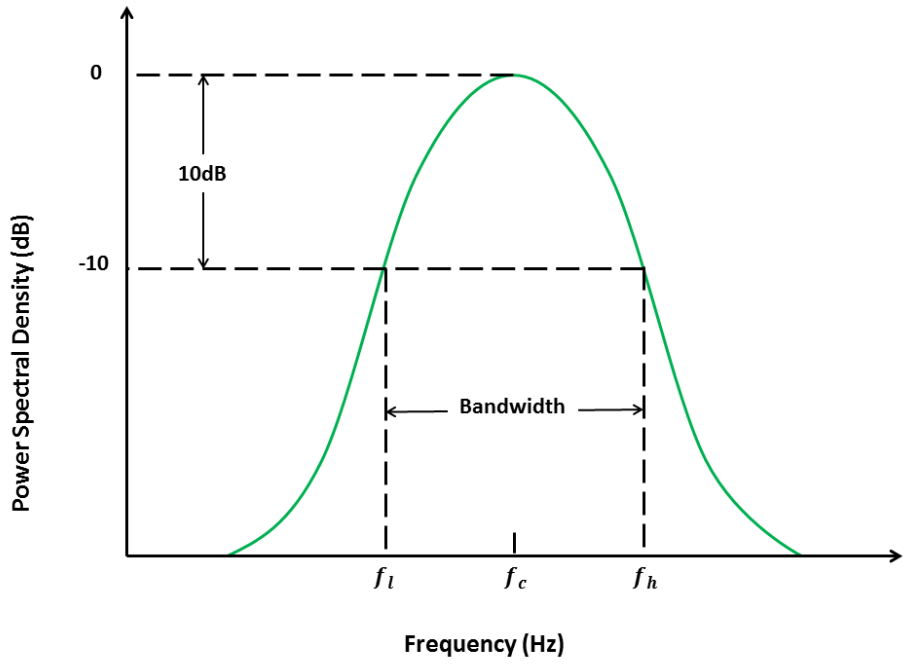


Figure 2.1 Definition of -10dB Bandwidth

2.2.2 UWB REGULATIONS

In its report, FCC also limits the emission levels of the UWB systems, in order to ensure that no interference would be introduced to the environment in which UWB systems are coexisting with other wireless communication systems. Two unlicensed frequency bands for UWB transmission are allowed: one is from DC to 960MHz and the other is from 3.1GHz to 10.6GHz. Owing to the fact that a part of its frequency band is overlapping with existing narrowband systems, UWB signals are specified to transmit with a lower power spectral density (PSD) which is defined by Equation (2.3).

$$PSD = \frac{P_t}{BW} \qquad (2.3)$$

where P_t is the transmission power and BW is the bandwidth of the UWB signal.

In FCC's report, the equivalent isotropic radiated power (EIRP) spectral density of UWB is limited to 41.3dBm/MHz (74×10^{-6}mW/MHz) or lower. Assuming that a UWB signal is transmitted and is occupying all the unlicensed frequency band of 7.5GHz (=10.6GHz-3.1GHz), the total consumed power is approximately 0.56mW ($=74\times10^{-6}$mW/MHz×7500MHz), which is even lower than the noise floor of a narrowband signal. As a result, it presents to narrowband systems not interferences but noises [4]. Figure 2.2 and Figure 2.3 show the FCC emission masks for UWB communication systems in indoor and outdoor environments, and Table 2.1 shows detailed EIRP limitations at each frequency level.

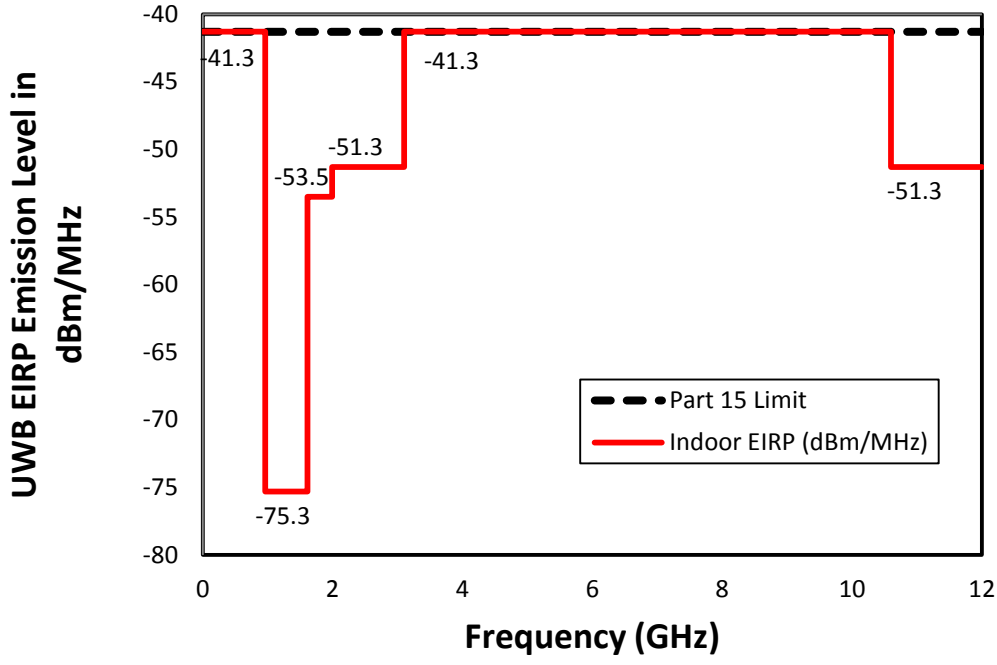


Figure 2.2 FCC emission mask for indoor UWB systems [5]

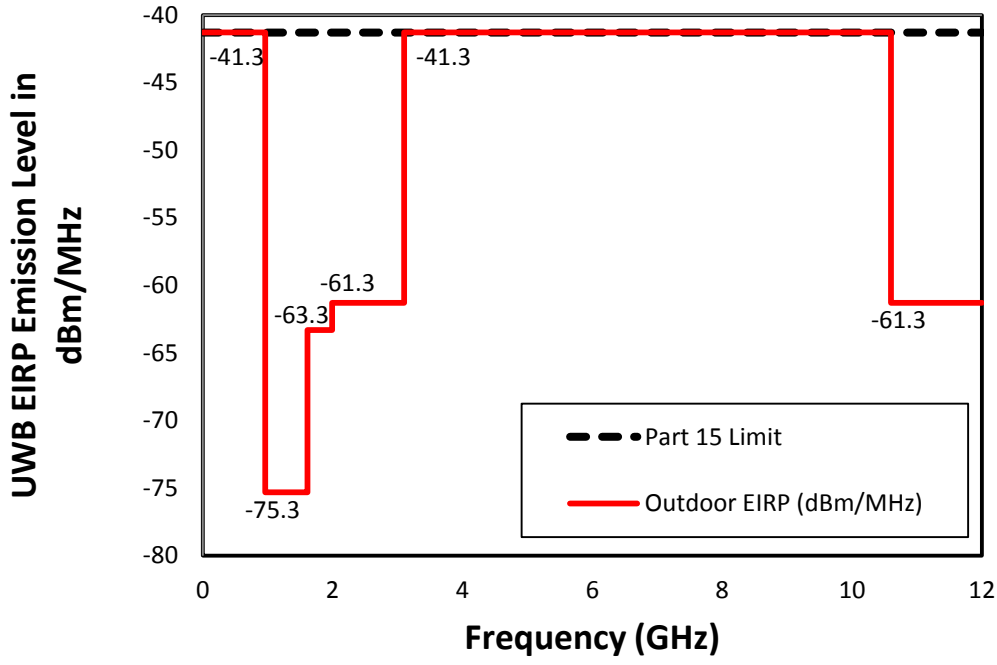


Figure 2.3 FCC emission mask for outdoor UWB systems [5]

Frequency (MHz)	Indoor EIRP (dBm/MHz)	Outdoor EIRP (dBm/MHz)
0-960	-41.3	-41.3
960-1610	-75.3	-75.3
1610-1990	-53.5	-63.3
1990-3100	-51.3	-61.3
3100-10600	-41.3	-41.3
Above 10600	-51.3	-61.3

Table 2.1 FCC emission limits for indoor and outdoor UWB systems [6]

It is noteworthy that the first frequency band (DC - 960MHz) is often used for low data-rate transmission, while the second frequency band (3.1GHz-10.6GHz) is frequently employed in communication systems [7]. This thesis deals with the applications of the second band.

2.3 TYPES OF UWB TRANSMISSION

FCC released UWB uses to public and regulated its operating bandwidth of 500MHz and maximum PSD of -41.3dBm/MHz. It didn't specify particular signaling technologies. Therefore, several different schemes are developed to implement UWB transmission. In general, multi-band orthogonal frequency division multiplexing (MB-OFDM) and impulse-radio (IR) UWB are two typical approaches in the research field of UWB transmission. The research of this thesis is based on IR-UWB technique; thus, a succinct introduction of MB-OFDM will be provided, and then a detailed introduction of IR-UWB will be made.

2.3.1 MB-OFDM UWB

OFDM technology has been applied in both wire and wireless systems for decades. The main idea of OFDM is to divide the whole channel to several orthogonal sub-channels; thus, the high data-rate signal could be converted into parallel low data-rate signal flow and modulated to sub-channels to transmit. An alliance called Multiband OFDM Alliance (MBOA), led by Intel, TI and Panasonic, has developed OFDM from traditional

multi-carrier modulation into UWB appliances. To meet the 500MHz bandwidth requirement, MBOA divides the whole 7.5GHz frequency band from 3.1GHz to 10.6GHz to 14 sub-channels (or bands) with the bandwidth of 528MHz for each sub-channel. All these 14 sub-channels are not overlapping with each other. Furthermore, OFDM divides these 14 sub-channels into 5 groups: the first four groups have 3 sub-channels in each, while the last group has the last two sub-channels [8]. Quadrature phase shift keying (QPSK) modulation is used for constellation mapping; a 128-point digital Fast Fourier Transform (FFT) is used to generate the QPSK carriers [9]. Figure 2.4 shows the MB-OFDM Channel allocation.

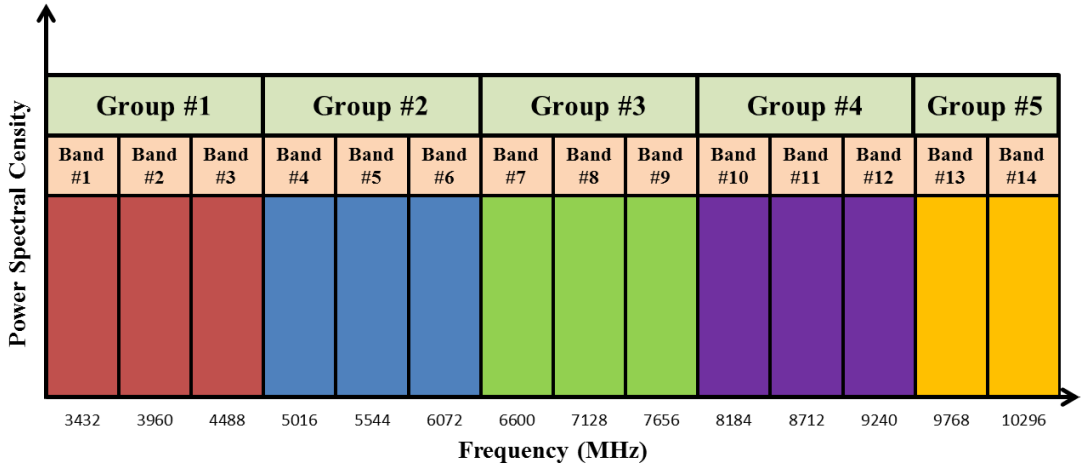


Figure 2.4 MB-OFDM Channel allocation [10]

The first band group, of which the frequency is from 3168MHz to 4752MHz, is mandatory for minimal systems design; all others are selectable and are remained for future development. The advantage of this setting is that MB-OFDM systems could keep in a better position to avoid interference with existing narrowband communication systems: if interference happens in the current transmission channel, the system can

simply skip to another channel which is free by using the time-frequency interpolation (TFI) technology [6] [9] [11].

MB-OFDM is a flexible scheme that can achieve different data rates by changing the coding rates and choosing different combinations of channels. In addition, it can also reduce the inter-symbol interference (ISI) and increase the ability of multipath tolerance, since the dwell time to transmit a symbol on an individual sub-channel can be long [9] [11].

Although MB-OFDM is a mature technology, it has the issue of being complex in implementation and relatively high in power consumption. Components, such as fast analog-to-digital converters (ADC), Viterbi decoders and Fast Fourier Transform (FFT) engines, are all needed which certainly increase the complexity [12].

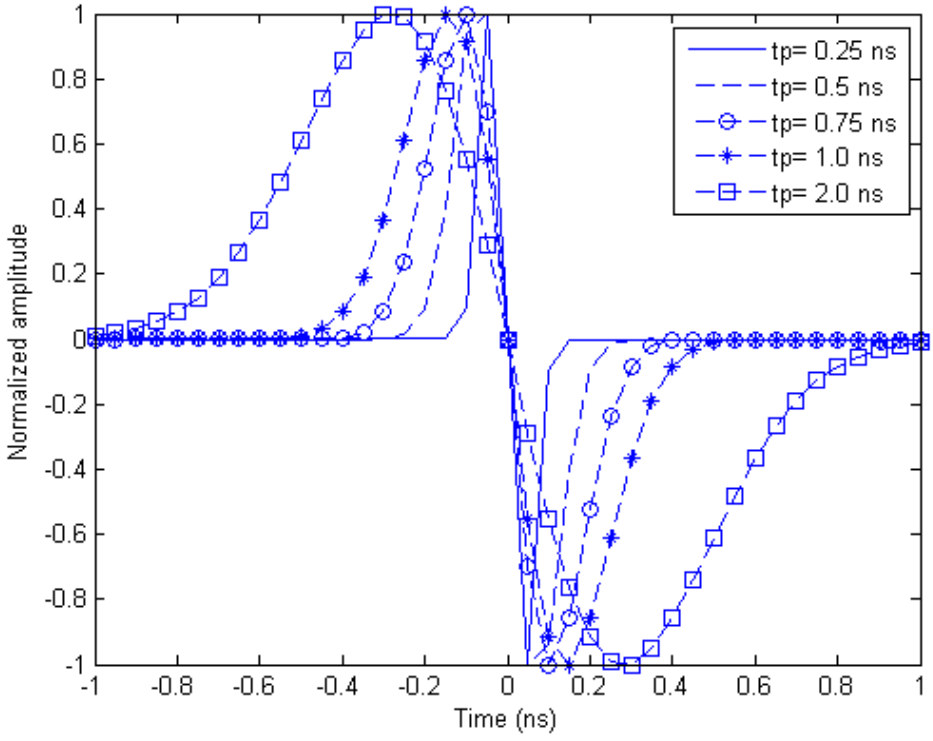
2.3.2 IR-UWB

Unlike MB-OFDM, which processes with continuous signals in the time domain, IR-UWB technology handles discontinuous signals or discrete pulses. In addition, IR-UWB has no need for supererogatory carrier modulation when transmitting in the radio channel [6]. Therefore, discrete pulses are the core of this signaling technology. In generating these pulses, factors such as pulse spectral bandwidth, pulse peak transmission power and pulse shape need to be carefully considered.

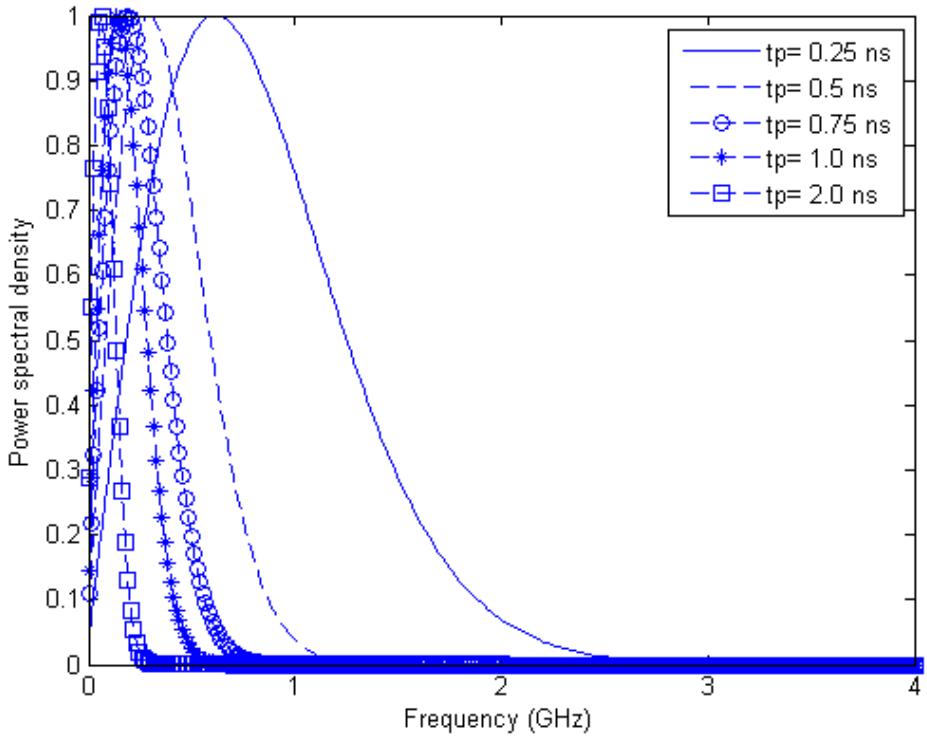
There is an approximate inverse correlation between the duration of the pulses (τ) and their spectral bandwidth (BW): the shorter the duration, the wider the bandwidth, and vice versa. Equation (2.4) can express this relationship:

$$\tau \approx \frac{1}{BW} \qquad (2.4)$$

IR-UWB pulses have very short durations in the time domain, for example, in the order of nanosecond (ns), which promise ultra-wide spectral bandwidth to meet FCC's 500MHz minimum bandwidth requirement. Figure 2.5 shows Gaussian monocycle pulses in the time domain (a) and in the frequency domain (b) [6].



(a)



(b)

Figure 2.5 Gaussian monocycle in (a) the time domain and (b) the frequency domain [6]

FCC specified the maximum PSD is -41.3dBm/MHz; therefore, a tradeoff should be made between the peak transmission power ($P_{T,peak}$) and the pulse repetition frequency (PRF). Their relationship is represented by Equation (2.5) [14]:

$$P_{T,peak} = \frac{PSD \times BW}{PRF \times \tau} \qquad (2.5)$$

where BW is pulse bandwidth and τ is the pulse duration. In order to satisfy FCC emission limits, $P_{T,peak}$ should be low when PRF is high, or $P_{T,peak}$ should be high

when PRF is low. $P_{T,peak}$ can also be converted to amplitude in voltage; the relation is [15]:

$$P_{T,peak} \propto V^2 \tag{2.6}$$

Pulse shape is closely related to energy efficiency. The smoother a pulse has in its rising and falling edges, the fewer side lobes it has in frequency domain; it means that less energy is wasted to undesired bands. Therefore, by choosing appropriate pulse shape, IR-UWB system is able to achieve higher energy efficiency to realize the best performance under FCC emission limits. For this purpose, Gaussian pulse, Rayleigh monocycle, Manchester monocycle and Hermite pulse are the most common pulse shapes used for IR-UWB transmission; among them, Gaussian pulse is the most popular one owing to its advantage of easy generation [1] [9]. Equation (2.7) and Equation (2.8) present the basic Gaussian waveform and its n-order derivatives in the time domain; Figure 2.6 shows different n-order Gaussian monocycles in time domain (a) and frequency domain (b), where t_p is the effective width of the pulse [13].

$$w_0(t; t_p) = e^{-2\pi(\frac{t}{t_p})^2} \tag{2.7}$$

$$w_n(t; t_p) = \frac{d^{(n)}}{dt^n}(e^{-2\pi\left(\frac{t}{t_p}\right)^2}) \tag{2.8}$$

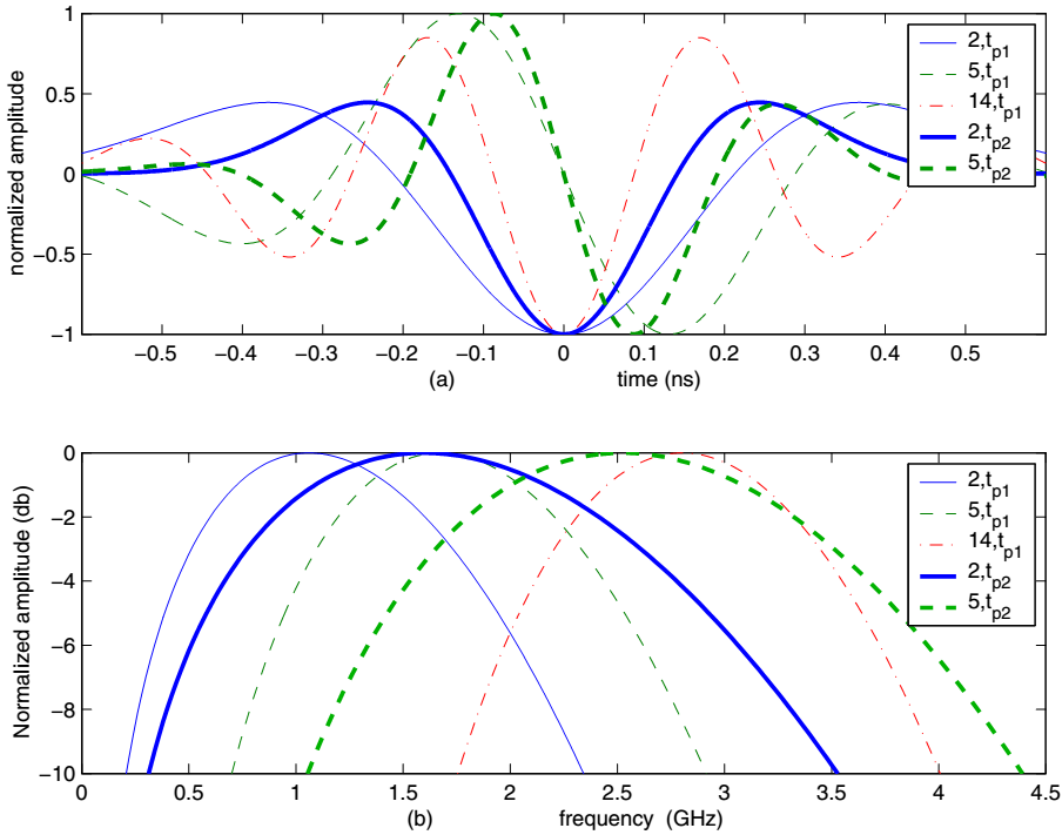


Figure 2.6 (a) Time domain waveforms and (b) frequency spectrum of n-order Gaussian monocycles, where t_{p1}*= 0.7521ns,* n *= 2, 5, 14;* t_{p2}*= 0.5ns,* n *= 2, 5 [13]*

Obviously, when n is increased and t_p remains unchanged, the spectrum of Gaussian monocycles moves to higher frequency but the bandwidth remains largely unchanged; when t_p is increased and n remains unchanged, the spectrum of Gaussian monocycles moves to lower frequency and the bandwidth is reduced. Therefore, by controlling the order n and the pulse width t_p we can generate desired UWB pulses [13].

2.4 ADVANTAGES OF IR-UWB

IR-UWB systems have many significant advantages that make it an effective alternative to MB-OFDM UWB and attract attention. These advantages are elaborated below.

The most noticeable advantage of IR-UWB is its potential high transmission capacity or data rates due to its fairly wide bandwidth. According to Shannon, the maximum channel capacity (C) has a linear relationship with the channel bandwidth (BW) [16]:

$$C = BW\ log_2(1 + \frac{S}{N}) \qquad (2.9)$$

where $\frac{S}{N}$ is the signal-to-noise ratio (SNR). Owing to the wide bandwidth BW which can be hundreds of MHz to several GHz, the achievable data rates can range from hundreds of Mbps to even Gbps with fixed SNR. With fixed data rates, reliable transmission can be achieved with low SNR.

Moreover, IR-UWB systems have flexible adjustability between data rates and transmission distance. The pulse repetition time (PRT, which is the reciprocal of PRF) is directly proportional to the time of one data bit, as expressed in Equation (2.10):

$$t_d = N \times PRT \qquad (2.10)$$

where N is the number of pulses per data bit. PRT is generally much longer than the pulse duration (τ); therefore, N is frequently increased to achieve high SNR. With doubled N, the SNR is doubled as well, which provides extra 6dB in communication link budget allowing longer transmission distance. Figure 2.7 shows the relationship

between t_d and PRT. However, it is important to note that N cannot be increased at will, since it may result in unwanted pulse aliasing and excessive PSD; the only solution is to extend t_d, which leads to low data rates [6]. In other words, the lower the data rates, the longer transmission distance, and vice versa.

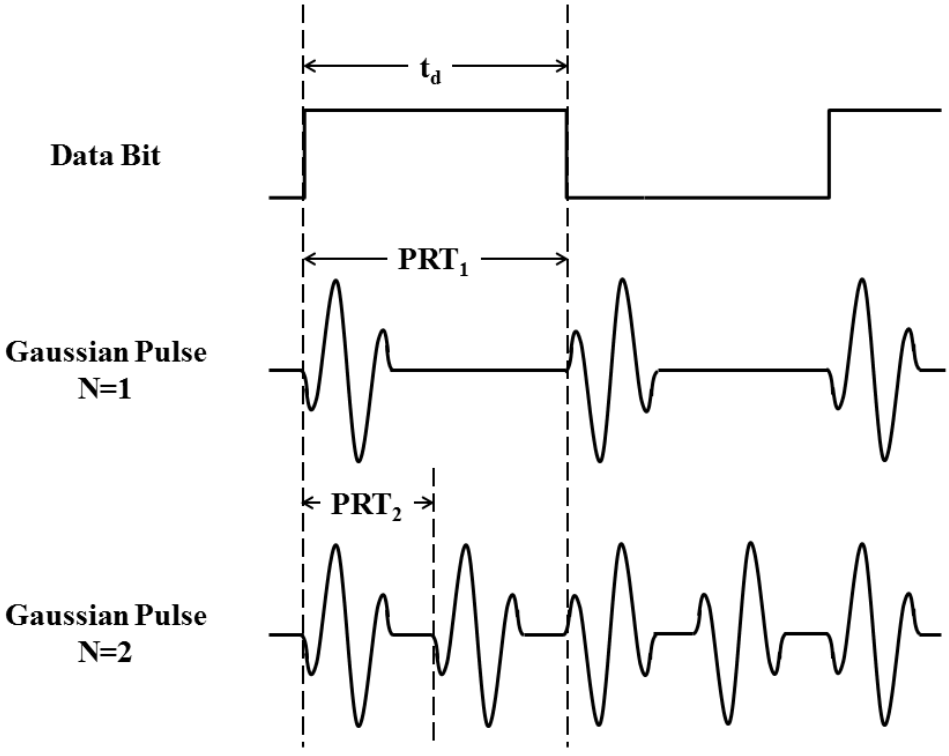


Figure 2.7 The relationship between t_d and PRT

High communications security is also a benefit of IR-UWB. Since UWB signals have PSD which is lower than the noise floor of narrowband signals, not only will narrowband systems treat IR signals as noise instead of interferences, but also it is difficult or

impossible to intercept IR-UWB signals. Therefore, for secure and military applications, IR-UWB technology is an appropriate choice [6].

Furthermore, IR-UWB signals can be made very resistant to multipath interferences. Multipath is known as a radio signal emitted from the transmitter, then arriving at receiver through different paths which may form destructive interferences to each other. The cause of multipath is that, in real transmission environment, there are objects located between the transmitter and the receiver; they cause unwanted reflection, absorption, diffraction and scattering of a transmitted signal. Signals traveling over various different paths then arrive at the receiver at different times or different phases in frequency domain; hence the signal captured by the receiver suffers multipath interference [1]. Multipath is particularly prominent in indoor transmission environments. Figure 2.8 shows this phenomenon.

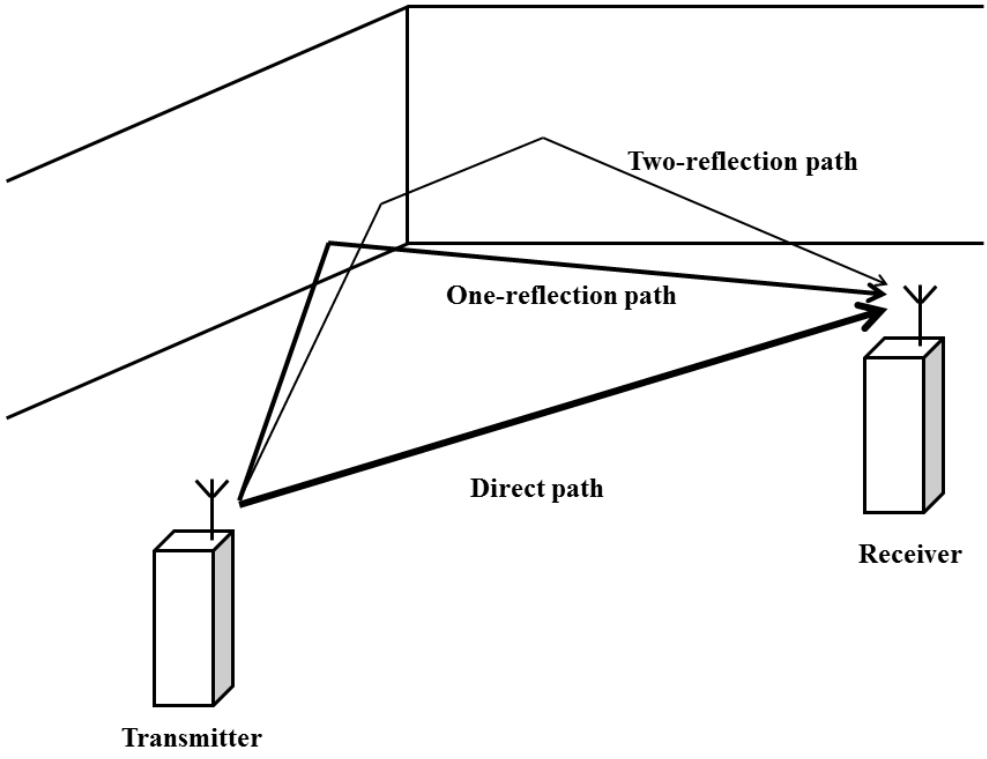


Figure 2.8 Typical multipath phenomenon in indoor environment [1]

Only overlapping pulses at receiver will cause interference problems; namely, if the received pulses are not overlapped with each other, the multipath effect can be resolved. The shorter duration of the pulse, the smaller chance of the pulse overlapping. Therefore, the extremely narrow pulse width of IR-UWB signal, in the order of nanosecond, makes the radio system possible to highly resistant to multipath interference [1].

Low power consumption is another outstanding characteristic of radio systems using IR-UWB technology. The maximum -41.3dBm/MHz PSD determines that IR-UWB systems cannot consume a large amount of power. Besides that, data is modulated on

discontinued nanosecond-order baseband pulses for transmission, which means neither modulator nor demodulator is required in transceiver circuits; hence power consumption decreases further [1].

2.5 APPLICATIONS

Due to its many significant benefits, IR-UWB technology has been found good applications. It could be used for both high-data-rate (HDR) short-distance and low-data-rate (LDR) long-distance applications. In general, UWB has three distinct application areas: imaging, positioning and high-speed wireless communication [2] [17]. Some examples are illustrated below:

a. Electrocardiogram (ECG): in biology science, UWB's accurate measurement and positioning ability makes it possible to detect patient's breath and heartbeat without using any electrode or transducer to touch the patient's body.

b. Smart home: UWB can be used to build an effective network to combine all the home appliances together, such as high-definition television (HDTV), personal computer (PC) and even smart refrigerator.

c. Portable device: due to its high data rates and low power consumption, UWB technology is quite suitable for portable devices to transfer large size files such as high quality images, music, and even videos, without losing their mobility.

2.6 CHALLENGES

As described before, IR-UWB technology has of its reasons to be attractive and promising. However, there are still some challenges standing in the way. The most significant one is the undetermined regulation. Users can design and implement their own IR-UWB systems over the whole frequency band; they may interfere with each other [1].

Hardware design is another area that needs attention. For IR-UWB transceivers, devices working on radio frequency (RF), such as nanosecond-pulse generators, UWB antennas, UWB low noise amplifiers and so on, present stringent requirements to specific circuit design comparing to narrowband circuits.

CHAPTER 3 IR-UWB TRANSCEIVING SCHEMES

For IR-UWB technology, effective detection and recovery of the signal are always the challenges, since the duration of transmitted pulses is very short. As a result, effective transceiving schemes or technologies are needed. In this chapter, different schemes are illustrated.

3.1 RAKE RECEIVER

An effective way to recover UWB signals is to correlate the received signal with the known transmitted pulse waveform [18]; Rake receiver is the ideal one. The idea of Rake receiver is to combine multipath components by correlation; thus the signal to noise ratio (SNR) can be increased and performance of the system can be improved. The ideal Rake receiver, or called all rake (I-rake or A-rake), captures every achieved signal component (including multipath) with detection fingers that have the same number as the multipath components (MPCs), as shown in Figure 3.1. If the maximum ratio combining (MRC) is adopted, the performance, which is as good as that of AWGN channel, can be achieved. However, it is impossible to implement this approach under real environment since the number of fingers has to be infinite in order to capture the possible infinite number of multipath components. In addition, channel estimation is required for pulse correlation [6], which can be hard to do.

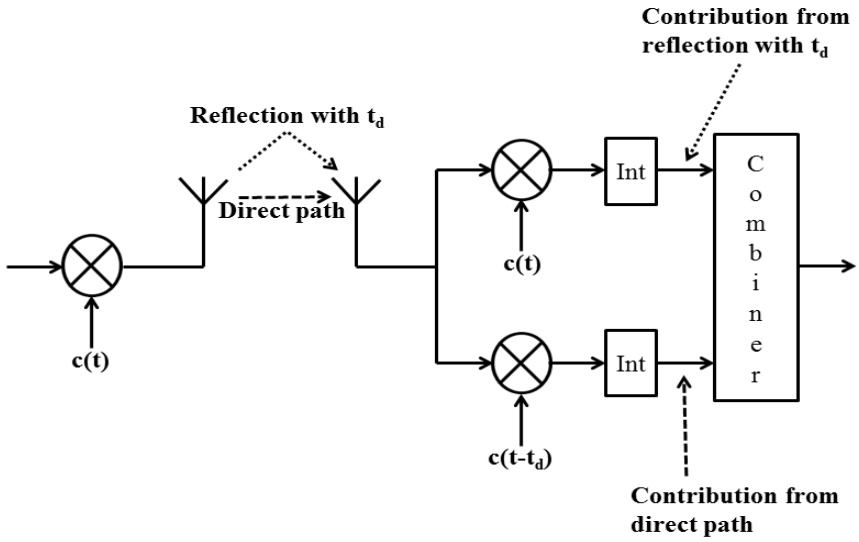
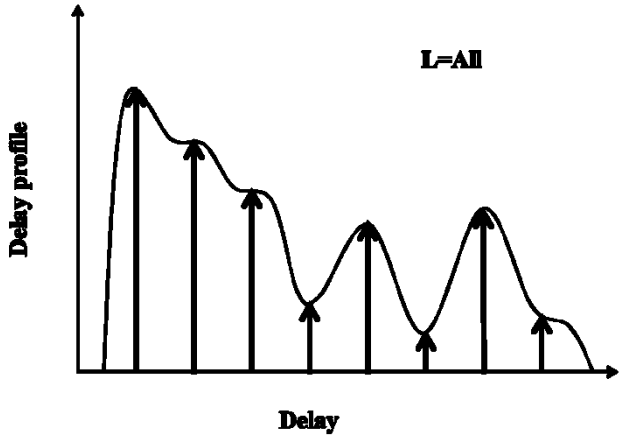


Figure 3.1 General Rake receiver structure (with two MPCs) [19]

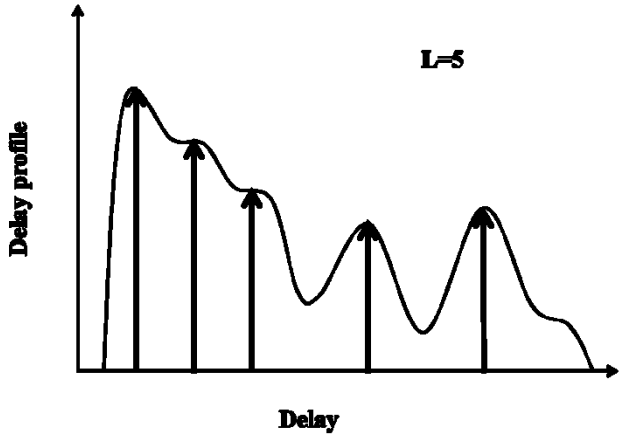
In practice, only the finite *L* multipath components of the strongest amplitudes are captured and processed, resulting in less than optimal performance. In other words, selective rake and partial rake (S-rake and P-rake) are those implemented realistically for Rake receiver. The S-rake only picks up the *L* strongest MPCs. The P-rake is a simplified version of S-rake by assuming that the first *L* MPCs are the strongest and then picking them up. Therefore, the main disadvantage of P-rake is that if the first *L* is not the strongest, the performance of the receiver will degrade [6]. Figure 3.2 shows a comparison between the operational principles of A-rake, S-rake and P-rake.

Although the above Rake receivers works well in theory, it has its biggest problem: to implement Rake receiver, channel estimation, multipath acquisition and tracking

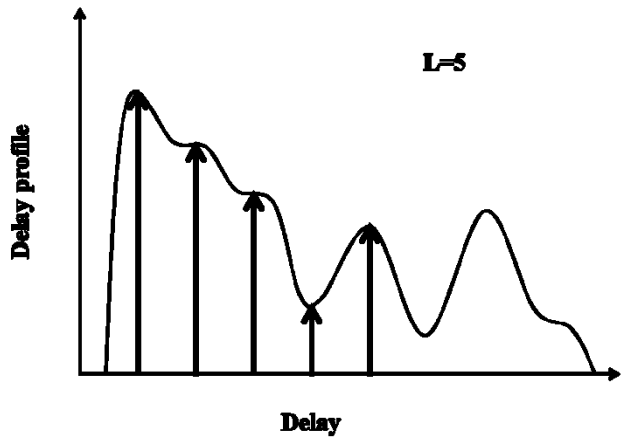
operations are necessary for each finger to match the amplitude, phase and delay of each MPC. It undoubtedly will make the implementation very complex and expensive [1] [6] [20].



(a)



(b)



(c)

Figure 3.2 Comparison between the principles of (a) A-rake, (b) S-rake and (c) P-rake [6]

To circumvent the problems Rake receivers inherently have, non-coherent receivers, using envelope detection or energy detection to avoid channel estimation, were introduced. They are elaborated below.

3.2 TRANSMIT REFERENCE (TR) IR-UWB

Transmit reference (TR) is a typical autocorrelation receiver. The basic principle of transmit reference is to transmit an un-modulated reference pulse and a modulated data pulse in pairs with a short delay time d between them. While the delay is shorter than the channel coherent time (i.e. the duration in which the channel impulse response has the same characteristics), both the reference pulse and the data pulse suffer the same distortion when they arrive at the receiver. Therefore, the data pulse can be demodulated by correlating with the paired reference pulse [2] [21]. Figure 3.3 shows the block

diagram of a typical TR receiver. Figure 3.4 shows the demodulation procedure of TR receiver.

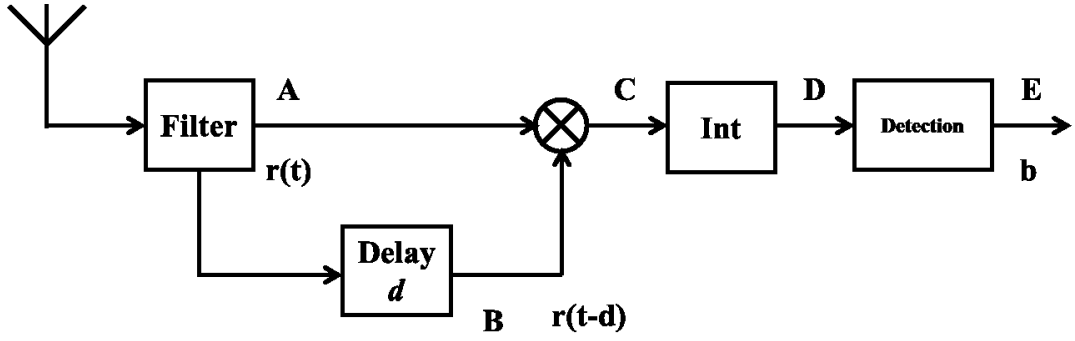


Figure 3.3 The block diagram of a typical TR receiver [2]

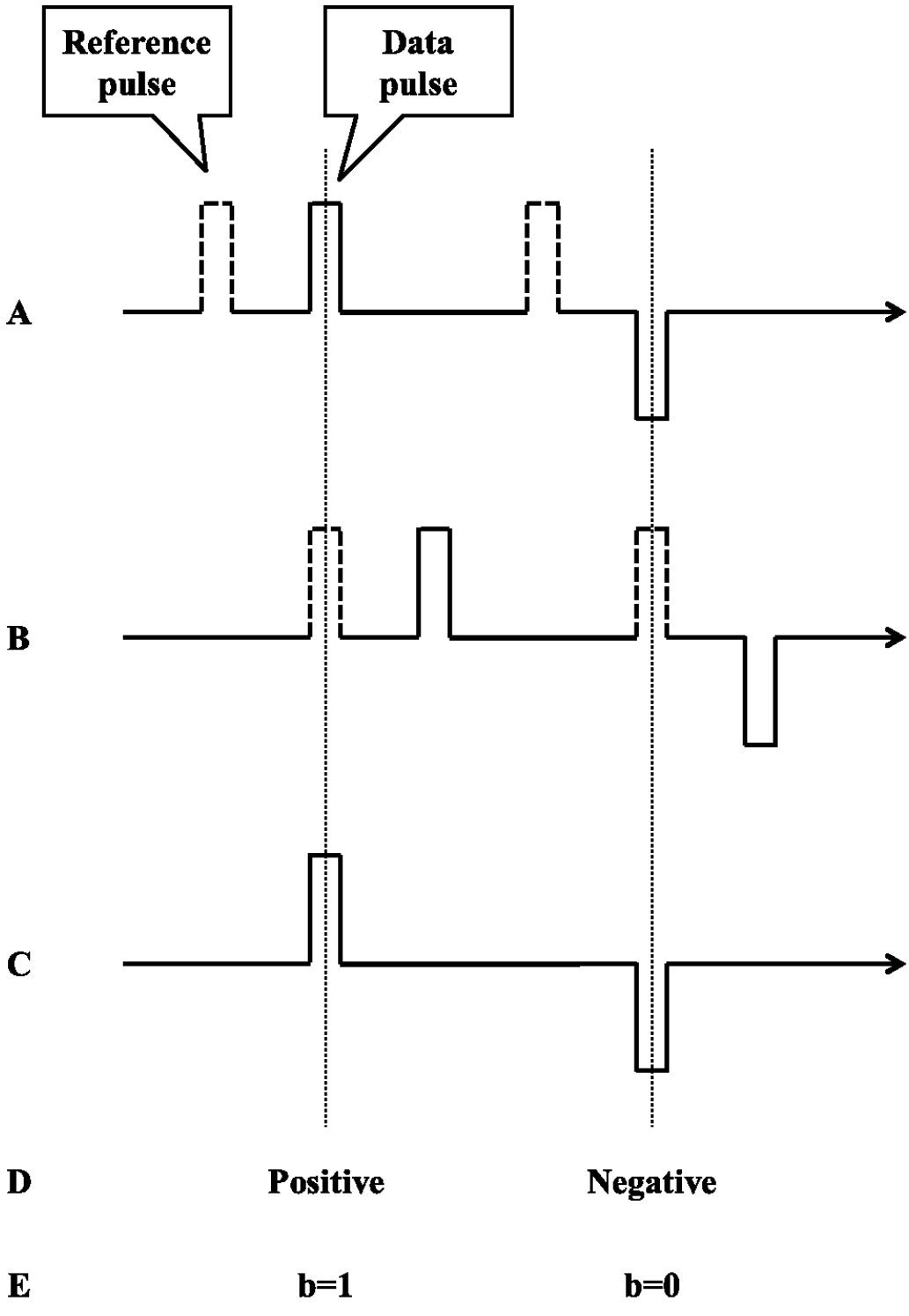


Figure 3.4 The demodulation procedure of TR receiver [2]

Although TR receiver removes the requirement of channel estimation, it suffers from a major problem. As a key component, the delay element has to be implemented accurately. However, even with current techniques it is difficult to realize the delay of such an ultra-wideband in the integrated circuit environment [22].

3.3 FREQUENCY-SHIFTED REFERENCE (FSR) IR-UWB

As an improvement of TR receiver, frequency-shifted reference (FSR) scheme was proposed. Different from the TR scheme where a reference pulse is shifted from a data pulse in the time domain, the reference pulse is now shifted from the data pulse in the frequency domain. As a result, FSR does not need the ultra-wideband delay. Instead, the frequency offset f_0 between the reference and data pulses is made smaller than the channel coherent bandwidth and it can be represented by Equation (3.1):

$$f_0 = \frac{1}{T_s} = \frac{1}{N_f T_f} \qquad (3.1)$$

where T_s is the duration of one symbol, N_f is the number of frames per symbol, T_f is the duration of one frame containing one data pulse [22].

In FSR, at the transmitter one or more data pulse sequences are transmitted and accompanied by one reference pulse sequence, with each data pulse sequence shifted slightly from the reference pulse sequence in frequency offset f_0; at the receiver, the reference pulse sequence is shifted by the same frequency offset and correlated to recover the information from the data pulse sequence [22]. Figure 3.5 shows the block diagram of a typical FSR receiver.

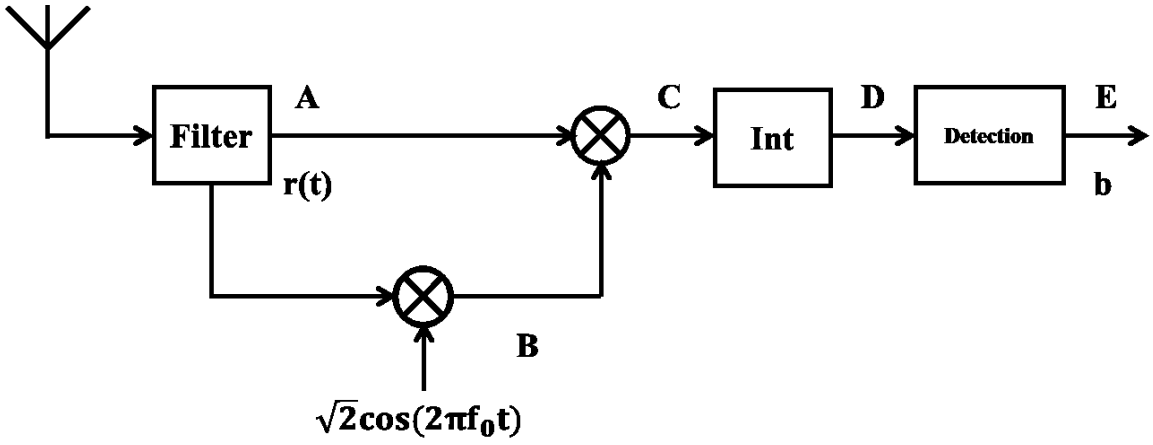


Figure 3.5 The block diagram of a typical FSR receiver [22]

Since FSR shifts the reference pulse in the frequency domain, analog carrier is required. The introduction of analog carrier may cause several problems, such as frequency errors due to oscillator mismatch, phase errors due to multipath fading and amplitude errors due to non-linear amplifiers [20]. As a result, practical implementation of FSR becomes challenging.

3.4 CODE-SHIFTED REFERENCE (CSR) IR-UWB

Different in shifting the reference pulse in the time domain or in frequency domain, code-shifted reference (CSR), which shifts the reference pulse by codes, was proposed for IR-UWB transceiver. At the transmitter, CSR transmits one reference pulse sequence and one or more data pulse sequences together, separated by selected shifting codes. At the receiver, the related detection codes are used to decode and recover the data pulse sequences from the received coded sequences. Since CSR employs the code-shifting technique rather than time-shifting or frequency-shifting, neither the delay element

required by TR transceiver nor the analog carrier required by FSR transceiver is needed anymore. In the other words, both the implementation complexity and the probability of transmission errors can be reduced [20].

3.4.1 THE STRUCTURE OF CSR TRANSMITTER

The CSR signal $x(t)$ transmitted at the end of the transmitter can have a mathematic expression:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} p\left[t - \left(jN_f + i\right)T_f\right]\left|\sqrt{M}c_{i0} + \sum_{k=1}^{M} b_{jk}c_{ik}\right| \qquad (3.2)$$

where $p(t)$ is the basic IR-UWB pulse which has a duration of T_p and a frequency band from W_L to W_H, T_f is the duration of one frame between two pulses, N_f is the number of total frames, b_{jk} is the k^{th} information bit which is transmitted during the j^{th} N_fT_f duration, c_{ik} is the i^{th} bit of the k^{th} selected shifting codes, M is the number of the data pulse sequences transmitted simultaneously with one reference pulse sequence. Both b_{jk} and c_{ik} have a value of 1 or -1. Obviously, $M + 1$ shifting codes are used to transmit M data pulse sequences. The following matrix can express the shifting codes [20]:

$$\begin{bmatrix} \boldsymbol{c_0} \\ \vdots \\ \boldsymbol{c_k} \\ \vdots \\ \boldsymbol{c_M} \end{bmatrix} = \begin{bmatrix} c_{00} & \cdots & c_{i0} & \cdots & c_{(N_f-1)0} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ c_{0k} & \cdots & c_{ik} & \cdots & c_{(N_f-1)k} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ c_{0M} & \cdots & c_{iM} & \cdots & c_{(N_f-1)M} \end{bmatrix} \qquad (3.3)$$

The general structure of CSR IR-UWB transmitter is indicated in Figure 3.6.

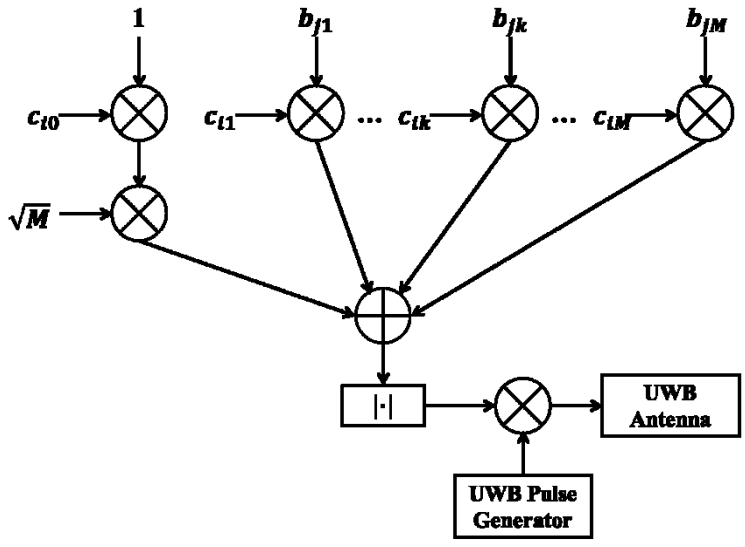


Figure 3.6 The general structure of CSR IR-UWB transmitter [20]

It should be noted that M is limited by the number of total frames N_f with the relationship $M = 2^{N-1}$ where $N_f = 2^N$. In the other words, with $N_f = 2^N$, the maximum number of information bits that can be transmitted at the same time is $M = 2^{N-1}$ [20].

3.4.2 THE STRUCTURE OF CSR RECEIVER

Figure 3.7 illustrates the general structure of CSR IR-UWB receiver. $r(t)$ is the received signal that contains not only the original transmitted signal $x(t)$, but also the noise and interference components coming from the channel. After a band-pass filter (BPF), the filtered signal $\tilde{r}(t)$ is obtained from $r(t)$ without the noise and interference which are out of the frequency band of the signal of W_L to W_H. Then, $\tilde{r}(t)$ is squared and integrated during the duration of T_M, which varies from T_p to T_f due to the possible delay under different transmission conditions such as an additive white

Gaussian noise (AWGN) channel or a severe-delay-spread multipath channel. Next, r_{ij} is obtained and decoded with the M detection codes related to the shifting codes used at the transmitter [20].

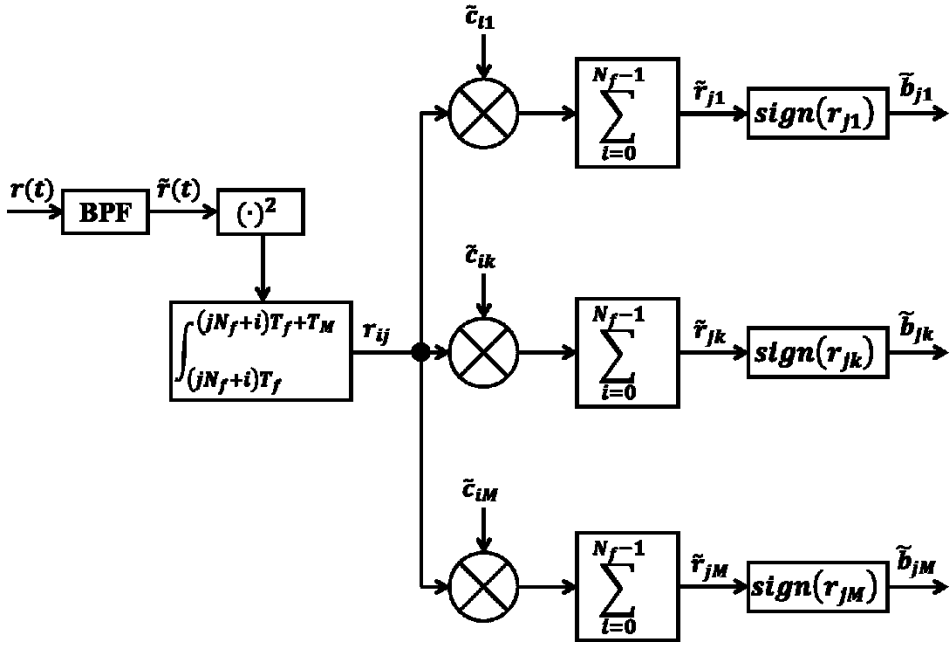


Figure 3.7 The general structure of CSR IR-UWB receiver [20]

The detection codes are expressed in the following matrix:

$$\begin{bmatrix} \tilde{c}_0 \\ \vdots \\ \tilde{c}_k \\ \vdots \\ \tilde{c}_M \end{bmatrix} = \begin{bmatrix} \tilde{c}_{00} & \cdots & \tilde{c}_{i0} & \cdots & \tilde{c}_{(N_f-1)0} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0k} & \cdots & \tilde{c}_{ik} & \cdots & \tilde{c}_{(N_f-1)k} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0M} & \cdots & \tilde{c}_{iM} & \cdots & \tilde{c}_{(N_f-1)M} \end{bmatrix} \quad (3.4)$$

After the decoded signals are added, the sign of the result $\tilde{r}_{jk}$ presents the information bit as logic "1" or "0" [20], as determined by Equation (3.5):

$$\tilde{b}_{jk} = \begin{cases} 1, if\ sign(r_{jk}) > 0 \\ 0, if\ sign(r_{jk}) < 0 \end{cases} \quad (3.5)$$

3.4.3 SELECTION OF THE SHIFTING AND DETECTION CODES IN CSR SYSTEMS

To detect the CSR signals, the shifting and detection codes should meet the two following conditions:

$$\tilde{c}_k = c_0 c_k, \forall k \in \{1, 2, \cdots, M\} \quad (3.6)$$

$$c_1 c_n \neq \tilde{c}_k, \forall k, l, n \in \{1, 2, \cdots, M\} \quad (3.7)$$

One of the possible codes is Walsh Codes. Table 3.1 gives an example of the shifting and detection codes for CSR algorithm coming from an example of Walsh codes [20].

Code Length	Shifting Codes	Detection Codes
$N_f = 2$	$\boldsymbol{c_0} = [1, \ 1]$ $\boldsymbol{c_1} = [1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{1}} = [1, -1]$
$N_f = 4$	$\boldsymbol{c_0} = [1, \ 1, \ 1, \ 1]$ $\boldsymbol{c_1} = [1, -1, \ 1, -1]$ $\boldsymbol{c_2} = [1, \ 1, -1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{1}} = [1, -1, \ 1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{2}} = [1, \ 1, -1, -1]$
$N_f = 8$	$\boldsymbol{c_0} = [1, \ 1, \ 1, \ 1, \ 1, \ 1, \ 1, \ 1]$ $\boldsymbol{c_1} = [1, -1, \ 1, -1, \ 1, -1, \ 1, -1]$ $\boldsymbol{c_2} = [1, \ 1, -1, -1, \ 1, \ 1, -1, -1]$ $\boldsymbol{c_3} = [1, \ 1, \ 1, \ 1, -1, -1, -1, -1]$ $\boldsymbol{c_4} = [1, -1, -1, \ 1, -1, \ 1, \ 1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{1}} = [1, -1, \ 1, -1, \ 1, -1, \ 1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{2}} = [1, \ 1, -1, -1, \ 1, \ 1, -1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{3}} = [1, \ 1, \ 1, \ 1, -1, -1, -1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{4}} = [1, -1, -1, \ 1, -1, \ 1, \ 1, -1]$

Table 3.1 An example of the selected Walsh Codes for CSR algorithm [20]

3.5 DIFFERENTIAL CODE-SHIFTED REFERENCE IR-UWB

Since it has to spend half of the transmission power on transmitting the reference pulse sequence, CSR could only achieve the performance similar to the TR system, which is lower than the Rake receiver. To increase the power efficiency and improve the performance, an advanced scheme of the CSR system, called the differential code-shifted reference (DCSR) scheme, has been developed [23]. It is elaborated below.

3.5.1 THE STRUCTURE OF DCSR TRANSMITTER

DCSR transmitter can transmit one or more data pulse sequences at the same time. The only difference is that the data pulse sequence in DCSR is differentially encoded by the previous data pulse sequence; in the other words, one data pulse sequence is used as the reference pulse for the data pulse sequence following the previous one. As a result, the power consumption on transmitting the reference pulse sequence can be reduced from half of the transmission power to $\frac{1}{M+1}$ when M information bits are transmitted simultaneously. The mathematic expression of the transmitted DCSR signal is shown in the following equation [23]:

$$x(t) = \sum_{j=-\infty}^{\infty} \sum_{i=0}^{N_f-1} p\left[t - \left(jN_f + i\right)T_f\right] \left| \sum_{k=0}^{M} d_{jk} c_{ik} \right| \qquad (3.8)$$

where $p(t)$ is the basic IR-UWB pulse which has a duration of T_p and a frequency band from f_L to f_H, T_f is the duration of one frame between two pulses, N_f is the number of total frames, d_{jk} is the differentially encoded information bit, c_{ik} is the i^{th}

bit of the k^{th} selected shifting codes, and M is the number of information bits transmitted simultaneously. The definition of d_{jk} is expressed as followed [23]:

$$d_{jk} = \begin{cases} 1, k = 0 \\ \prod_{l=1}^{k} b_{jl}, \forall k \in \{1, 2, \cdots, M\} \end{cases} \quad (3.9)$$

where b_{jk} is the k^{th} information bit which is transmitted during the j^{th} $N_f T_f$ duration. Both b_{jk} and c_{ik} have a value of 1 or -1 in bipolar expression [23]. The general structure of DCSR IR-UWB transmitter is indicated in Figure 3.8.

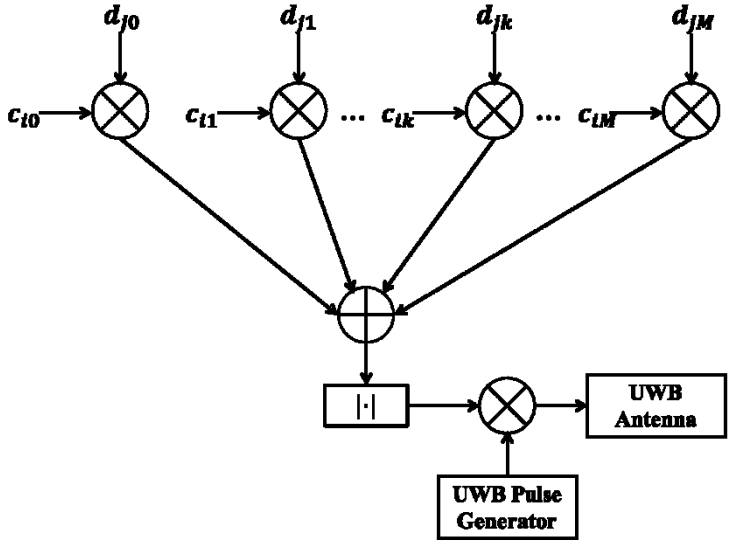


Figure 3.8 The general structure of DCSR IR-UWB transmitter [23]

In DCSR, the number of information bits M is limited by the number of frames N_f with the relationship $\frac{M(M+1)}{2} \leq 2^N - 1$ where $N_f = 2^N$ [23].

3.5.2 THE STRUCTURE OF DCSR RECEIVER

Based on its operation principle, the DCSR receiver has the same structure as the CSR receiver except the decoding part. If $M+1$ shifting codes are used at the transmitter, to extract the M received information bits, $\frac{M(M+1)}{2}$ orthogonal detection codes are needed. The general structure of DCSR IR-UWB receiver is shown in Figure 3.9:

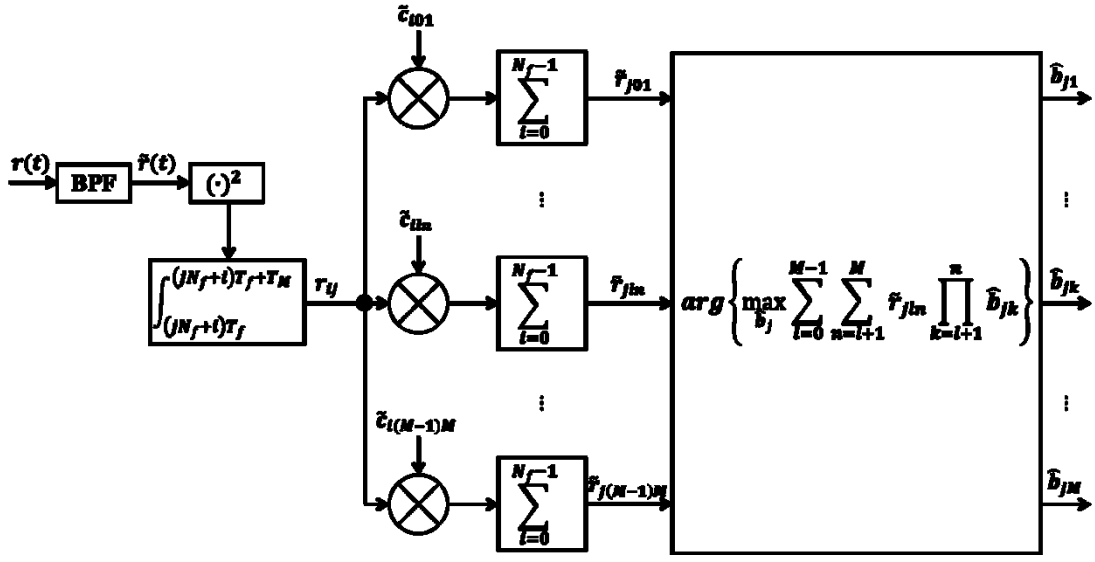


Figure 3.9 The general structure of DCSR IR-UWB receiver [23]

The detection codes of DCSR receiver $\tilde{c}_{iln} \in \{-1, 1\}$ are expressed in the following matrix [23]:

$$\begin{bmatrix} \tilde{\boldsymbol{c}}_{\boldsymbol{01}} \\ \vdots \\ \tilde{\boldsymbol{c}}_{\boldsymbol{0M}} \\ \tilde{\boldsymbol{c}}_{\boldsymbol{12}} \\ \vdots \\ \tilde{\boldsymbol{c}}_{\boldsymbol{1M}} \\ \tilde{\boldsymbol{c}}_{\boldsymbol{23}} \\ \vdots \\ \tilde{\boldsymbol{c}}_{(\boldsymbol{M-1})\boldsymbol{M}} \end{bmatrix} = \begin{bmatrix} \tilde{c}_{001} & \cdots & \tilde{c}_{i01} & \cdots & \tilde{c}_{(N_f-1)01} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{00M} & \cdots & \tilde{c}_{i0M} & \cdots & \tilde{c}_{(N_f-1)0M} \\ \tilde{c}_{012} & \cdots & \tilde{c}_{i12} & \cdots & \tilde{c}_{(N_f-1)12} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{01M} & \cdots & \tilde{c}_{i1M} & \cdots & \tilde{c}_{(N_f-1)1M} \\ \tilde{c}_{023} & \cdots & \tilde{c}_{i23} & \cdots & \tilde{c}_{(N_f-1)23} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \tilde{c}_{0(M-1)M} & \cdots & \tilde{c}_{i(M-1)M} & \cdots & \tilde{c}_{(N_f-1)(M-1)M} \end{bmatrix} \quad (3.10)$$

3.5.3 SELECTION OF THE SHIFTING AND DETECTION CODES IN DCSR SYSTEMS

Similar to CSR scheme, the selection of the shifting and detection codes for DCSR should follow the two rules below [23]:

$$\tilde{\boldsymbol{c}}_{\boldsymbol{ln}} = c_l c_n \quad (3.11)$$

$$\tilde{\boldsymbol{c}}_{\boldsymbol{ln}} \neq \tilde{c}_{pq}, except\ l = p\ and\ n = q \quad (3.12)$$

Table 3.2 gives an example of the shifting and detection codes for DCSR transceiver chosen from Walsh Codes:

Code Length	Shifting Codes	Detection Codes
$N_f = 2$	$\boldsymbol{c_0} = [1, \ 1]$ $\boldsymbol{c_1} = [1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{01}} = [1, -1]$
$N_f = 4$	$\boldsymbol{c_0} = [1, \ 1, \ 1, \ 1]$ $\boldsymbol{c_1} = [1, -1, \ 1, -1]$ $\boldsymbol{c_2} = [1, \ 1, -1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{01}} = [1, -1, \ 1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{02}} = [1, \ 1, -1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{12}} = [1, -1, -1, \ 1]$

Code Length	Shifting Codes	Detection Codes
$N_f = 8$	$\boldsymbol{c_0} = [1, \ 1, \ 1, \ 1, \ 1, \ 1, \ 1, \ 1]$ $\boldsymbol{c_1} = [1, -1, \ 1, -1, \ 1, -1, \ 1, -1]$ $\boldsymbol{c_2} = [1, \ 1, -1, -1, \ 1, \ 1, -1, -1]$ $\boldsymbol{c_3} = [1, \ 1, \ 1, \ 1, -1, -1, -1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{01}} = [1, -1, \ 1, -1, \ 1, -1, \ 1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{02}} = [1, \ 1, -1, -1, \ 1, \ 1, -1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{03}} = [1, \ 1, \ 1, \ 1, -1, -1, -1, -1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{12}} = [1, -1, -1, \ 1, \ 1, -1, -1, \ 1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{13}} = [1, -1, \ 1, -1, -1, \ 1, -1, \ 1]$ $\tilde{\boldsymbol{c}}_{\boldsymbol{23}} = [1, \ 1, -1, -1, -1, -1, \ 1, \ 1]$

Table 3.2 An example of the selected Walsh Codes for DCSR algorithm [23]

3.5.4 AN EXAMPLE OF THE ENCODING AND DECODING PROCESS OF DCSR

To better understand the DCSR, an example is taken in this subsection. Assuming that $N_f = 2^N = 4$ frames are transmitted simultaneously, where $N = 2$; therefore, at most $M = 2$ information bits (for instance, $b_1 = 0$ and $b_2 = 1$) can be transmitted within these frames. Referring to Table 3.2, the following shifting and detection codes are picked:

Code Length	Shifting Codes	Detection Codes
$N_f = 4$	$\boldsymbol{c_0} = [1, \ 1, \ 1, \ 1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{01}} = [1, -1, \ 1, -1]$
	$\boldsymbol{c_1} = [1, -1, \ 1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{02}} = [1, \ 1, -1, -1]$
	$\boldsymbol{c_2} = [1, \ 1, -1, -1]$	$\tilde{\boldsymbol{c}}_{\boldsymbol{12}} = [1, -1, -1, \ 1]$

Table 3.3 The shifting and detection codes for the encoding and decoding example

The encoding process at the transmitter side is as follows:

- $d_{j0} = 1 \ (= +1$ with bipolar expression)

  $d_{j1} = b_1 = 0 \ (= -1$ with bipolar expression)

  $d_{j2} = b_1 * b_2 = 0 \ (= -1$ with bipolar expression)

- $d_{j0} * \boldsymbol{c_0} = \quad 1 \quad 1 \quad 1 \quad 1$

  $d_{j1} * \boldsymbol{c_1} = \ -1 \quad 1 \ -1 \quad 1$

  $d_{j2} * \boldsymbol{c_2} = \ -1 \ -1 \quad 1 \quad 1$

- $|\sum| \quad = \quad 1 \quad 1 \quad 1 \quad 3$

Hence, the encoded pulse sequences transmitted out of the transmitter are 1 1 1 3; in the other words, analog pulses with 3-to-1 ratio between the high pulse and the low pulse are

transmitted in the order of low-low-low-high to carry the information bits "01". Table 3.4 lists all combinations of $b_1 b_2$ in the case of $M = 2$, where Amp is the order of pulse amplitude. It can be found that in this case, there are only two different amplitudes available for the pulses to pick up, 3 or 1.

$b_1 b_2$	$d_{j0} d_{j1} d_{j2}$	Amp	$b_1 b_2$	$d_{j0} d_{j1} d_{j2}$	Amp
00	101	1311	10	110	1131
01	100	1113	11	111	3111

Table 3.4 All combinations of information bits when $M = 2$ [25]

The decoding process at the receiver side is as follows:

- $\boldsymbol{r_{ij}} = (1\ 1\ 1\ 3)^2 = 1\ 1\ 1\ 9$
- $\boldsymbol{r_{ij}} * \tilde{\boldsymbol{c}}_{\boldsymbol{01}} = \quad 1\ -1\quad 1\ -9\ \rightarrow\ r_{01} = -8$

  $\boldsymbol{r_{ij}} * \tilde{\boldsymbol{c}}_{\boldsymbol{02}} = \quad 1\quad 1\ -1\ -9\ \rightarrow\ r_{02} = -8$

  $\boldsymbol{r_{ij}} * \tilde{\boldsymbol{c}}_{\boldsymbol{12}} = \quad 1\ -1\ -1\quad 9\ \rightarrow\ r_{12} = +8$

- $\hat{\boldsymbol{b}}_{\boldsymbol{j}} = r_{01} * \hat{b}_1 + r_{02} * \hat{b}_1 * \hat{b}_2 + r_{12} * \hat{b}_2 \ \rightarrow\ \hat{b}_1 = -1\ (= 0 \text{ with } \{0, 1\} \text{ expression})$

  $\hat{b}_2 = +1\ (= 1 \text{ with } \{0, 1\} \text{ expression})$

Hence, the information bits “01” are extracted.

3.6 PERFORMANCE COMPARISONS

To verify the performance improvement provided by DCSR, computer-based simulations aimed at bit-error-rate (BER) versus signal-to-noise ratio (SNR) of four IR-UWB systems mentioned above have been carried out in [24]. Figure 3.10 and Figure 3.11 illustrate the comparison results of BER performance between TR, FSR, CSR and DCSR systems with different M and related minimum N_f.

Obviously, DCSR system can achieve the significant better BER performance under both indoor and outdoor conditions. One of the reasons is that the DCSR algorithm can provide the close-to-highest bit-to-pulse ratio $\left(\frac{M}{N_f}\right)$ which is positively related to BER compared with other three algorithms; another reason is that the power consumption of the reference pulse sequence is merely $\frac{1}{M+1}$ of the total power in DCSR transmitter, while other transmitters need $\frac{1}{2}$ of their total power to transmit the reference pulse sequence [24]. A comparison of the main aspects between four transceivers is provided in Table 3.5, where PAPR is peak-to-average power ratio.

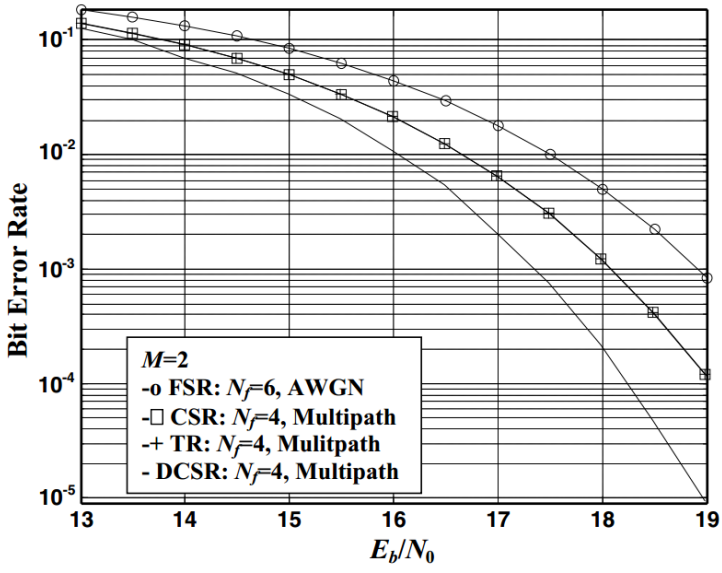


Figure 3.10 BER performance comparisons when $M = 2$ *[24]*

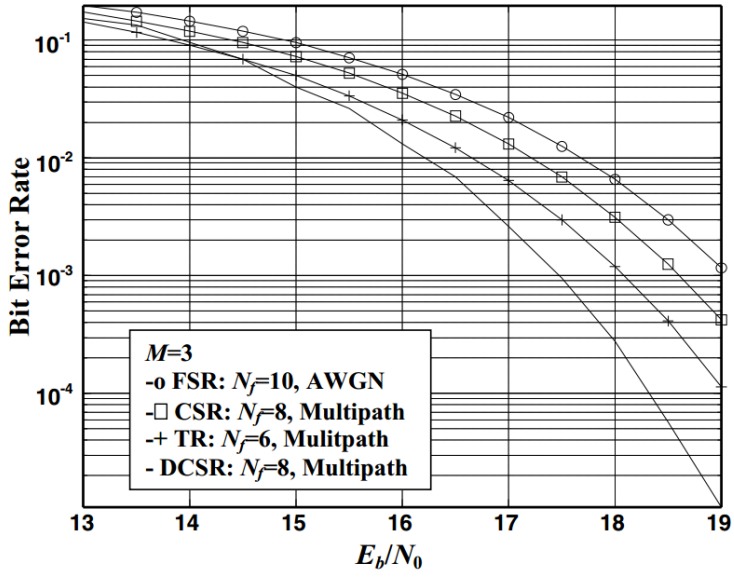


Figure 3.11 BER performance comparisons when $M = 3$ *[24]*

	TR	FSR	CSR	DCSR
Delay element	Yes	No	No	No
Analog carriers	No	Yes	No	No
Reference power	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{M+1}$
$\frac{M}{N_f}$	$\frac{1}{2}$	$< \frac{1}{2}$	Up to $\frac{1}{2}$	Up to $\frac{1}{2}$
Multipath errors	No	Yes	No	No
PAPR	Low	High	Medium	Medium
Performance	Good	Poor	Good	Best
Complexity	High	High	Low	Low

Table 3.5 Comparison of main aspects between four transceivers [24]

CHAPTER 4 CURRENT DCSR SYSTEM

This chapter briefly introduces the structure and implementation of the current DCSR IR-UWB transceiver system which have been designed by previous members of the RF/Microwave research group. Afterwards, the existing gain control scheme in DCSR receiver as well as its limitation is discussed. More detailed information can be found in [7] [25] [26] [27].

4.1 TRANSMITTER STRUCTURE

In general, the DCSR IR-UWB transmitter consists of three main stages: pulse generation, amplitude modulation and pulse gating. To generate the high and low pulses mentioned in the last chapter, two independent sequences with the same amplitude are generated and then combined to form the desired sequence which is finally gated with radio frequency (RF) to produce the transmittable RF-modulated Gaussian pulses of short duration. The block diagram of the DCSR transmitter is illustrated in Figure 4.1.

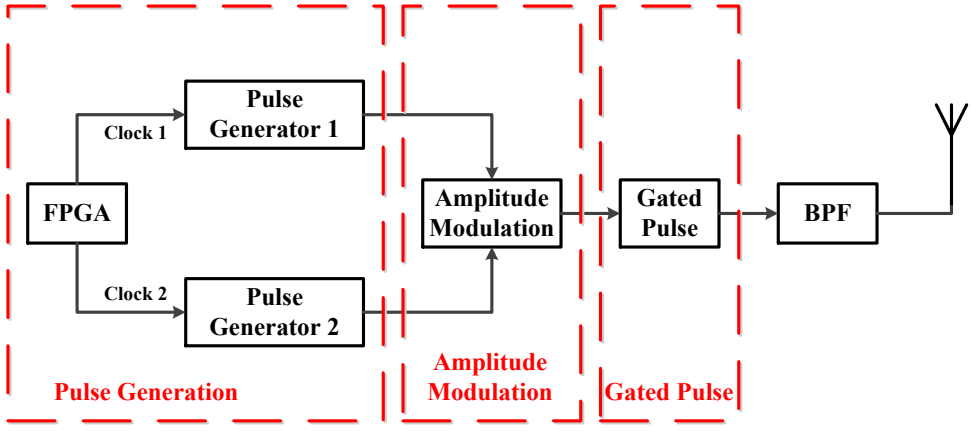
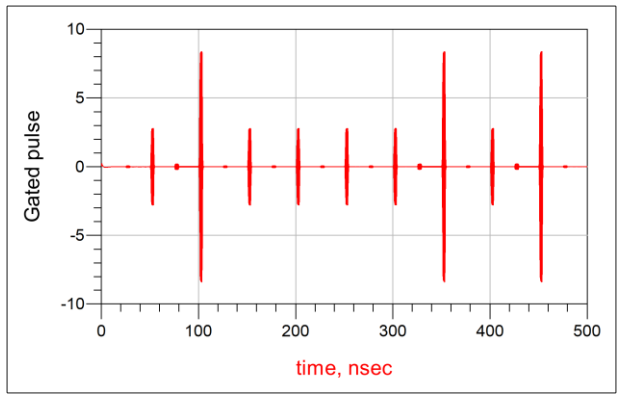


Figure 4.1 DCSR transmitter block [7]

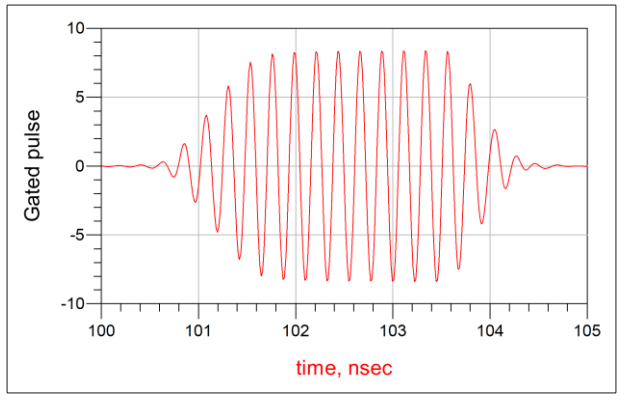
The first stage, pulse generation, is composed of a field-programmable gate array (FPGA) board and two identical pulse generator branches. Two 20MHz clocks, Clock 1 and Clock 2, are programmed in FPGA by the means of on-off keying (OOK); that is, when a high pulse is coming Clock 1 generates a trigger signal to Pulse Generator 1 meanwhile Clock 2 is shut down; otherwise when a low pulse is coming Clock 2 generates a trigger signal to Pulse Generator 2 and Clock 1 is shut down. After triggered by Clock 1 or 2, the pulse generators produce an ultra-narrow pulse which has duration of 4 ns. At this step, all pulses have uniform amplitude.

At the amplitude modulation stage, the amplitudes of the independent pulse sequences in the time domain are modulated based on DCSR coding requirements and then combined into one pulse sequence. The pulse sequence coming from Pulse Generator 1 is amplified to a high voltage corresponding to 3, while the pulse sequence coming from Pulse Generator 2 is amplified to a low voltage corresponding to 1; the ratio between them is 3.

At last, in the gated pulse stage, the combined pulse sequence is gated with a 4.44GHz sinusoidal signal. This process can also be considered as an on-off switching with an RF modulation signal. When a pulse arrives at the stage, the switch is on to allow the pulses to be modulated or mixed with the 4.44GHz signal; conversely, if no pulse shows up, the switch turns off. After being gated, the encoded pulse sequence is filtered by a band-pass filter (BPF) and then sent to UWB antennas. Figure 4.2 shows the simulation results of the transmitted pulse sequence.



(a)



(b)

Figure 4.2 Simulation results of the (a) transmitted pulse sequence and (b) pulse shape [7]

4.2 RECEIVER STRUCTURE

As shown in Figure 4.3, the general DCSR IR-UWB receiver has four stages: signal recovery, high frequency removal, energy detection and code synchronization.

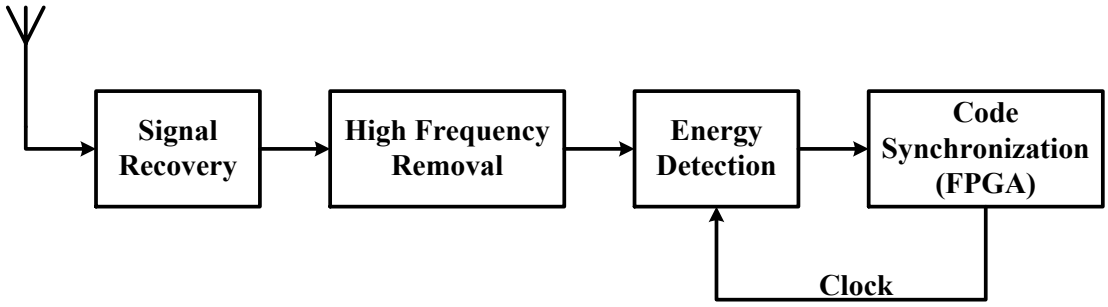


Figure 4.3 DCSR receiver block [7] [26] [27]

After received by UWB antenna, the signal is processed firstly within the signal recovery stage which is made up of a band-pass filter (BPF), a variable attenuator and a low noise amplifier (LNA), as illustrated in Figure 4.4. The main purpose of this stage is to filter the noise and interference, to eliminate the distortion of the received signal and to adjust the signal for further detection. The detailed description for this stage will be provided later since its gain control is the main interest of this research project.

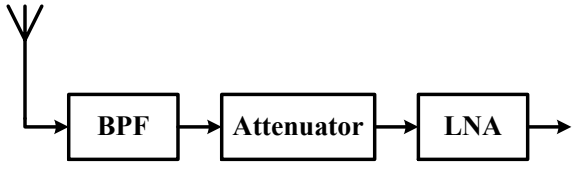


Figure 4.4 Signal recovery stage [7]

The next stage, the high frequency removal stage down-converts the 4.44GHz-modulated pulses to the baseband. It is accomplished by the means of "squaring: multiply the signal by itself through a power splitter and a mixer, and then filter out the high frequency components through a low-pass filter. The structure of high frequency removal stage is shown in Figure 4.5.

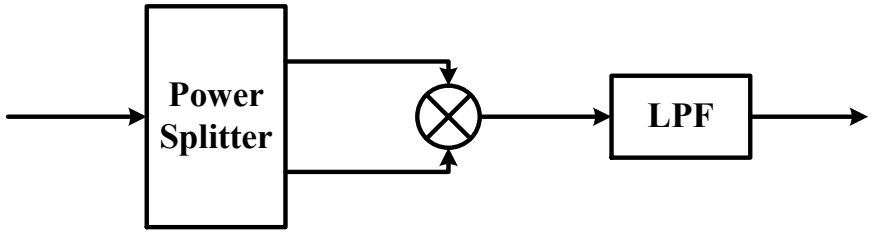


Figure 4.5 High frequency removal stage [7]

The following stage, energy detection, is composed of a DC voltage buffer, an active-LPF, an analog-to-digital converter (ADC) and a phase-locked loop (PLL) that cooperates with FPGA. To achieve energy detection, the active-LPF is used to expand the ultra-narrow pulse so that the ADC can oversample it by 4 times of the data-rate. The oversampling ensures that the received clock, which is regenerated in the FPGA at the receiver, can be synchronized with the clock operating at the transmitter side by using the PLL feedback loop. The sampled digital data is left to the next stage for extracting the data bits. Figure 4.6 shows the architecture briefly.

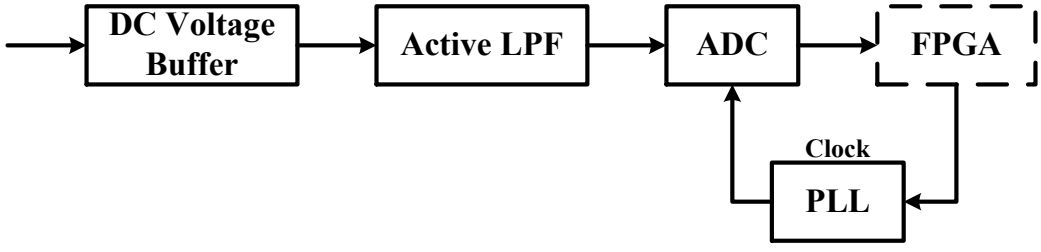


Figure 4.6 Energy detection [26] [27]

Code synchronization has to be applied at the end to perform correct bit extraction. In all, the clock synchronization, symbol synchronization and bit detection based on DCSR algorithm are implemented in FPGA using VHDL codes.

4.3 EXISTING GAIN CONTROL IN DCSR RECEIVER

4.3.1 DESIGN CONCEPT

As mentioned above, the existing gain control (or the signal strength adjustment) is implemented in the signal recovery stage which is cascaded with a band-pass filter, an attenuator and a low noise amplifier.

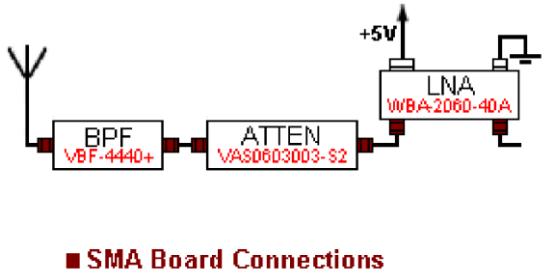


Figure 4.7 The schematic of the existing signal recovery [7]

Figure 4.7 shows the schematic of existing signal recovery. With the BPF, all noises and interferences outside the desired frequency band can be removed. Manual variable attenuator is used to adjust the received signal strength before it goes to the low-noise amplifier. If the received signal strength is too high, it may saturate the amplifier and result in loss the amplitude ratios among the received data pulses; then attenuator is manually adjusted to have more attenuation of the signals. If the signal received is too weak, attenuator is manually adjusted to less attenuation of the signals. The expectation is that the signal after the amplifier (or the signal recovery stage in general) maintain the exact amplitude ratio among the pulses before the amplifier (or the signal recovery stage in general), as shown in Figure 4.8 [7].

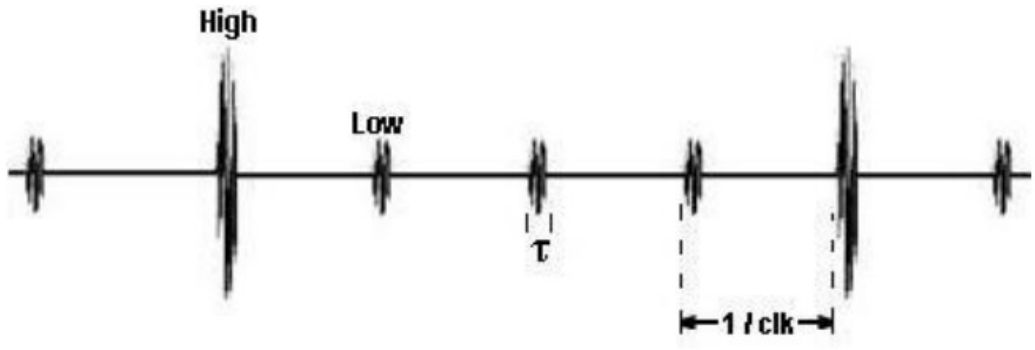


Figure 4.8 The output result of signal recovery [7]

4.3.2 TEST RESULT AND LIMITATIONS OF THE EXISTING SIGNAL RECOVERY STAGE

Hardware implementation of the signal recovery is shown in Figure 4.9. Tests were taken under the condition of a direct connection between the DCSR transmitter and receiver using Sub-Miniature-A (SMA) cable. Agilent Infiniium DSO81204B oscilloscope was used for the measurements.

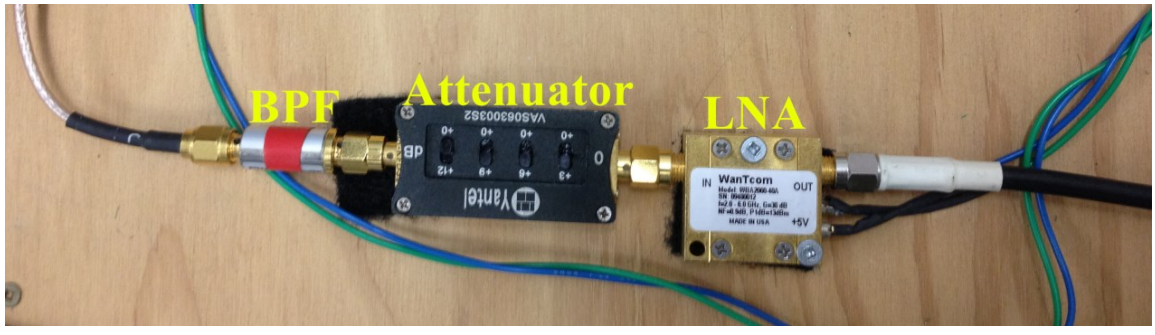
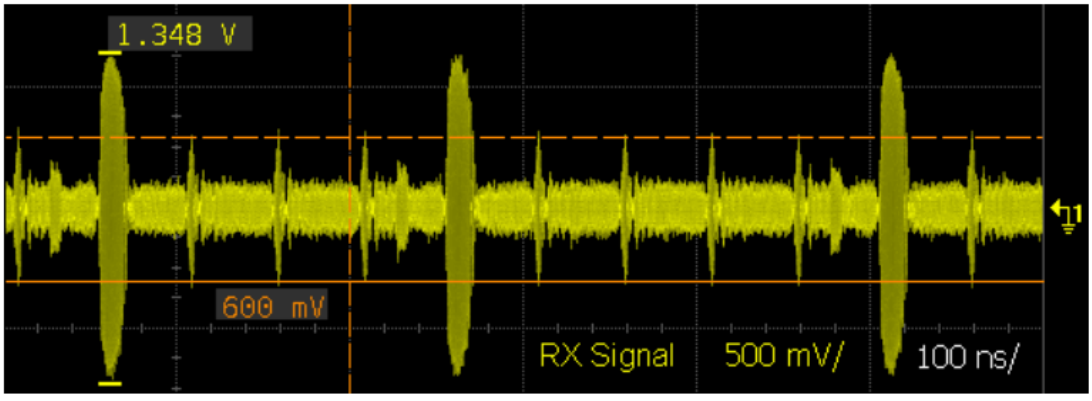


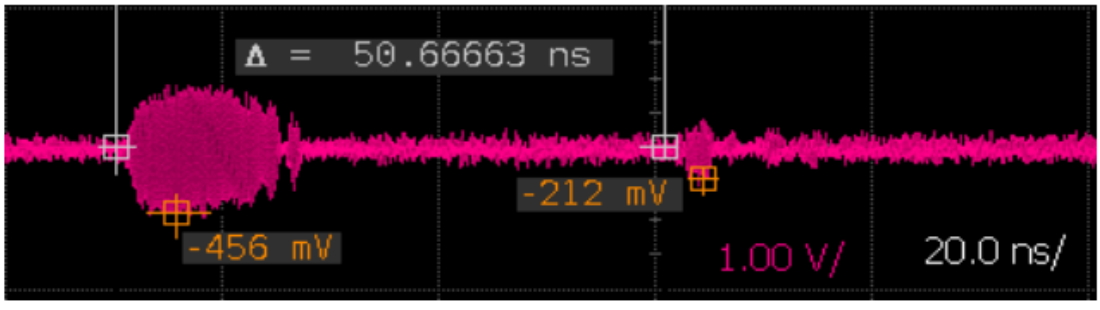
Figure 4.9 The implementation of the existing signal recovery

Figure 4.10 compares the test results between the output signal of the signal recovery in receiver and the output signal of gated pulse in transmitter. It can be seen that the

amplitude ratio between high and low pulses of the recovered signal is approximately 2:1 instead of desired 3:1. Noises appear large in the output of signal recovery. More importantly, the signal recovery block cannot perform signal strength adjustment itself or automatically. Manual variable attenuator was used which do not work in a real wireless environment where signal strengths may vary randomly. Therefore, new automatic signal strength adjusting method, or automatic gain control, should be developed.



(a)



(b)

Figure 4.10 The test results of the (a) recovered signal and (b) transmitted signal [7]

CHAPTER 5 DCSR IR-UWB SIGNAL STRENGTH ADJUSTMENT: PROPOSED APPROACHES

The existing design to perform signal strength adjustment in DCSR system and its problems has been discussed in the previous chapter. In this chapter, two new approaches to address the problems are introduced with the second approach being recommended as the final solution.

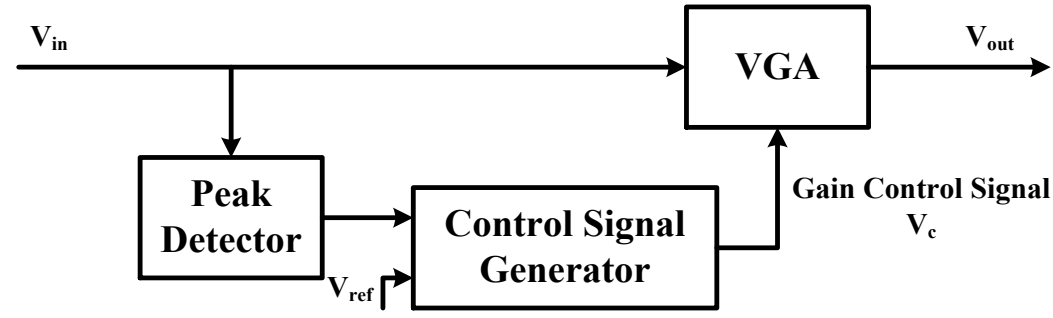
5.1 AUTOMATIC GAIN CONTROL

As discussed in the previous chapter, the main problem of the existing signal strength adjustment used in the signal recovery stage of the DCSR receiver is its incapability of self or automatic adjusting in a realistic time-variant wireless environment.

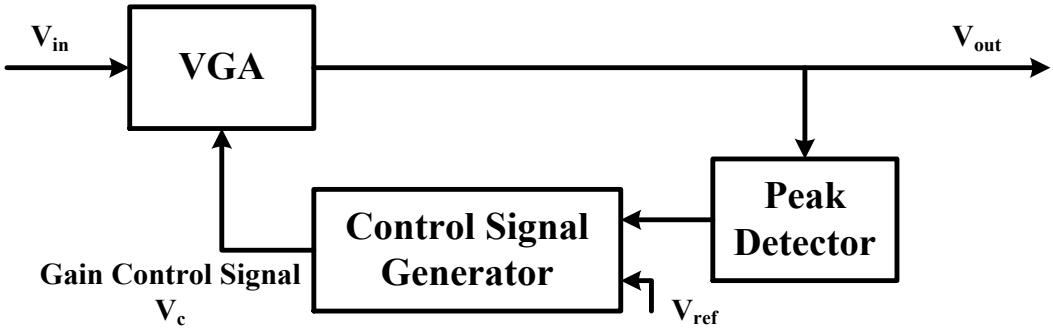
In general, signals going through a wireless channel experience many forms of distortions and interferences that include changes of waveforms and signal strengths. They bring potential problems to the DCSR receiver: missing weak signal or mistaking strong signal. As a result, for operating reliably and stably wireless receivers are required to accommodate certain dynamic ranges of the received signal strength [28]. To achieve a wide dynamic range in a low complex receiver, automatic gain control (AGC) is used to automatically adjust the signal strength before it is sent to a low-noise amplifier.

As its name suggests, the general function of AGC is to adjust the gain for the received signals of different signal strengths so that they settle to the desired level which is suitable for the rest components of the receiver, in particular the low-noise amplifier. In

the other words, if the received signal is too weak, AGC will amplify it; conversely, if the received signal is too strong, AGC will attenuate it. Since the output signal of AGC is relatively constant, all the following blocks such as amplifiers and/or mixers are not severely obliged to be designed with wide dynamic ranges; hence, the complexity of the receiver can be reduced [28].



(a)



(b)

Figure 5.1 The block diagram of (a) feed-forward and (b) feedback AGCs [29]

As shown in Figure 5.1, a basic AGC block can be designed in two different types: feed-forward control and feedback control. However, no matter which architecture is used, a general AGC is always composed of the following three components [29]:

a. Peak Detector: the PD is used to collect the strength information of the signal. For feedback control, the strength information is detected from the output signal of AGC, V_{out}; for feed-forward control, the strength information is detected from the input signal of AGC, V_{in}.

b. Control Signal Generator (CSG): after PD, the CSG compares the obtained strength information with a reference voltage, V_{ref}, finds the difference between two voltages and then generate a voltage control signal V_c, which is appropriate for VGA in the next step.

c. Variable Gain Amplifier (VGA): for performing automatically adjustment, the VGA amplifies or attenuates V_{in} by the control of V_c and produces V_{out}.

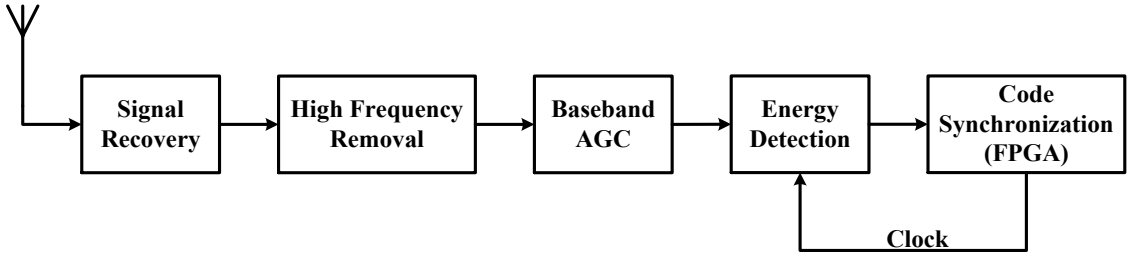
The advantages and disadvantages of the two approaches elaborated as follows. For the feed-forward AGC, since the control signal is produced directly from the input, there will be no more instabilities and settling time; on the other hand, PD needs to have a wide dynamic range since it takes the signal directly from the AGC input. Therefore, PD needs to of high linearity, which may pose a design challenge. For the feedback AGC, since the control signal is extracted from the output, PD is not required to have a wide dynamic range. Therefore, implementation can be relatively simple and high linearity can be relatively easily achieved. However, with the desired high compression or expansion ratio, the feedback AGC may suffer unwanted instabilities, and longer settling time [29].

It is noted that although AGC adjust the gain for a received signal based on the signal strength, the output signal of AGC will not lose any data information. The reason is that the amplitude variation has much lower variation rates than the data rates. Therefore, an effective AGC can eliminate the impact of variations of the channel conditions while keeping the recovered signal similar to the transmitted signal.

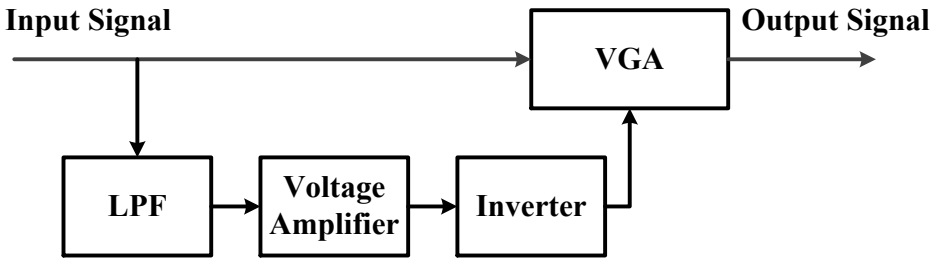
5.2 THE FIRST DESIGN: FEED-FORWARD AGC AT BASEBAND

5.2.1 DESIGN CONSIDERATIONS

In this work, an analog feed-forward AGC structure was firstly selected. Due to the high transmitting frequency which is 4.44GHz, difficulties arose in finding an appropriate RF variable gain amplifier that operates at 4.44GHz. As a result, our feed-forward AGC was implemented at baseband. Hence, the first proposed AGC, composed of a VGA, a low-pass filter (LPF), a voltage amplifier and an inverter, was designed to work at baseband, following the high frequency removal stage mentioned in Chapter 4. The block diagram of the design is shown in Figure 5.2.



(a)



(b)

Figure 5.2 The block diagram of the proposed (a) receiver and (b) feed-forward AGC

As the output of the high frequency removal stage, the input signal towards AGC is divided into two directions: one goes through the VGA branch directly and then goes to the following energy detection stage (can be considered as the main branch); the other goes through the control signal generation.

5.2.1.1 SIGNAL ADJUSTMENT

To adjust the signal strength, variable gain amplifier was introduced. The model of VGA for this design is VCA824. It is a wideband (710MHz) and continuous voltage-controlled gain amplifier from Texas Instrument [30], as shown in Figure 5.3. The VGA is powered by ±5V DC supply, with 40dB variable gain range dominated by control voltage up to ±1V.

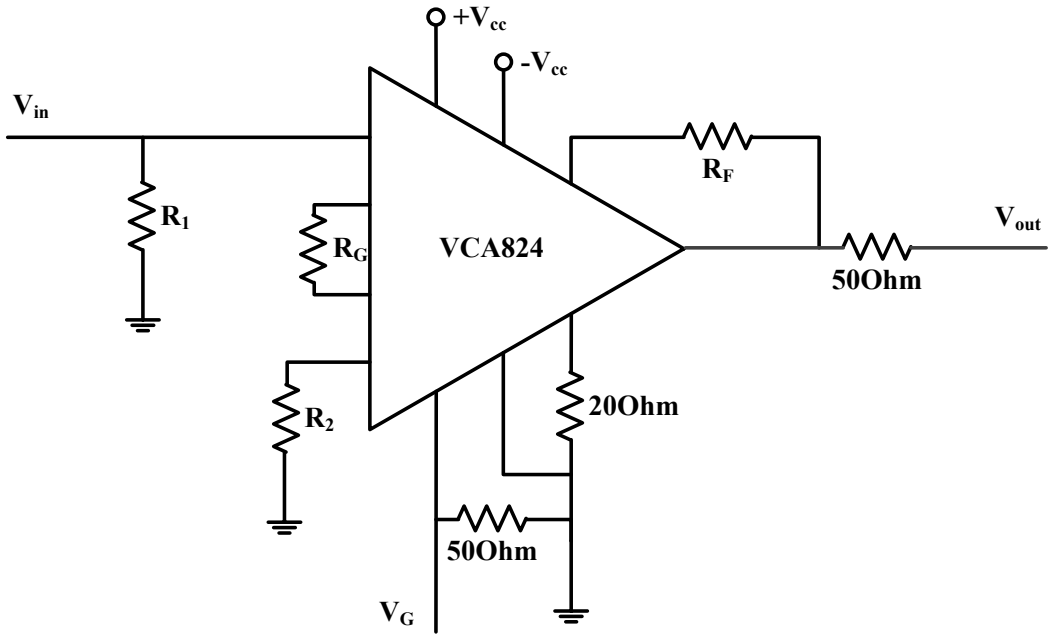


Figure 5.3 VGA in test circuit configuration [30]

The variable gain of VGA is determined by the followed equation:

$$G = 2 \times \frac{R_F}{R_G} \times \frac{V_G+1}{2} \qquad (5.1)$$

For this design, the maximum gain of +3.6V/V is chosen as a result of taking into account the maximum input voltage range of subsequent circuits. Hence, the values of resistors are:

$$R_1 = R_2 = 50\Omega,$$

$$R_G = 200\Omega,$$

$$R_F = 360\Omega.$$

Figure 5.4 shows the relationship between the gain and the gain control voltage.

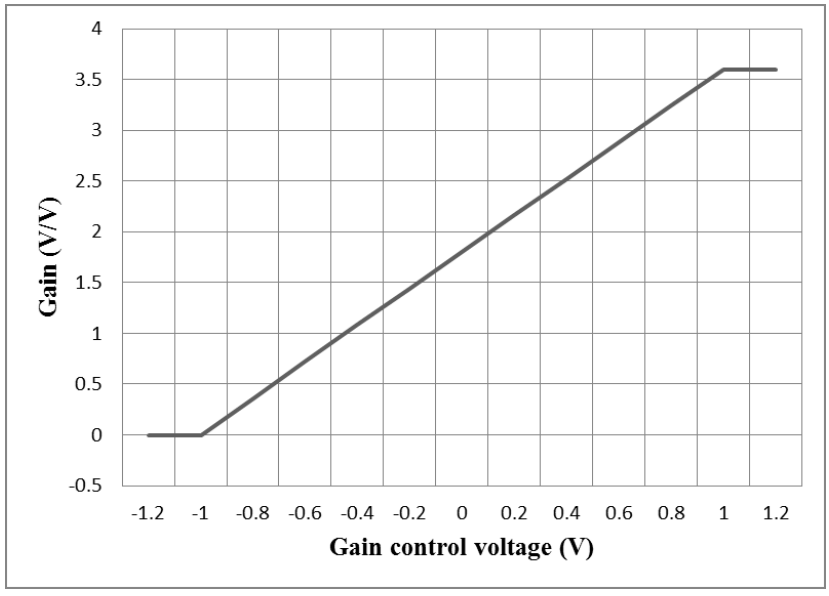


Figure 5.4 Gain vs gain control voltage

5.2.1.2 CONTROL SIGNAL GENERATION

The control signal generation branch, as shown in Figure 5.2, has three stages. They are to generate an appropriate control signal for VGA to adjust the strength of the received signal in the main branch. As mentioned above, AGC should adjust the signal strength without losing any data information. In the case of DCSR, a desired AGC under normal operation should produce a stable output signal that still retains high-to-low pulse ratio. Therefore, control signal should contain signal strengths that are of low frequency in nature. The process is elaborated below.

After high frequency components have been removed, the input signal that is sent to the control signal generation branch supposedly contains only data information (high pulses and low pulses). Since the data rates have a much higher frequency than the amplitude

variations that represent channel variation conditions, it is reasonable to use LPF as an average amplitude detector to filter out the rapid-changing data information (can be considered as high frequency component) and obtain the slow-changing amplitudes(can be considered as low frequency component). The rectifier/filter circuit, as shown in Figure 5.5, can be implemented to carry out the function without much difficulty. . The design starts with a series diode, which acts as a rectifier or a clipper, following by an inductor in series and a capacitor in parallel whose combination may act as a low-pass filter to smooth the ripple and filter out the high frequency components. The process of the signal going through the proposed LPF is illustrated in Figure 5.6.

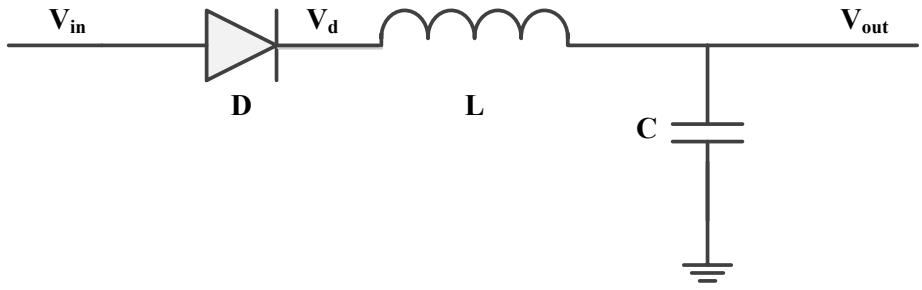


Figure 5.5 The schematic of low-pass filter in the proposed feed-forward AGC

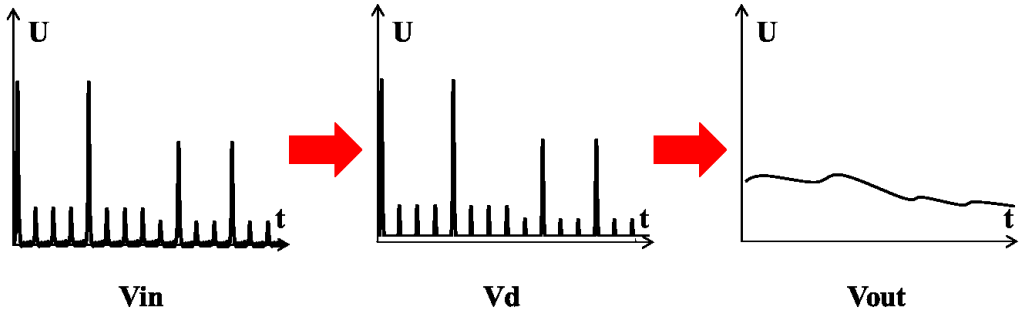


Figure 5.6 The filtering process through the proposed LPF

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{5.2}$$

$$\tau = \sqrt{LC} \tag{5.3}$$

Based on Equation (5.1) and Equation (5.2), optimal values of the inductor L and the capacitor C are picked as a trade-off between a lower cut-off frequency and a smaller delay:

$$L = 270\mu H,$$

$$C = 1\mu F.$$

Unfortunately, the control voltage obtained as described above cannot be directly applied to VGA yet. When the strength of received signal is strong, the output voltage of LPF would have a higher value; conversely, when the strength of received signal is weak, the output voltage of LPF would have a smaller value. However, For a VGA, as shown in Figure 5.4, a low control voltage brings about a low gain, while a high control voltage brings about a high gain. Consequently, the output signal of LPF is required to be inverted. A voltage amplifier and an inverter are introduced as a solution, as shown in Figure 5.7.

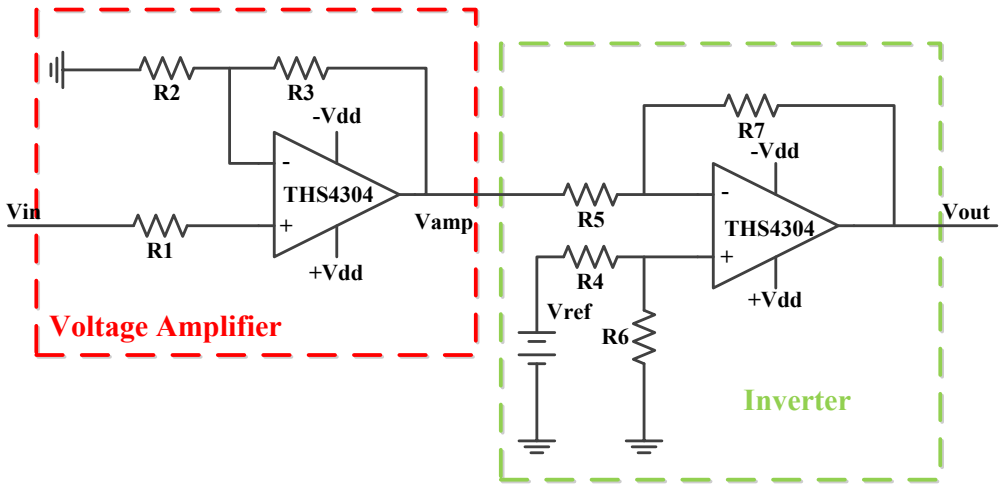


Figure 5.7 The schematic of voltage amplifier and inverter

The input of the voltage amplifier is the output of LPF, and the output of inverter is the control signal sent to VGA. Those voltages have the following relationship:

$$\begin{cases} V_{amp} = AV_{in} \\ A = \frac{R_3}{R_2},\ R_1 = R_2 \end{cases} \tag{5.4}$$

$$V_{out} = \frac{R_6}{R_4}V_{ref} - \frac{R_7}{R_5}V_{in} = V_{ref} - V_{in},\ R_4 = R_5 = R_6 = R_7 \tag{5.5}$$

Based on Equation (5.4) and Equation (5.5), the values of resistors are picked as:

$$R_1 = R_2 = 500\Omega,$$

$$R_3 = 14.7k\Omega,$$

$$R_4 = R_5 = R_6 = R_7 = 1k\Omega.$$

Figure 5.8 shows the process of the signal going through the voltage amplifier and inverter. Figure 5.9 shows how the feed-forward AGC adjusts the received signal strength automatically. It should be noted that signals showed in Figure 5.6, Figure 5.8 and Figure 5.9 are merely for demonstration process; the actual amplitude distortion is more gently and smooth.

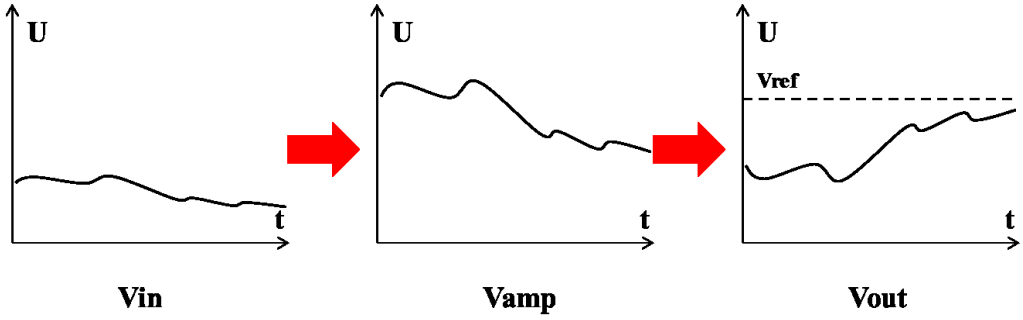


Figure 5.8 The amplifying and inverting process

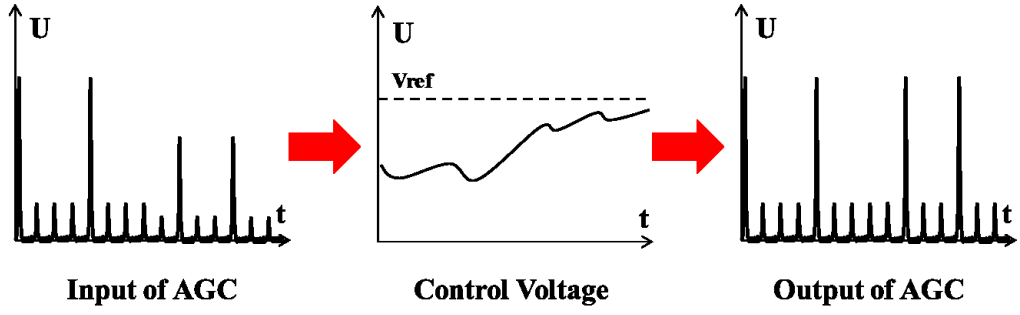


Figure 5.9 The automatic adjusting process using the proposed feed-forward AGC

5.2.2 SIMULATION RESULTS

The simulation of the proposed feed-forward AGC was executed in Advanced Design System 2011 (ADS 2011) manufactured by Agilent to check the validity of the design before implementation. The existing DCSR transmitter and receiver introduced in Chapter 4 were modeled and simulated using ADS to obtain input signals. The original DCSR signal with no amplitude distortion (see Figure 5.10) was first amplitude modulated with a 1kHz sinusoidal signal that emulated the channel variation and then sent to the designed AGC. Figure 5.11 shows the simulated AGC block.

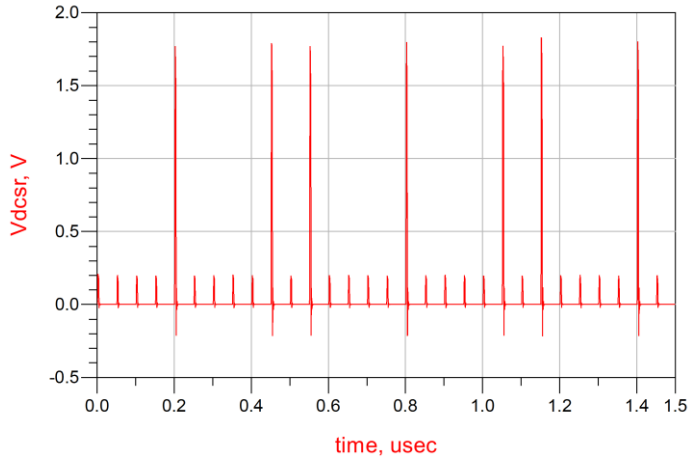


Figure 5.10 The simulated DCSR signal

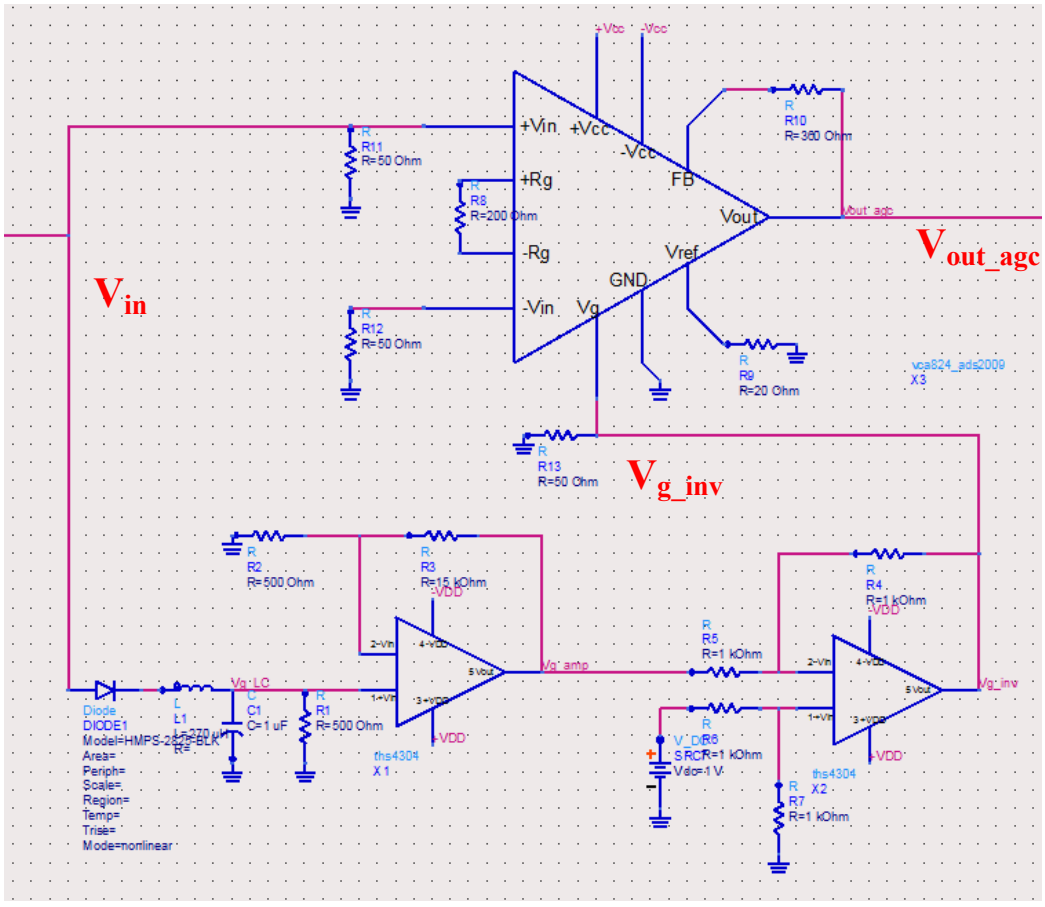


Figure 5.11 The schematic of the proposed feed-forward AGC in simulation

Figure 5.12 shows the simulation results of the proposed feed-forward AGC ((b) is an expanded version of (a), which shows the expanded pulse shape). The input signal, V_{in}, is the distorted DCSR signal after removing the high frequency carrier. The voltage control signal, V_{g_inv}, is generated through the control signal generation branch and sent to VGA. The output signal, V_{out_agc}, is the adjusted result of VGA that goes towards the energy detection stage. Referring to Figure 5.9, it can be see that the automatic signal adjustment has been achieved with the proposed design, since the low amplitude variations have been removed without losing any transmitted data information.

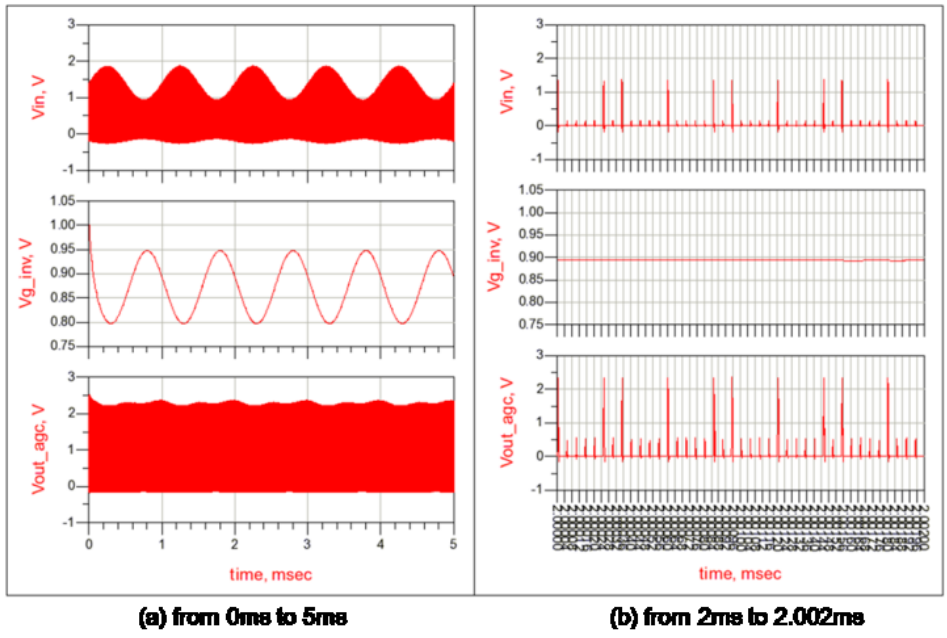


Figure 5.12 Simulation results of the proposed feed-forward AGC

5.2.3 IMPLEMENTATION AND TEST RESULTS

The proposed feed-forward AGC was fabricated on a FR4 double-sided copper-clad printed circuit board (PCB) using grounded coplanar waveguide (GCPW) owing to its outstanding transmission performance at RF and microwave frequencies. All components used were made of surface mount technology (SMT) to improve assembly density and minimize high-frequency interference. The proposed AGC was prototyped with EAGLE PCB Design Software manufactured by CadSoft. Figure 5.13 illustrates the top layer of PCB layout of the proposed feed-forward AGC in reference to the schematic shown in Figure 5.11, while Figure 5.14 shows the prototype. The waveforms were measured and captured by Agilent 54831D 4+16-Channel, 600 MHz Mixed-Signal Infiniium Oscilloscope.

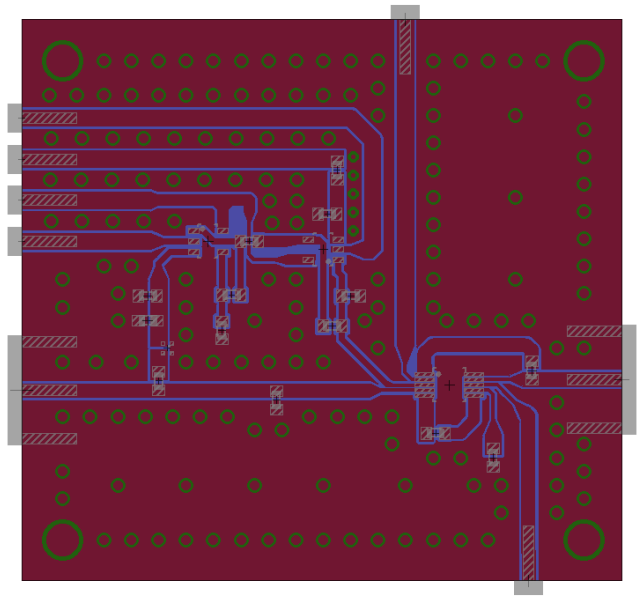


Figure 5.13 PCB layout of the proposed feed-forward AGC (top layer)

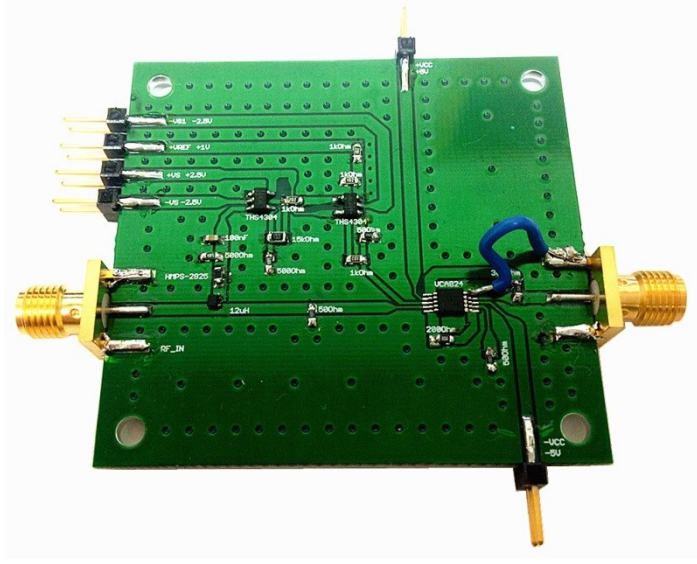


Figure 5.14 Photo of the proposed feed-forward AGC

To test the effective the dynamic range of the proposed feed-forward AGC quantitatively, signal generator 33250A, which is an 80MHz function/arbitrary waveform generator

manufactured by Agilent, was input to the AGC directly. In the real DCSR system, the high pulse of 4ns appears in each 200ns. Therefore, to approximate real DCSR signal the input was set up as a 5MHz pulse sequence with 5ns pulse duration (4ns was unavailable due to the limitation of the generator). The test results are shown in Figure 5.15. The yellow signal is the input generated by signal generator with different signal strength, while the green signal is the output of AGC. Clearly, the proposed AGC is able to adjust the input signal in a certain range. More tests verify that the proposed baseband AGC works well with a stable 820mV output when the envelope of the input signal is between 447mV and 1.256V.

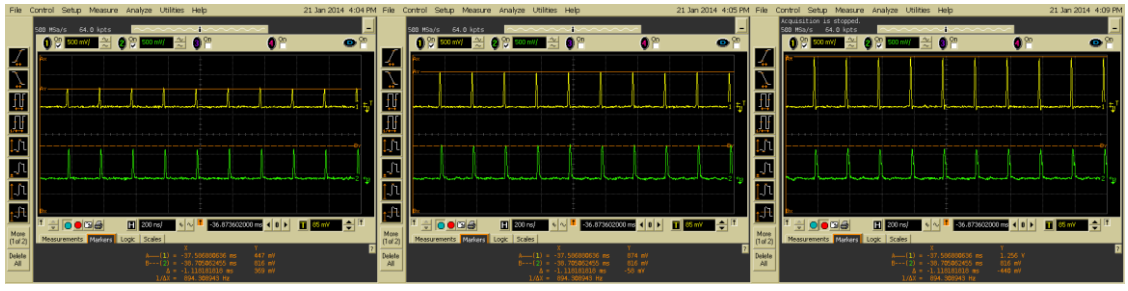
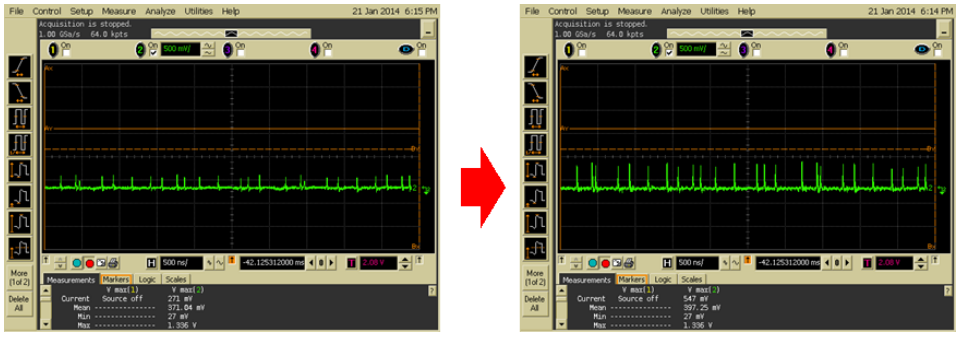


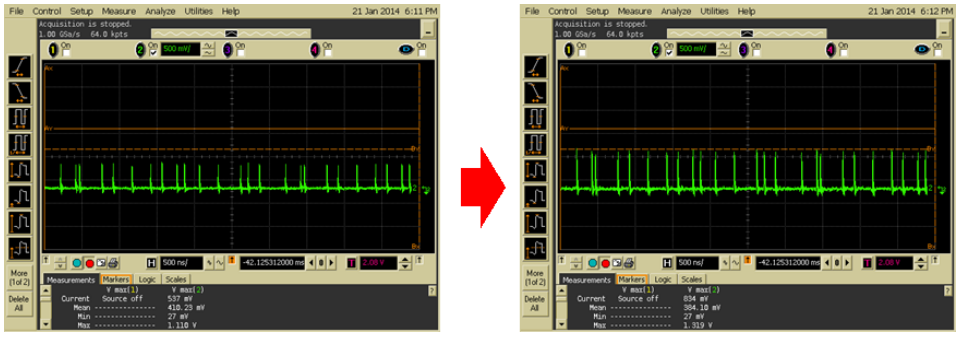
Figure 5.15 Measured input range of the proposed feed-forward AGC

Test of the proposed baseband AGC board incorporated in in the entire DCSR system was made with a wireless connection between the transmitter and the receiver using UWB antennas. Figure 5.16 is the results of the proposed feed-forward AGC. The left column is the input signal of AGC while the right column is the corresponding output signal of AGC. It can be seen that when the high pulses of input signal (can be considered as the envelope of the signal) have an amplitude of 271mV, the envelope of output signal is 547mV. When the envelope of the input signal is between 537mV and 728mV, the envelope of the output signal may be stabilized around 830mV. When the

envelope of the input signal reaches 841mV, severe change of the ratio between high pulses and low pulses is observed since the signal has already exceeded the saturation point of the previous circuits in receiver; although the envelope of output signal has been stabilized at 846mV, this ratio change is there.

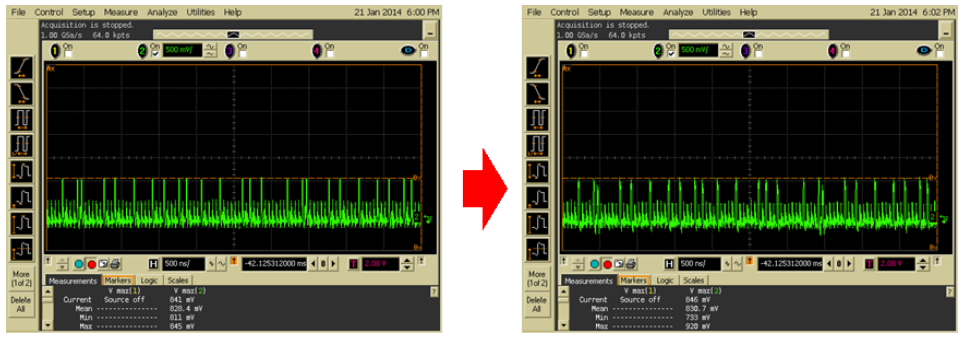


(a)



(b)

(c)



(d)

Figure 5.16 Implementation results with and without the proposed feed-forward AGC while the high pulses of input signal have envelope amplitude of (a) 271mV, (b) 537mV, (c) 728mV and (d) 841mV

In summary, if the envelope of the input signal ranges from 447mV to 1.256V, the envelope of output signal of the proposed baseband AGC can be stabilized around 820mV to 830mV; if the input envelope is smaller than 400mV, the output envelope will reduce rapidly since the AGC cannot provide enough amplification; if the input envelope is higher than 1.3V, the output envelope will also reduce rapidly since the AGC starts to malfunction. The effective input voltage range is only from 271 mV to 728mV where the ratio of high to low pulses in magnitude is kept. One of the main inadequacies of the first design is that it is done at the baseband while in reality ACG should be provided at the front end of the receiver so that both weak and strong signals received by the UWB antennas can be adjusted for all the component stages after the antenna, especially the low noise amplifier. Thereupon, a second design was carried out.

5.3 THE SECOND DESIGN: FEEDBACK AGC AT RF

5.3.1 DESIGN CONSIDERATIONS

As mentioned in the previous section, although the feed-forward ADG may work well, it is difficult to obtain proper commercial products at 4.44GHz to implement them. As a result, the feedback control method for AGC becomes the sole feasible choice in this design. The side benefit is that the digital control signal can be generated by the FPGA that has already existed in the DCSR receiver, which will further reduce the cost of implementation. The block diagram of the feedback AGC design is shown in Figure 5.17.

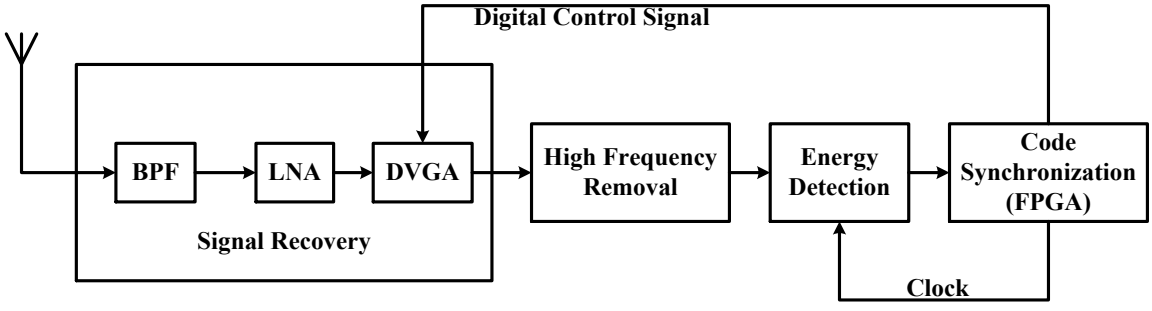


Figure 5.17 The block diagram of DCSR receiver with the proposed feedback AGC

5.3.1.1 DIGITAL VARIABLE GAIN AMPLIFIER/ATTENUATOR (DVGA)

The selected DVGA is HMC625LP5E, a 0.5dB LSB 6-bit digital variable gain amplifier from Hittite Microwave Corporation [31], as shown in Figure 5.18. It is powered by a single +5V DC supply, with 31.5dB variable gain range controlled by 6-bit digital signal

in 0.5dB steps. The 6 parallel bit signal come directly from FPGA. The gain variation principle abides by the following table in reference to Figure 5.18.

Relative AMP/ATT (dB)	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1
-0.5	1	1	1	1	1	0
⋮						
-8	1	0	1	1	1	1
-8.5	1	0	1	1	1	0
⋮						
-31	0	0	0	0	0	1
-31.5	0	0	0	0	0	0

Table 5.1 Relative gain variation principle of DVGA

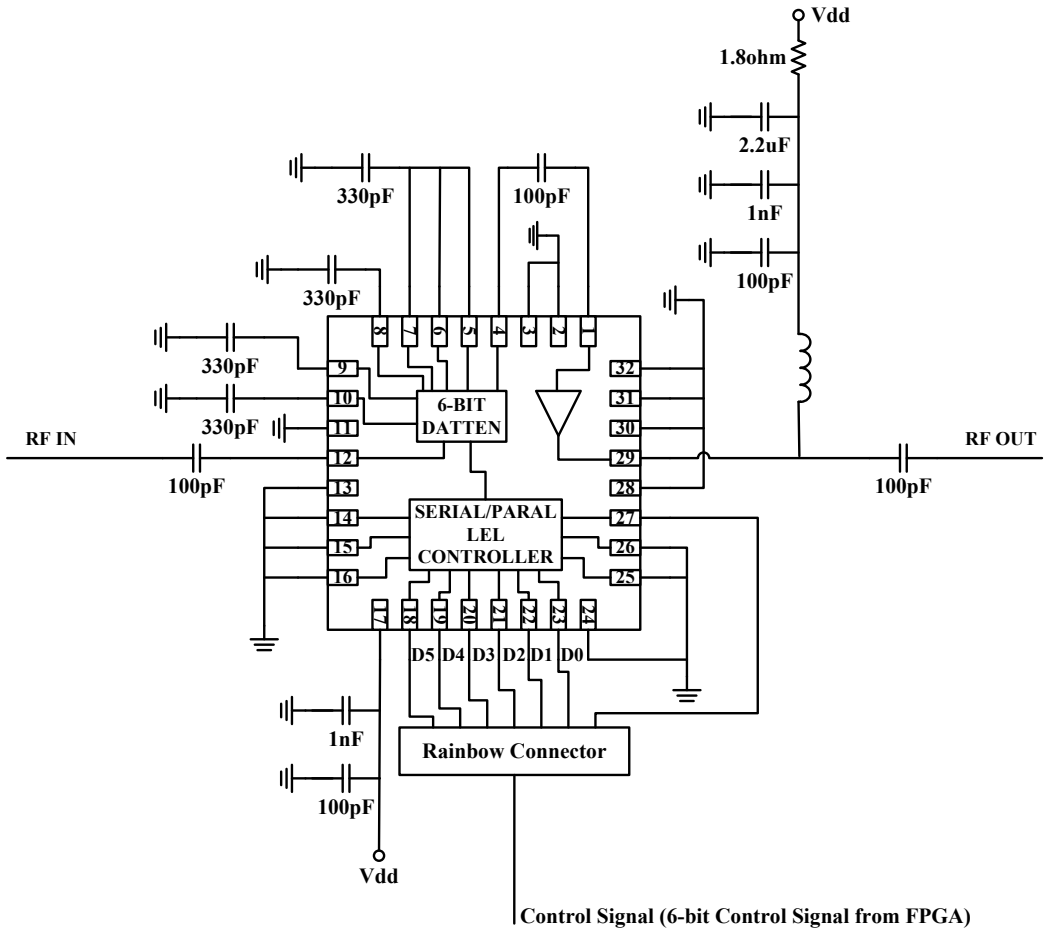


Figure 5.18 DVGA in test circuit configuration [31]

5.3.1.2 CONTROL SIGNAL GENERATION ALGORITHM

Different with the feed-forward design, the received signal reaches FPGA at the end of DCSR receiver and is processed. The envelope amplitude information is extracted by FPGA and then the corresponding correlative control signal is generated and sent back to DVGA for signal strength adjustment. In the following paragraphs, the operation of the feedback AGC is elaborated.

In the DCSR receiver, the received 4ns duration pulse is first expanded or broadened from 4*ns* to 37*ns* through the process shown in Figure 5.19 (as described in the previous chapter). Then the broadened pulses are sampled by ADC (ADC08100 from Texas Instrument) with a sample clock of 80MHz produced by FPGA (Figure 5.19(c)). Within the 50ns frame duration between two pulses, each pulse is sampled and represented by four digital points (A, B, C and D). FPGA picks the first three points (A, B and C) for timing recovery and signal synchronization while leaves point D as a watershed between two adjacent pulses. When clock synchronization is realized, Point B should have the peak value comparing to other points and is identified as the sampled result of the pulse for code detection.

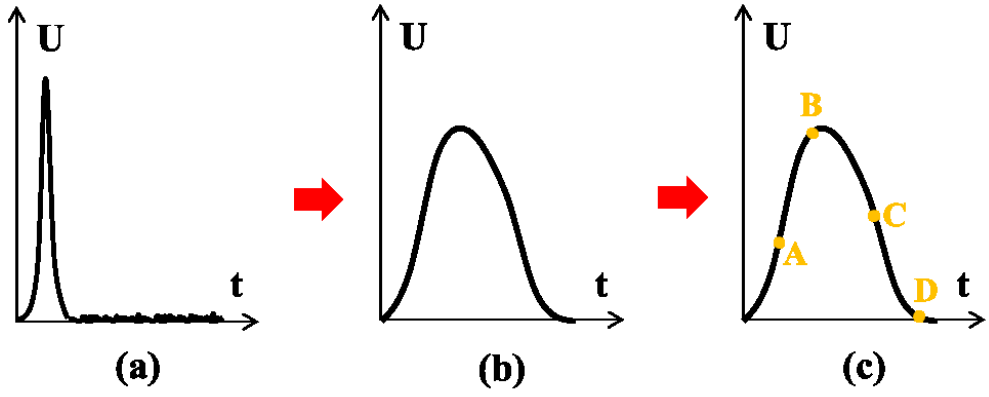


Figure 5.19 The pulse broadening sampling process in DCSR receiver

The proposed control signal generation procedure takes advantages of the above sampling and pulse broadening process with the field programmable gate array (FPGA) and very-high-speed integrated circuit hardware description language (VHDL). The flowchart of the control signal generation is shown in Figure 5.20. At the starting point, the sampled points $data\_in$ (A, B, C and D) are picked by FPGA at the clock of

80MHz, and are employed to calculate the average signal strength env. Afterwards, a comparison takes place between the average signal strength env and the default signal strength env_def. The default signal strength env_def is set up to achieve the best signal synchronization performance. There are three different comparison results: (a) the average signal strength env is greater than the default signal strength env_def; In such a case, FPGA will produce a smaller control signal $control\_out$ to reduce the gain; (b) env is less than env_def; FPGA will produce a larger control signal to raise the gain; (c) env is equal to env_def, in which FPGA will retain the control signal at the current value.

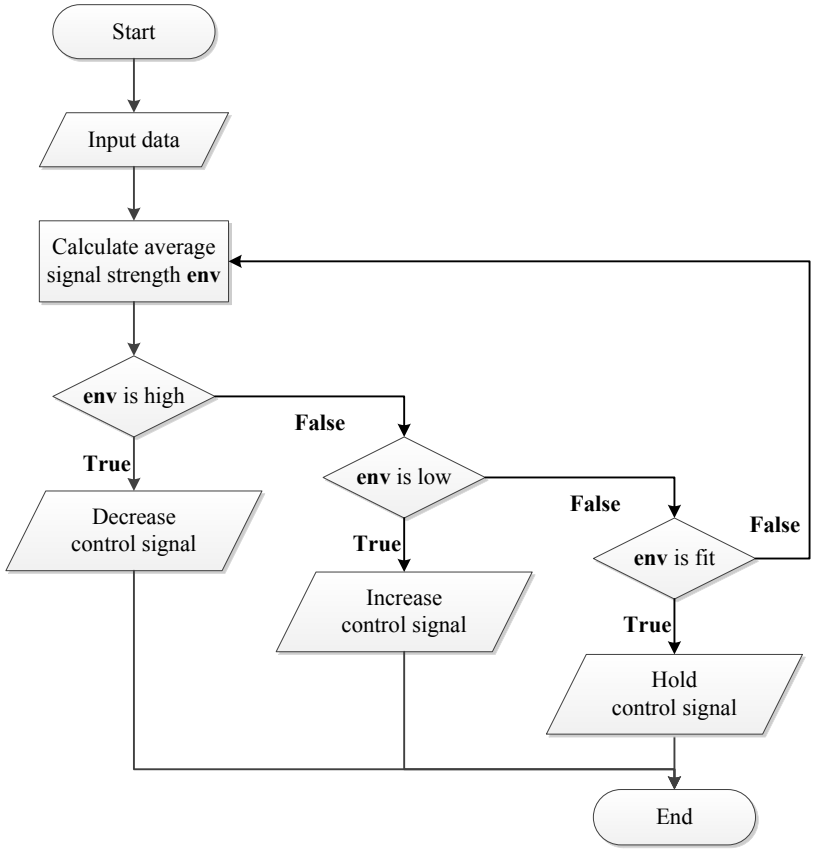


Figure 5.20 The basic flowchart of the proposed control signal generation

To be more specific, the proposed control signal generation algorithm has three parts:

a. Average calculation of the signal strength:

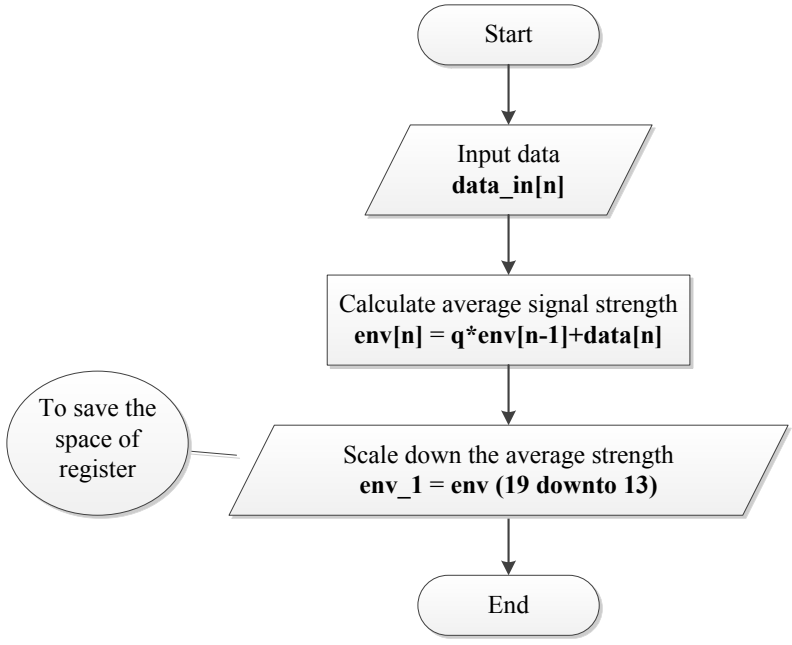


Figure 5.21 The flowchart for average signal strength calculation

As shown in Figure 5.21, when the input data has arrived following the rising edge of the 80MHz clock, the average signal strength env is calculated based on the concept of moving average filter (which is a sort of digital low-pass filter) using a statistical approach [32]. In brief, moving average filter utilizes a register with a length of N to store continuously sampled data, and then measure the average value of these N data elements. When the latest sampled data has arrived, the oldest data needs to be removed for a new round of measurement, as shown in Figure 5.22. The merit of this method is that smooth renewal can be acquired with the newly arrived data. The average signal strength env is determined by the following equation:

$$\begin{cases} env[n] = env[n-1] - 2^{-m} \times env[n-1] + data\_in[n] \\ = q \times env[n-1] + data\_in[n] \\ q = 1 - 2^{-m} \end{cases} \quad (5.6)$$

, where n is the number of current 80MHz clock period, m determines the loss rate of oldest data, and q is known as forgetting factor. Owing to the VHDL implementation of the control signal and the storage of data in binary format, it is very simple and efficient to achieve diverse loss rate by shifting the previous binary average signal strength $env[n-1]$ to left or right. At last, the average signal strength env is down scaled to env_1 for further usage.

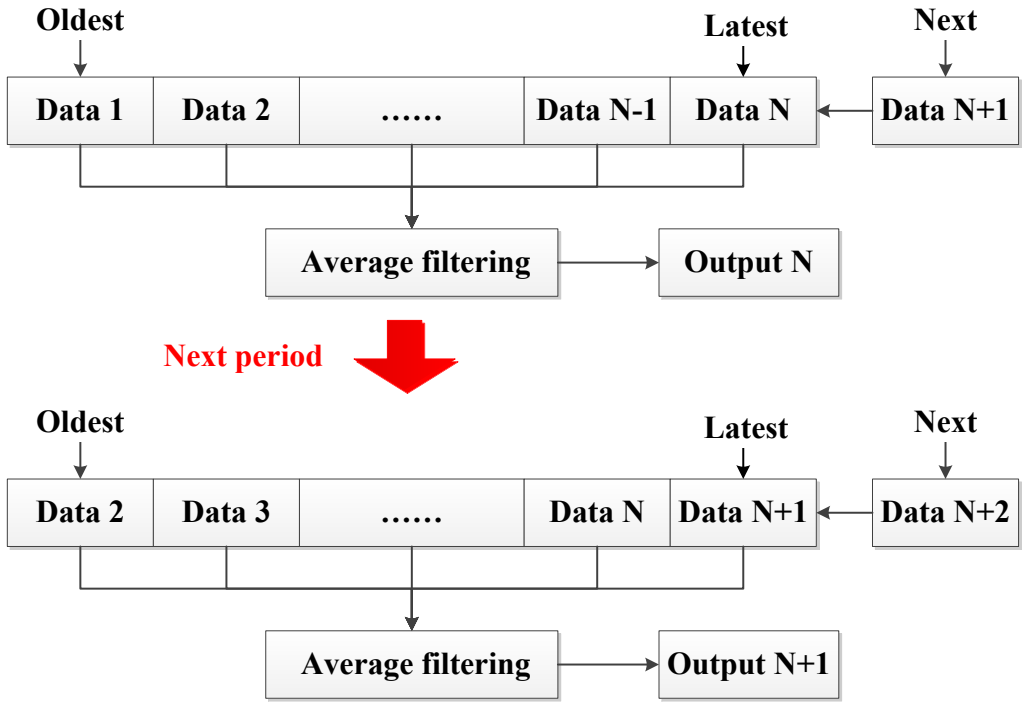


Figure 5.22 The basic moving average filtering procedure

It should be noted that timing recovery and signal synchronization process use only the first three sampled points (A, B and C) while the proposed control signal generation

algorithm utilizes all four sampled points (A, B, C and D) for average signal strength calculation. The reason is obvious. The sampling process depends on the 80MHz clock controlled by timing recovery function, which means, if the clock synchronization has been lost on account of unexpected situation, significant amplitude information might be lost with calculating only three points since it is possible that Point D is holding the vital amplitude value. Hence, the proposed control signal generation algorithm makes the best use of all sampled points.

b. Comparison of the signal strengths

The purpose of the average signal strength comparison is to detect deviation of the received signals from the expected level. Generally, the differences between the average signal strength and the default signal strength are considered and programmed in four situations for signal strength adjustment: when the difference is huge, coarse tuning of the gain is applied to DVGA for quickly adjusting the signal to the desired range; when the difference is normal, a normal-speed tuning is used; when the difference is light, fine tuning of the gain is applied to smooth the adjustment which means a stable output signal for DVGA; when there is no difference between the average signal strength and the default signal strength, no tuning is required. Coarse tuning is implemented to shorten the adjusting period of the control signal, while fine tuning is implemented lengthening the adjusting period.

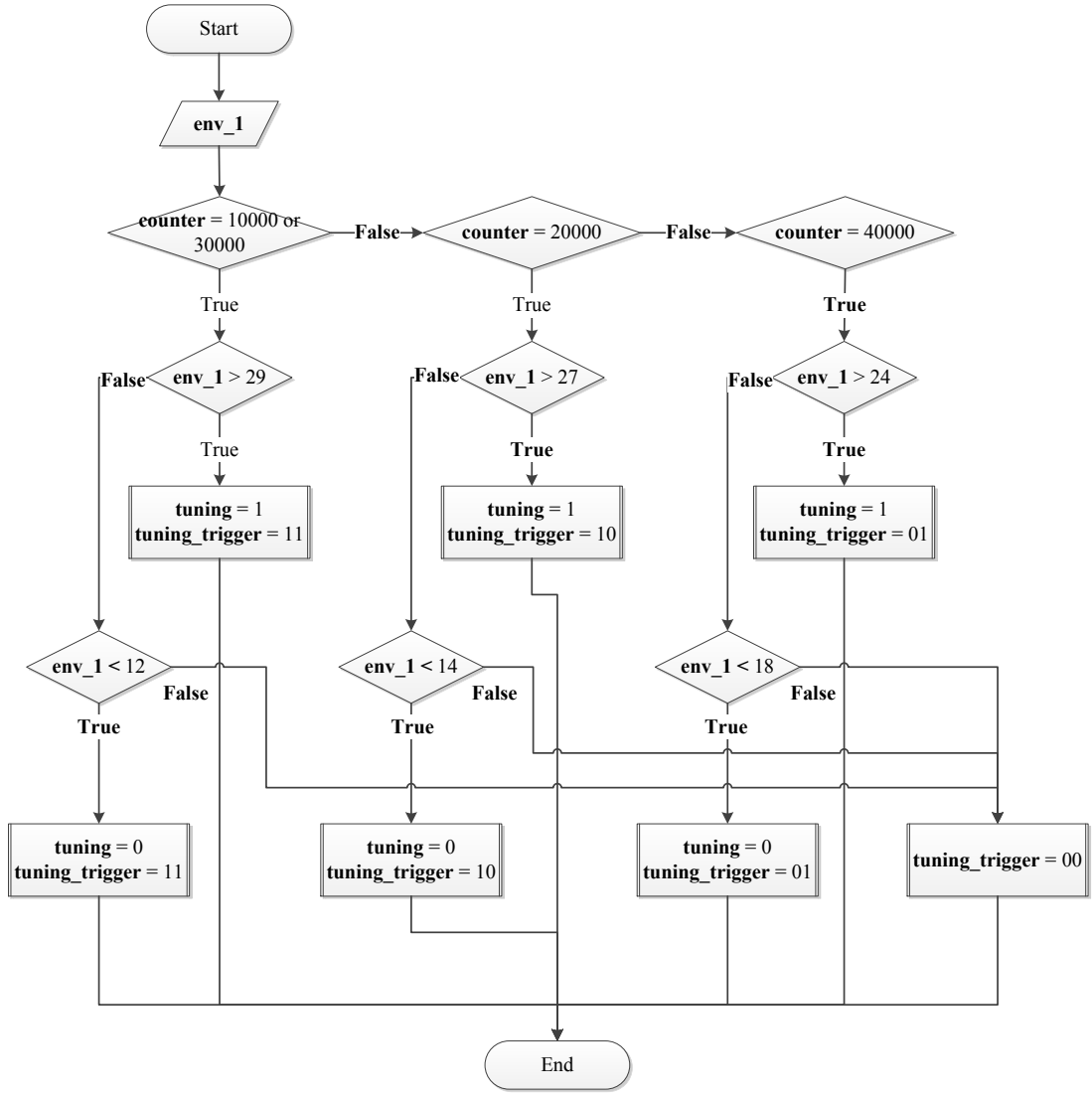


Figure 5.23 The sub flowchart for signal strength comparison

As shown in Figure 5.23, the $counter$, which is driven by the rising edge of the 80MHz clock, is utilized to control the adjusting period. When the $counte$ is equal to 10000 or 30000, the comparison occurs. If the difference is huge, the $tuning\_trigger$ is set up to "11" to indicate that coarse tuning is needed, along with the $tuning$ set up to "1" to express the average signal strength is too strong or "0" to express the average signal

strength is too weak; if not, the $tuning\_trigger$ is set up to "00" to indicate that no tuning is required. Similarly, when the $counter$ is equal to 20000 or 40000, the comparison is made for normal-speed tuning or fine tuning. When the $counter$ reaches 40000, it will be reset to zero at next rising edge of the clock. When the received signal needs coarse tuning, the adjusting frequency is double of the frequency for normal tuning; when the received signal merely needs fine tuning, the adjusting frequency is half of the frequency for normal tuning. The values of default signal strength shown in the flowchart have been optimized through experiments.

c. Adjustment of control signal

The process of adjustment of control signals is relatively simple. The original control signal is set to "101111" which presents the gain of 0dB. The $tuning\_trigger$ judges the tuning level of the control signal to be coarse, normal, fine or none; meanwhile the $tuning$ signal determines the tuning type to be positive or negative. The collection of all possible situations is presented in Table 5.2. Figure 5.24 is the flowchart for the operation.

$tuning\_trigger$	$tuning$	Tuning type
00	0	No tuning
	1	No tuning
01	0	Positive fine tuning
	1	Negative fine tuning
10	0	Positive normal tuning
	1	Negative normal tuning

tuning_trigger	*tuning*	Tuning type
11	0	Positive coarse tuning
	1	Negative coarse tuning

Table 5.2 Collection of all possible control signal adjustment types

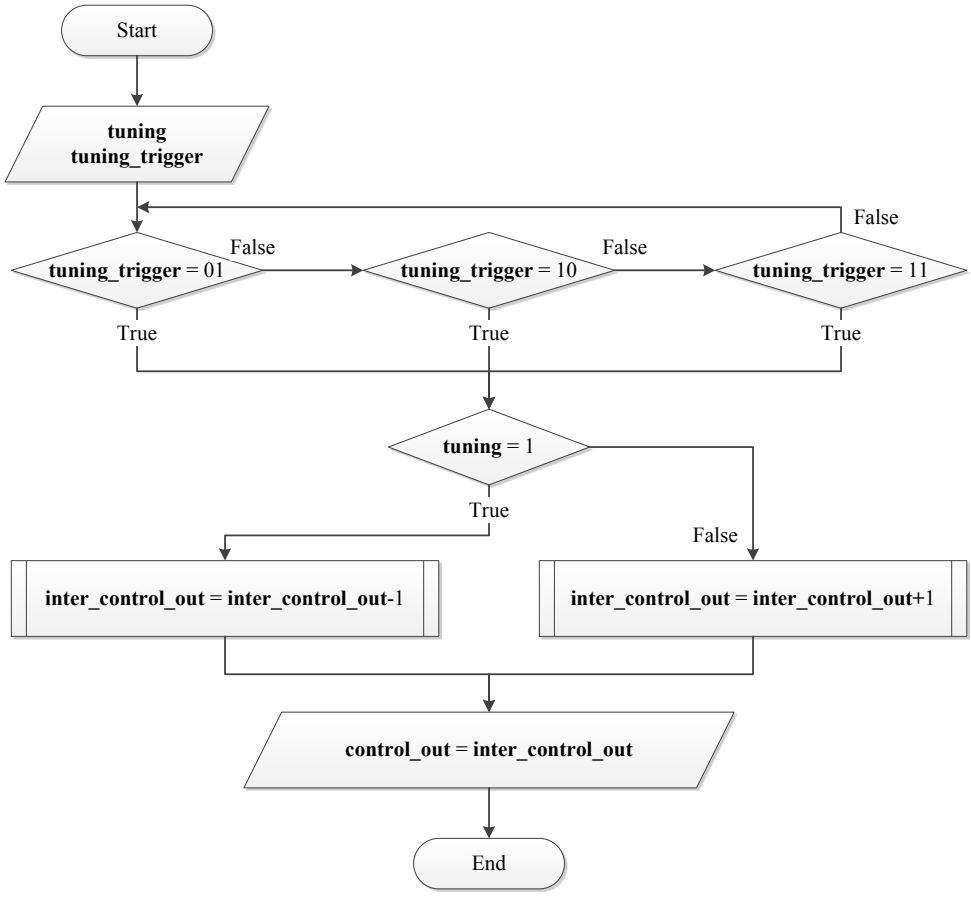
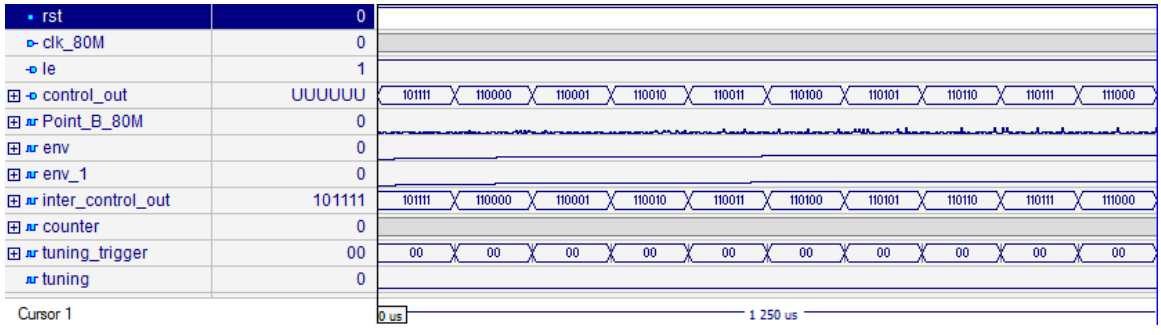


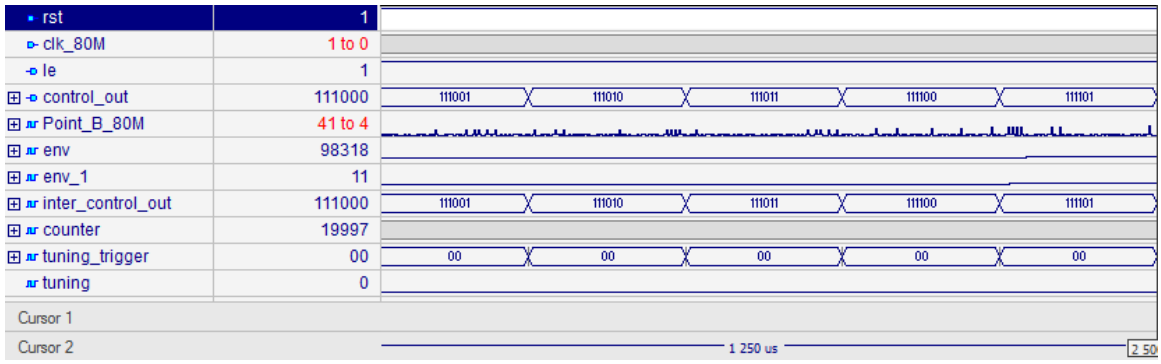
Figure 5.24 The sub flowchart for control signal adjustment

5.3.2 SIMULATION RESULTS

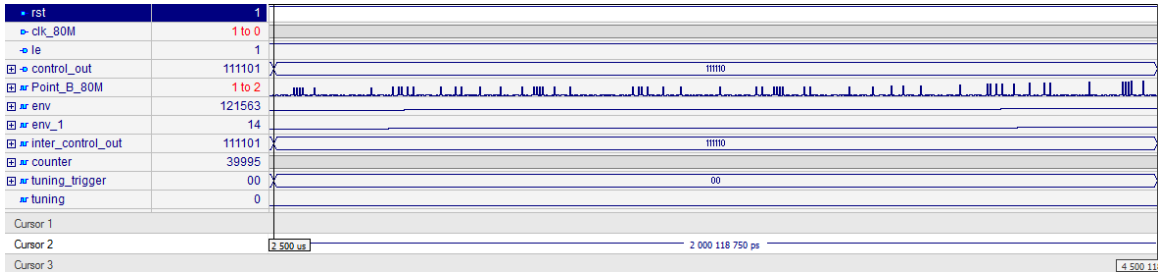
Simulation of the proposed control signal generation algorithm was executed in Active-HDL, which is a FPGA design simulation software made by ALDEC. The relevant VHDL code contains three main sections: libraries, entity and architecture. The library section contains the libraries that are called by the design. The entity section describes the name of the design and defines all inputs and outputs, which can be imagined as component symbol in a circuit schematic. The third section, architecture, defines all internal signals and specific functions. Figure 5.25 shows the simulation results of the proposed control signal generation algorithm from 0μs to 9000 μs. "rst" is the reset signal to initialize the whole process. "clk_80M" is the clock signal to trigger every action during the process. "LE" is a logic control signal sent directly to DVGA for the parallel control interference configuration. "$Point\_B\_80M$", which is simulated as the real sampled signal, is in lieu of actual input signal $data\_in$ only for simulation purpose. Other signals have been introduced in Section 5.3.1.2. Both "rst" and "clk_80M" were stimulated by Active-HDL.



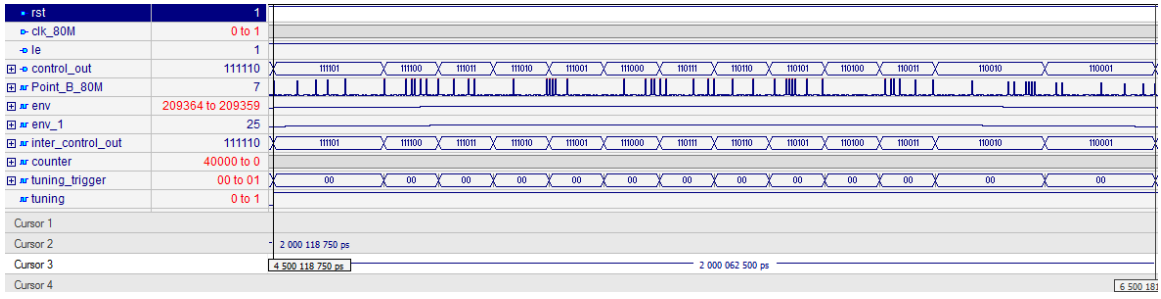
(a) 0μs - 1250μs



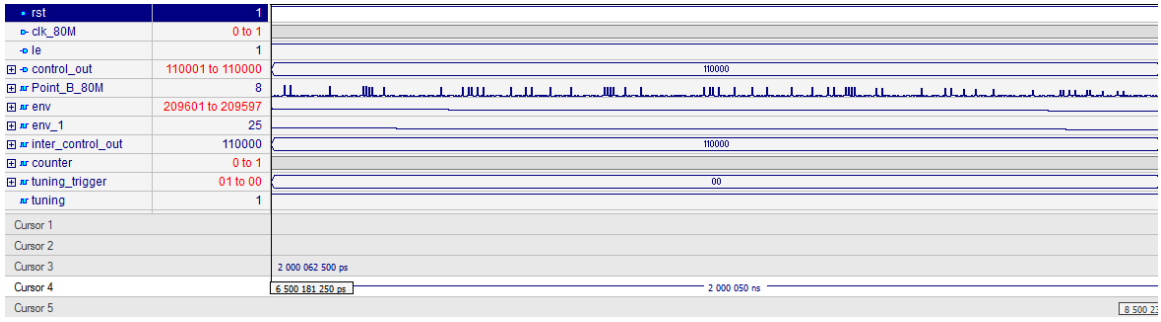
(b) 1250µs - 2500µs



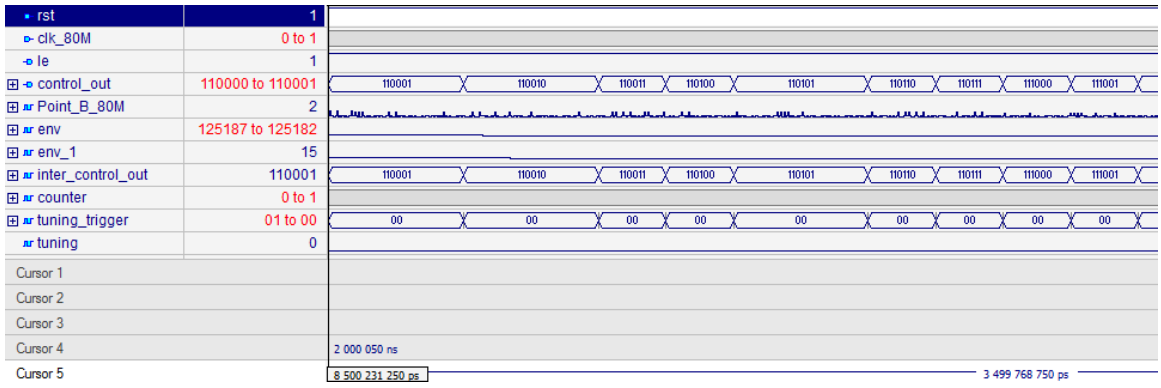
(c) 2500µs – 4500µs



(d) 4500µs - 6500µs



(e) 6500µs - 8500µs



(f) After 8500μs

Figure 5.25 Simulation results of the proposed control signal generation algorithm

From the simulation results, it can be seen that the calculated average signal strength "env" and "env_1" are able to reflect amplitude envelope variation of the input signal properly. When the input signal is much weaker or stronger than the default level, as shown from 0 μs to 1250μs, from 4500μs to 6500μs and after 8500μs, the "$tuning\_trigger$" and "$tuning$" signal are able to generate corresponding tuning information to increase or decrease the control signal "$inter\_control\_out$" rapidly. From 1250μs to 2500μs, it can be observed that while the input signal approaches to the default level, the tuning speed slows down.

It should be noted that owing to mismatch between the long simulation time and the limited display resolution, a number of pulses in "$Point\_B\_80M$", which are able to see in a zoom-in view, are not displayed in Figure 5.25. Nonetheless, the simulated amplitude variations of the input signal corroborate well with the simulations.

5.3.3 IMPLEMENTATION RESULTS

Like the first design, the proposed feedback AGC was fabricated on FR4 double-sided copper-clad printed circuit board (PCB) using grounded coplanar waveguide (GCPW). All components were surface mounted. The layout of the proposed feedback AGC was done with EAGLE PCB Design Software. The FPGA is Lattice ECP2 FPGA evaluation board. Figure 5.26 shows the top layer of the PCB layout with the schematic presented in Figure 5.18, while Figure 5.27 shows the PCB implementation. The waveforms were measured and captured by Agilent 54831D 4+16-Channel, 600 MHz Mixed-Signal Infiniium Oscilloscope. The S-parameters were measured with Agilent 8722ES 50MHz – 40GHz S-parameter network analyzer. The bit error rates were measured with Tektronix 200Mb/s BERT transceiver packet BERT™200.

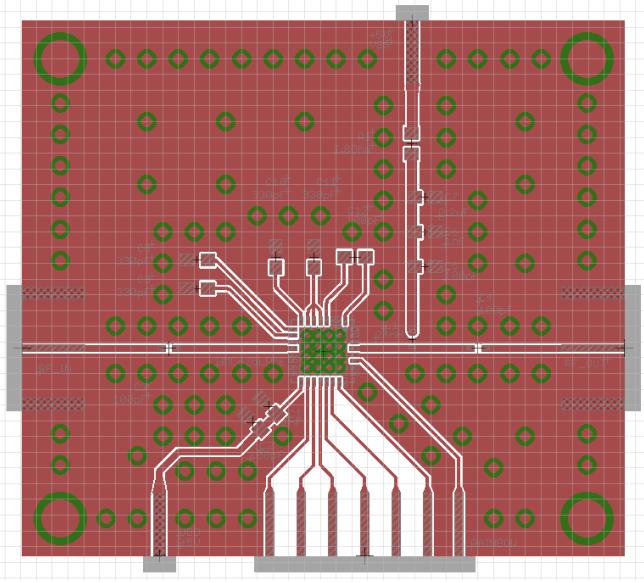


Figure 5.26 PCB layout of the proposed feedback AGC (top layer)

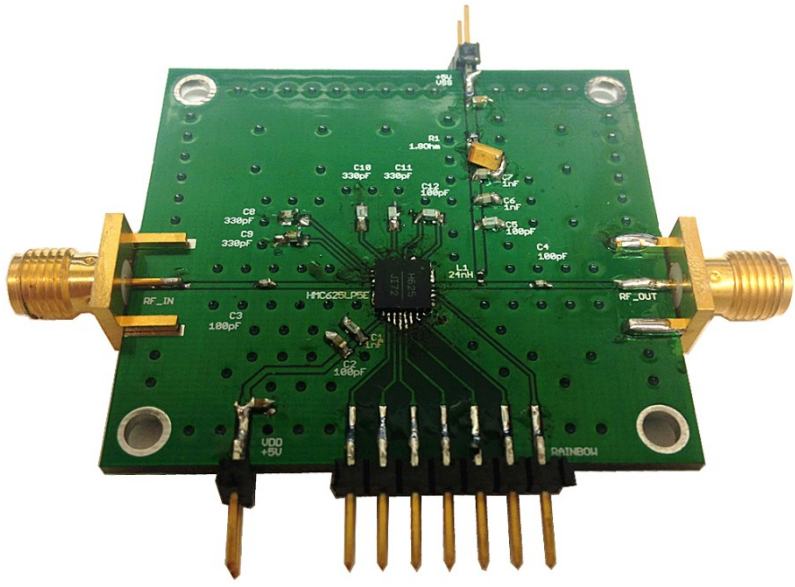


Figure 5.27 PCB implementation of the proposed feedback AGC

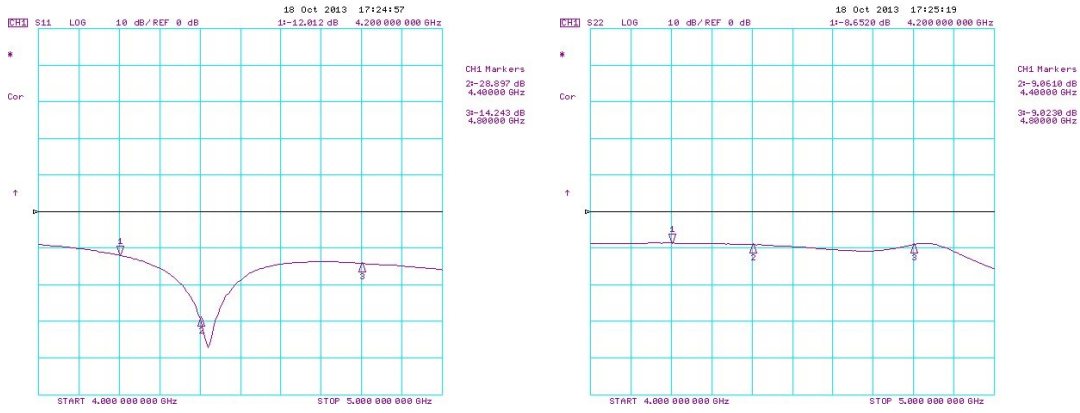
5.3.3.1 GAIN VARIATION RANGE TESTING

The effective gain variation range of DVGA was measured with Agilent 8722ES 50MHz – 40GHz S-parameter network analyzer. The measurements started at 4GHz and stopped at 5GHz. Figure 5.28 shows the measured results: (a) is S21 that has a value of 8.283dB at 4.44GHz while testing with a control signal “111111”; (b) is S21 that has a value of -22.985dB at 4.44GHz while testing with a control signal “000000”; (c) is S11 whose value is -28.897dB at 4.44GHz; (d) is S22 whose value is -9.061dB at 4.44GHz. As presented in Table 5.1, the gain of the proposed feedback AGC is able to vary from -22.985dB in attenuation to 8.283dB in amplification. Table 5.3 describes the actual value of gain variation of DVGA.

AMP/ATT (dB)	Relative AMP/ATT (dB)	D5	D4	D3	D2	D1	D0
8	0	1	1	1	1	1	1
7.5	-0.5	1	1	1	1	1	0
⋮							
0	-8	1	0	1	1	1	1
-0.5	-8.5	1	0	1	1	1	0
⋮							
-23	-31	0	0	0	0	0	1
-23.5	-31.5	0	0	0	0	0	0

Table 5.3 The actual value of gain variation of DVGA

(a) (b)

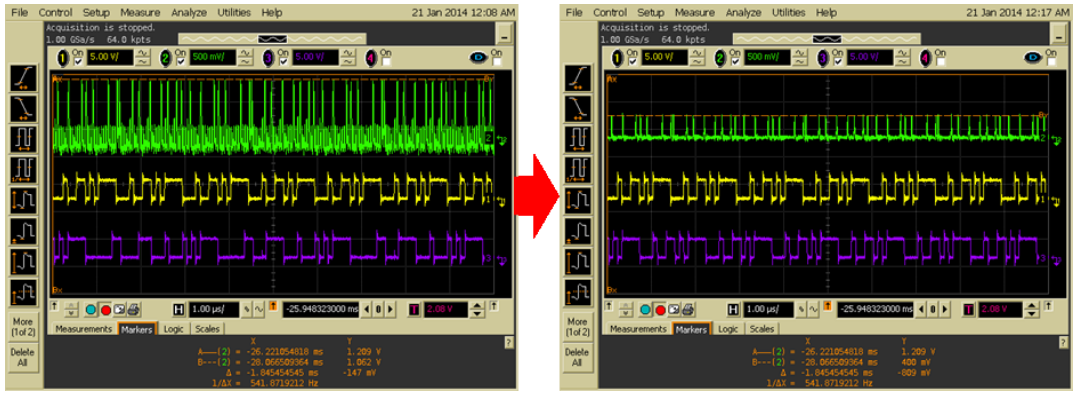


(c) (d)

Figure 5.28 Measured S-parameters of the proposed feedback AGC

5.3.3.2 INDOOR ENVIRONMENT TESTING

Test of the performance of the proposed RF feedback AGC board in the entire DCSR system was made with a wireless connection between the transmitter and the receiver. The measurement was set up inside Dalhousie RF/Microwave Wireless Research Laboratory. Figure 5.29 shows the test results of the proposed feedback AGC. For comparisons, tests were done with and without the proposed RF AGC under the same environmental conditions. Figure 5.29 shows the results where the pairs of the "without" results (on the left side) and the "with" result (on the right side) come with the same environment set-ups.



(a)

(b)

(c)

Figure 5.29 Implementation results without/with the proposed feedback AGC within indoor environment

The green signal is the output of active-LPF at energy detection stage. The reason to check only the output signal is due to the 600 MHz bandwidth of the oscilloscope available in the lab. The yellow signal is the original DCSR bit sequence generated by FPGA on the transmitter side. The purple signal is the recovered DCSR bit sequence produced by FPGA on the receiver side. Three situations of different distances between the transmitter and receiver have been tested and the results are shown in Figure 5.29.

a. The distance between the transmitter and the receiver is set to be only 48cm that leads to strong received signal (the high pulse amplitude is 1.062V) exceeding the saturation level of the LNA at the signal recovery stage. Without the proposed AGC, pulse amplitude ratios will change and the transmitted DCSR bit sequences are unable to be recovered. With the proposed AGC added to the system, the received signal has been attenuated and stabilized with an envelope of 400mV; the ratio distortion disappears and the transmitted DCSR bit sequences have been recovered successfully.

b. The distance between the transmitter and the receiver is set to be 5.18m that leads to weak received signal (the high pulse amplitude is only 121mV). Without the proposed AGC, the received signal is unable to be recovered, since the signal received is too weak to distinguish the differences between sampled points. With the proposed AGC, although the envelope of received signal is not raised to the ideal level of 400mV, it is large enough to allow the successful detection of the DCSR bit sequence.

c. The distance between the transmitter and the receiver is set to be 3.21m that leads to normal level of the received signal (the high pulse amplitude is 435mV). With

the AGC, the received signal envelope is able to be maintained at the level of the 401mV.

More laboratory tests have also been carried out with the antennas being moved around or even invisible to each other, the proposed feedback AGC has the ability to adjust the received signal smoothly and steadily.

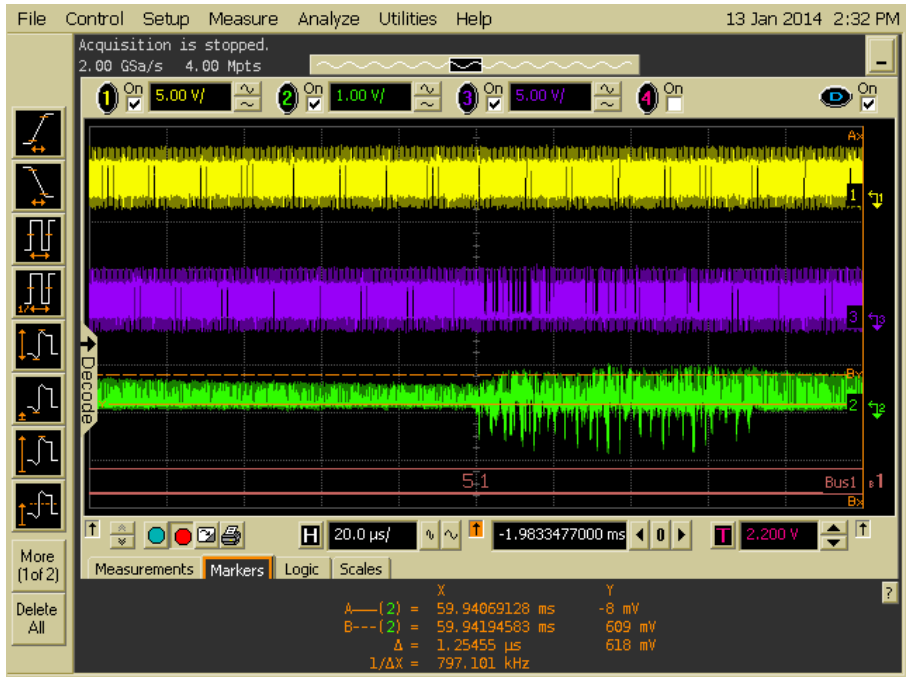
BER test results in the above three situations are shown in Table 5.4. It can be seen that the introduction of the proposed RF feedback AGC makes a quite improvement to system performance.

Original signal strength	AGC connection	Envelope of received signal	BER
too strong	without	1.062V	3.29×10^{-3}
	with	400mV	1.38×10^{-5}
too weak	without	121mV	4.59×10^{-2}
	with	165mV	7.48×10^{-3}
normal	without	435mV	6.26×10^{-6}
	with	401mV	3.81×10^{-7}

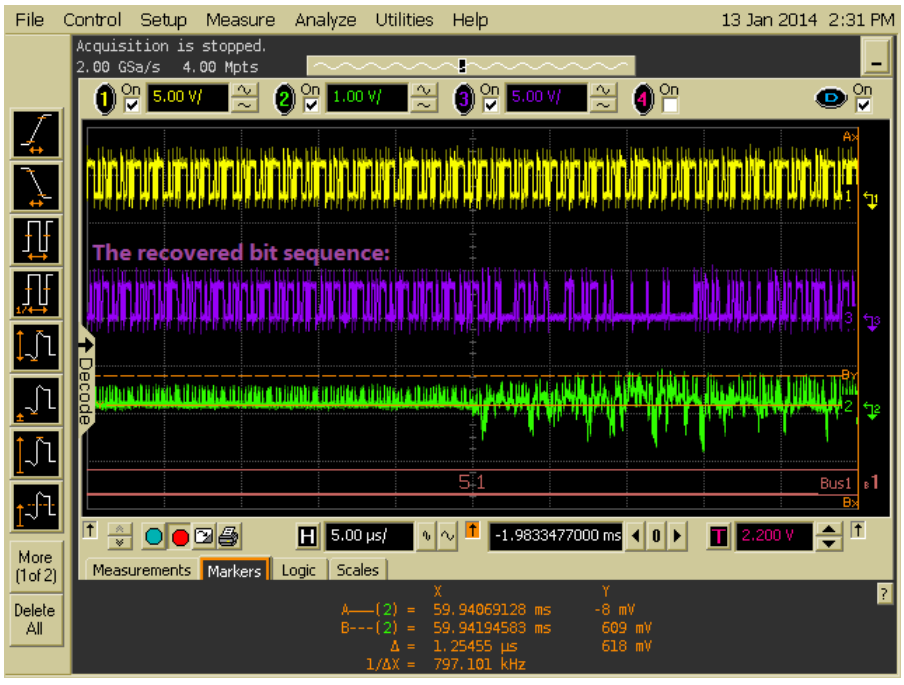
Table 5.4 BER testing results of indoor environment

Although the proposed AGC improves the BER, the values of BER are still not as good as expected in the cases of "too strong" and "too weak" signals. After some experimental investigations, two external interferences are discovered as the possible causes of the not so good BER.

The first interference appears at times with duration of around 70µs, as shown in Figure 5.30 (there (b) is an expanded version of (a), which shows the expanded waveform). When such interference occurs, useful waveforms are overwhelmed. First, the interference was suspected to be picked up only from the receiver antenna so receiving antenna was removed. However, the interference was found to still exist. Then, a copper box was made and soldered to the ground plane of the proposed AGC as the shielding cover as shown in Figure 5.31, while other boards and components were covered with grounded aluminum foils. The interference was found to completely disappear. The value of BER in the "too strong" case then drop to the order of 10^{-7}. This suggests that the DCSR requires a good shielding case to isolate it from the external interferences.



(a)



(b)

Figure 5.30 The first type of interference

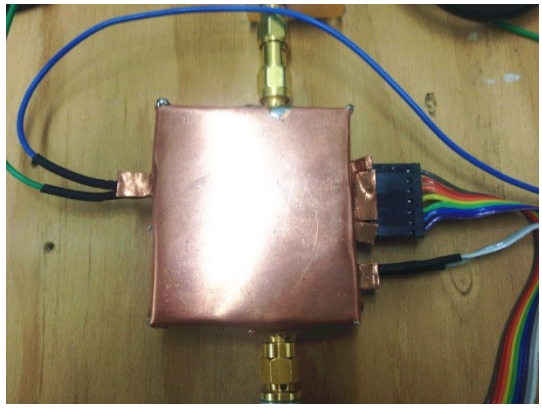
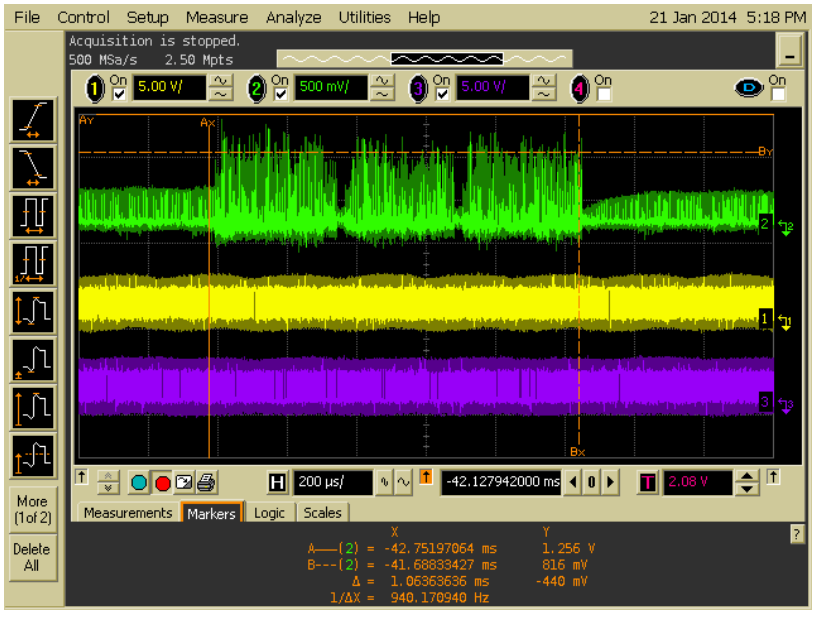


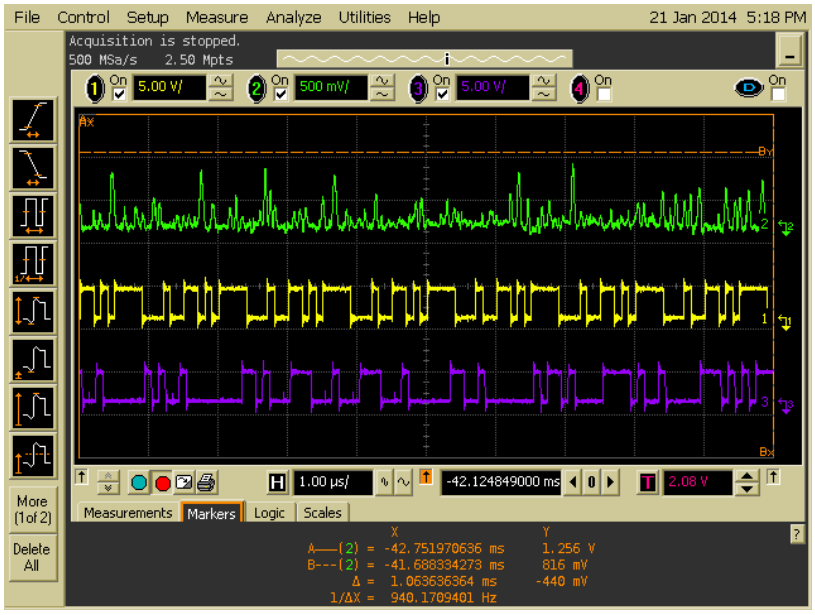
Figure 5.31 Shielding cover of the proposed feedback AGC board

The second of interference occurs periodically every 100ms with duration of around 1ms, as shown in Figure 5.32 ((b) is an expanded version of (a), which shows the detailed

waveform). Like the first interference, it also overwhelms the UWB signal waveforms. The strength of this interference was found to be proportional to the distance between the transmitter and receiver antennas; that is, the longer distance, the weaker the received signal and the stronger interference. As a result, this interference must be an external signal that falls into the UWB band. To locate the interference source, all electronic devices inside the laboratory, which night cause electromagnetic interferences, were turned off; however, the interference still existed. A spectrum analyzer was then employed to discover more specifics and identify the interference. The interference was found to have the peak of -50dBm around 5.2GHz, which fell into the 5GHz band of 802.11n Wi-Fi network, shown in Figure 5.33. Therefore, the interference came from the Wi-Fi signal sent out by a university installed Wi-Fi router installed just outside the laboratory. Since the band-pass filter used at signal recovery stage could not provide a sharp cut-off around 5.2GHz (the attenuation at 5.2GHz is only -2dB), the second interference was hard to be removed.



(a)



(b)

Figure 5.32 The second type of interference

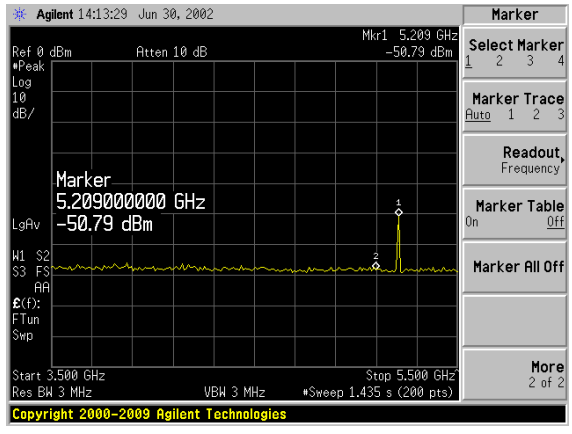


Figure 5.33 Power spectrum of the second type of interference

5.3.3.3 CHAMBER ENVIRONMENT TESTING

To observe the precise performance of the proposed feedback AGC, the testing environment was moved to an anechoic chamber which shielded all external interferences from inside equipment. The measurement results are shown in Figure 5.34. Similarly to Figure 5.29, the green signal is the output of active-LPF at energy detection. The yellow signal is the original DCSR bit sequence generated by FPGA at the transmitter side and it is used as a reference. The purple signal is the recovered DCSR bit sequence produced by FPGA at the receiver. The distances between the transmitter and receiver antennas were 20cm, 2.34m and 1.52m. It can be observed that, within chamber, the proposed feedback AGC is able to achieve the desired performance. It should be noted that the distances within the chamber are shorter than the distances in the indoor environment due to the limited size of the anechoic chambers.

(a)

(b)

(c)

Figure 5.34 Test results without/with the proposed feedback AGC within anechoic chamber

The corresponding BER test results are shown in Table 5.5. The results indicate that the proposed feedback AGC does improve the BER performance. It is further confirmed that the second interference is an external one that causes high BER.

Original signal strength	AGC connection	Envelope of received signal	BER
too strong	without	1.019V	1.4×10^{-8}
	with	416mV	0×10^{-8}
too weak	without	253mV	0.23×10^{-8}
	with	401mV	0×10^{-8}
normal	without	577mV	0.48×10^{-8}
	with	386mV	0×10^{-8}

Table 5.5 BER test results of chamber environment

5.4 CONCLUSION

In this chapter, two automatic approaches to overcome the limitation of manual signal adjustment techniques used in the DCSR IR UWB receiver design were presented. The first approach presented a solution at baseband, which had been confirmed not effective as desired. The second approach focused on a remedy at the first stage of receiver, which had been confirmed as effective objective as expected. Simulations and implementations were executed to verify the proposed approaches. The second approach was recommended to be the final solution for automatic signal strength adjustment.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSION

This thesis has presented two novel approaches for achieving automatic signal strength adjustment in the non-coherent DCSR IR-UWB receiver. The previous design employed manual attenuator to perform signal strength adjustment, which is not feasible for practical use. Details of the limitation of the previous design were discussed and two new automatic gain control techniques have been proposed and developed.

The first approach adopted the feed-forward automatic gain control technique; thus, the circuit was completely designed in the analog domain. The circuit consisted of four components: a variable gain amplifier to adjust the signal strength, a low-pass filter to detect the strength of input signal, a voltage amplifier and an inverter to generate corresponding control signal. The schematic was simulated by ADS. Fabrication was realized on PCB using GCPW technique. Laboratory tests were conducted to examine the performance of the design. Test results showed that the first proposed approach did not work well.

The second approach adopted the feedback automatic gain control technique. Both analog and digital methods were employed to complete the design. The analog circuit, implemented on PCB using GCPW technique, was made of variable gain amplifier/attenuator which adjusted signal strength with digital control signal. The digital control signal was generated and programmed in FPGA using VHDL code. It was simulated by Active-HDL and prototyped. Laboratory tests took place in both indoor

environment and chamber environment. Results verified that the second proposed approach was able to achieve desired automatic signal strength adjustment. More specifically, it achieved the input dynamic range of 179mV to 1.062V with the constant output of about 400mV.

6.2 FUTURE WORK

Since the DCSR transceiver system is a novel technology which is still at the stage of being fully developed, future work is expected to be carried out along the directions below.

a. As mentioned above, all analog circuits are exposed to external electromagnetic interferences without any shielding protection; it has led to severe interferences that adversely affect the performance of the DCSR system. Therefore, effective shielding cover should be designed.

b. It has been discovered that the current DCSR receiver is adversely by the 5GHz band of 802.11n Wi-Fi network due to low out-of-band attenuation by the current band-pass filter used. A new band-pass filter that has a sharp cut-off frequency should be used and its effect should be investigated.

c. The current DCSR transceiver system consists of two integrated FPGA boards, several PCB boards and independent components. For practical application, they should all be integrated and placed as close as possible.

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