CMOS Sensor front-end and Data Converters for interface readout applications

By

Ximing Fu

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

at

Dalhousie University
Halifax, Nova Scotia
December 2022

Table of Contents

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The need for easily interfaced sensors is ever-increasing in the growing world of computers and digital systems. System performance depends more on many applications' sensors, actuators, and interface electronics. As a result, it is becoming increasingly important to develop and improve interface electronics. This thesis proposes a low-power, high-resolution, high-sensitivity analog front-end for IoT sensor node array or Biomedical Sensor, Device, and Measurement Systems. The signal measurement under very low SNR is essential for integrated readout circuits. There are various methods used to detect the signal buried under ambient noise. An integrated lock-in amplifier (LIA) with automatic phase tuning and second-order harmonic frequency extraction is presented in this thesis. The automatic phase alignment loop implemented in the proposed single-channel LIA can directly align the phases of an input signal with a reference signal. Furthermore, the proposed LIA system also includes an enhanced signal detection method in which the 2nd harmonics of the carrier frequency (ω_{ref}) is applied. This method, unlike conventional LIA, reduces flicker noise and input offset effects that limit the signal-to-noise ratio (SNR). In terms of signal power detection, the proposed single-channel LIA architecture does not require phase synchronization between input and reference signals. The circuit is designed for a reference frequency of 100 Hz, which is suitable for biomedical applications. The LIA is implemented using 0.18-µm CMOS technology with a single power supply voltage of 1.8 V. The system consumes 360 µW at an operating frequency of 100 Hz and presents a high input sensitivity dynamic range for a detection bandwidth of 50 Hz and a FOM of 55.4 nW/Hz.

It is essential that the backend ADC after the sensing interface be low power, high resolution, and not impacted by the environment's noise level or the circuit's implementation in order to demodulate the LIA output signal in the digital domain. The Noise-Shaping SAR-ADC (NS-SAR) is one of the most promising hybrid architectures that emerged during this decade. While the conventional SAR-ADC has low power consumption and a small area, the comparator's noise and offset, quantization noise, and complimentary DAC (CDAC) thermal noise limit its accuracy. On the other hand, the sigma-delta ADC is the most used structure to achieve high precision, but due to the need for many opamps in this structure, its power consumption is high, and the area is large. By combining SAR and DSM architectures, NS-SAR-ADC can take advantage of both advantages: Like SAR-ADC, NS SAR-ADC has low power consumption and cost but simultaneously offers a high SNR comparable to conventional DSM ADCs. Additionally, NS-SAR is very amenable to scaling, making it a promising long-term development strategy. A further benefit of the NS SAR-ADC is that it requires a lower oversampling ratio (OSR) than the traditional sigma-delta modulator, resulting in a wider bandwidth. The simulation results in this thesis show that the proposed SAR ADC consumes 0.88mW at 10MS/s, with an SNDR of 89.43 dB and SFDR of 98.64 dB within 0.1 fs oversampling frequency.

LIST OF ABBREVIATIONS USED

PSRR	Power supply rejection Ratio
SNR	Signal-to-Noise Ratio
LIA	Lock-in amplifier
FSM	Finite-state machine
APA Loop	Automatic phase tuning
SC integrator	Switch capacitor integrator
SAR	Successive approximation
PCB	Printed Circuit Board
pk-pk	Peak-to-Peak
PVT Process,	Voltage and Temperature
PWM	Pulse Width Modulation
DTD	Die-to-Die
PLL	Phase Locked Loop
SS	Slow-Slow
FF	Fast-Fast
SF	Slow-Fast
FS	Fast-Slow
NS	noise shaping
LDO	Low dropout regulator

ACKNOWLEDGMENTS

I would like to thank my supervisor Prof. Kamal El-Sankary for his guidance, funding, and support throughout the research work for this thesis. I also want to thank Prof. Dalton Martini Colombo and Prof Yadong Yin. Prof. Yushi zhou and Prof. Issam Hammad, Prof. Yuan Ma for being part of my supervisory committee, and Prof. Li hong for serving as the external Ph.D. examiner.

I wish to thank our department secretary Nicole Smith for her help and support on countless administrative matters during my Ph.D. studies. I express my heartfelt gratitude to my parents for their unending patience and support throughout this long journey. Moreover, I express my sincere respect for my colleagues Pierre Leduc, Ge Yang, Yan Ming, Wang Shihao. Finally, I express my true feelings about the years of studying experience in the academy; Failure is not the mother of success, but rather, small steps of success lead to larger successes.

It is a great privilege for me to study abroad and change my life as a result of the opportunities provided by the Chinese government and the Chinese Communist Party, as well as the Canadian government, Dalhousie University, and both the men and the women funded, appreciated, loved, believed, and encouraged me on my journey through life.

Ultimately, I wish all people's dreams will come true, and the world will be at peace.

CHAPTER 1 INTRODUCTION

1.1 SENSORS FOR FRONT-END INTERFACE TECHNICAL INTRODUCTION

1.1.1 POTENTIAL OF CMOS SENSORS FOR FRONT-END INTERFACE READOUT APPLICATIONS

Today, most electronic devices use sensors to detect physical environmental phenomena (such as temperature, pressure, or light intensity). Sensors convert physical events into electrical signals that are to provide useful information to the users. Due to many sources of interference in the modern environment (electronic devices, cars, mobile phones, etc.), it is important to condition and process the electrical signals from the sensor with a high signal-to-noise ratio (SNR), as the signals are small and susceptible to corruption.

Featured by small size, high reliability, low power consumption (battery-powered devices), and low production costs, CMOS integrated circuits are widely used in the sensors. In the conventional sensor system, the incoming data is sampled and processed in the sensor node, subsequently transmitted to controlling devices, e.g., microcontrollers adopted in smaller electronic systems, or embedded systems, and microprocessors commonly used in mobile phones, and laptop computers [3]-[8].

Sensors for front-end interface readout applications are also increasingly used in fundamental and applied research fields such as chemistry, biology, and biomedicine, as well as in developing emerging technologies such as machine learning automata, automated vehicles, and secure and resilient internet technology infrastructures. Low-power, front-end sensor products are highly desirable in long-lasting autonomous portable equipment. In the field of interface readout circuits, smart front-end sensors within wireless sensor networks (WSN) are representative examples of CMOS interface readout circuits. It is often not possible to recharge or replace batteries on a regular basis, which requires low power consumption and low supply voltage during the design process [1-3]. In this energy-constrained scenario, taking the proper acquisition of sensor data in high-noise environments becomes an even more challenging task. When the supply voltage decreases, the readout output signals may become very small compared to the signal noise level. Linear filtering is not an option. Therefore, unique treatments are needed to extract the signal information.

Signal conditioning is essential for any technology that interacts with the physical world. In order to extract accurate signals for monitoring and controlling systems, sensor ICs connect directly to the outside environment and provide the needed signal conditioning. As a typical example in IoT applications, sensor interfaces are bridges between devices and sensors connected to the IoT. Sensor interfaces transmit data from sensors to devices. Such as a water level sensor sending data to a radio transmitter. Another typical example can be found in I²C interface applications; in addition to being a widely used and ubiquitous interface, I²C is also popular due to its relative simplicity and ease of integration, which allows many devices to be integrated on a single platform.

1.1.2 DESIGN CHALLENGES IN SENSORS FOR FRONT-END INTERFACE

Due to the high level of noise present in this energy-constrained scenario, acquiring sensor data becomes even more challenging. In the event of a reduced supply for future technology advances, sensor output signals may be very small as compared to noise levels. Sensors integrated with electronics are referred to as smart front-end sensors. Several problems are associated with this application, including the low output signal level compared to the noise level, which can significantly exceed signals of interest, particularly in noisy environments. Consequently, special amplification techniques are required in order to increase the signal-to-noise ratio [1]-[10].

Various standard techniques and tools are utilized in order to design on-chip analog components for front-end interface readout applications; Several key components are incorporated into the proposed high-resolution sensor interface, including lock-in amplifiers interface readout, driver amplifiers, noise-shaping SAR-ADCs, low noise, high precision BGR and large dynamic capacitive range LDOs with ultra-high-speed. Using lock-in amplifiers, driver amplifiers, and high-resolution noise-shaping SAR-ADCs, the proposed sensor front-end will mitigate the ongoing scaling of CMOS technology. With the NS-SAR-ADC, for example, the accuracy of analog components (CDAC mismatch, comparator offset, noise) is traded for a higher oversampling ratio (OSR) and more digital circuitry.

The proposed LIA prototype in this dissertation is implemented in a 0.18um standard CMOS technology to overcome these previously mentioned limitations, which aims to provide fully integrated, embedded solutions for CMOS interface readout devices. With the development of

Internet of Things (IoT) sensors, CMOS technology have also enabled the development of multi-purpose, multi-band front-ends that can be fully integrated with remote processors and communication nodes. As such, this thesis covers the design of key analog components to implement low-power front-end sensor nodes. Firstly, a 1.8V, 360 uW analog LIA featuring wide bandwidth (50Hz), a wide tuneable range, and a constant high-quality factor 4th order bandpass filter with process compensation will be described. The constant quality factor and the fourth-order bandpass frequency response provide excellent performance in frequency selectivity and out-of-band signal suppression. Secondly, this thesis uses a second-order, low-power, passive-active NS-SAR ADC architecture to overcome the process variations from conventional analog design trade-offs. The third and fourth key components are a Bandgap Reference Circuit with a new high-order curvature compensation technique and an ultra-high-speed, wide dynamic range, low dropout (LDO) regulator, which maintains high sensor performance despite being insensitive to variations in reference voltage and noise in the power supply. Two potential applications using a combination of the proposed design are an IoT sensor node array, as shown in Fig 1.1(a), for long-life autonomous portable equipment, for example, to enable smart sensors within wireless sensor networks (WSN) and Biomedical Sensor, Device, and Measurement Systems shown in Fig.1.1(b).

1.2 THESIS GOALS AND RESEARCH MOTIVATIONS

The ever increasing demand for long-life autonomous portable equipment is driving the current trend toward low-power design. In the field of smart sensing, sensors within wireless sensor networks (WSN) are representative examples. They need to increase the battery lifetimes since it is often impossible to recharge or replace batteries frequently. Consequently, keeping low power consumption and low supply voltage is highly desirable.
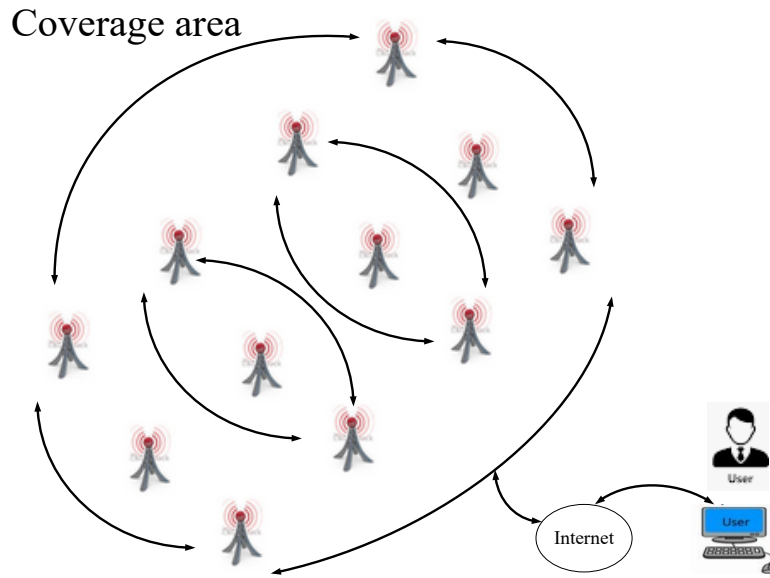
Figure 1.1 (a) A general description of the architecture of the sensor array in a wireless sensor network (WSN). [148]
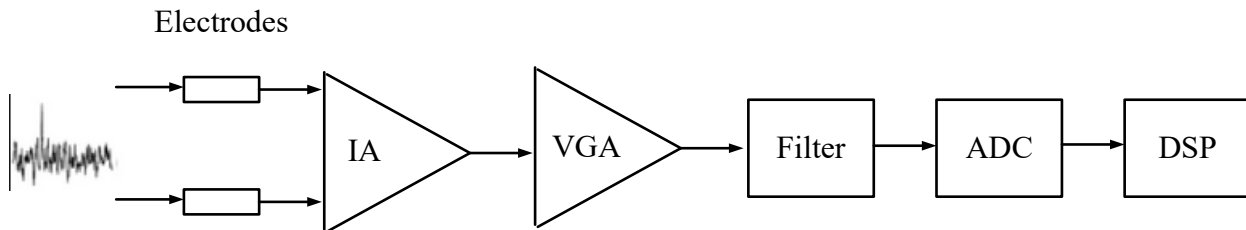
Figure 1.1 (b) Biomedical Sensor, Device , and Measurement Systems [149]
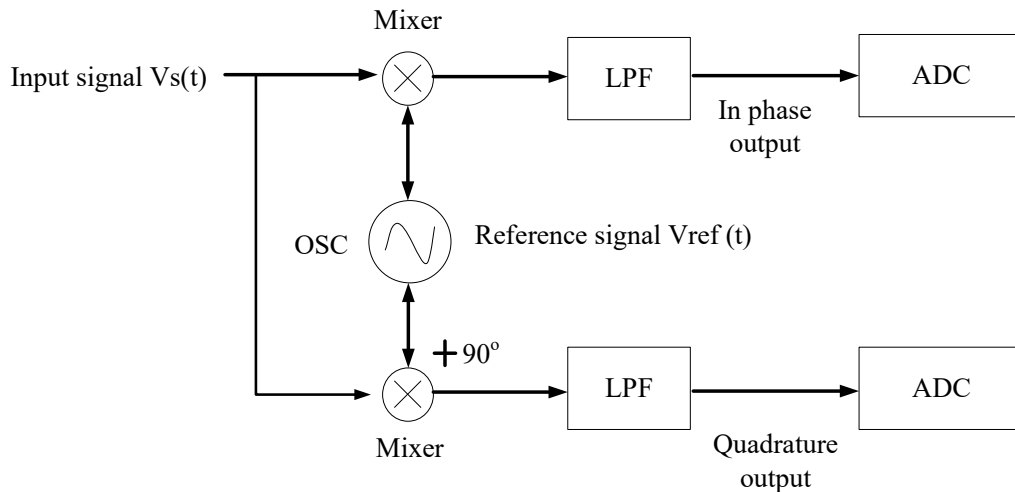
Fig 1.2 (a) Conventional Analog lock-in amplifier front-end sensor: the signal is split into two paths (in-phase and quadrature), mixed with the reference signal, filtered, and then converted to digital output.
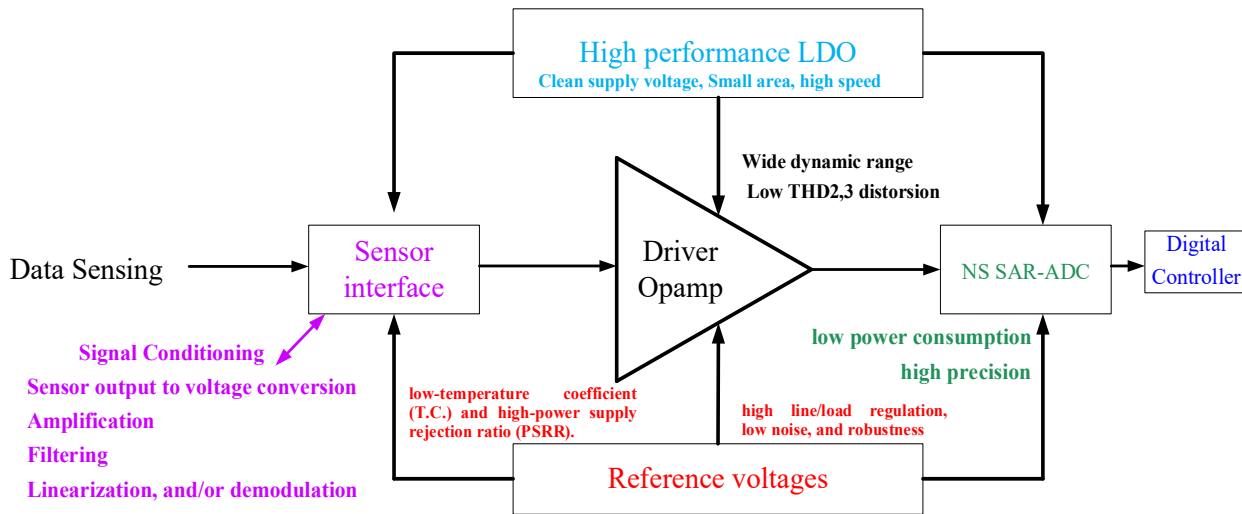
Fig. 1.2 (b) The proposed analog front-end sensor interface circuits are designed to detect very small signals for chemistry, biology, and biomedicine applications.

Besides WSN applications, with technological advancements in recent years, integrated instrumentation systems have been developed for various portable sensor-based applications, including environmental monitoring, monitoring of civil infrastructure, medical care, scientific research, chemical reaction analysis, etc. [1]-[10]. Medical, sanitary, and industrial applications currently use CMOS interdigitated electrodes (IDE) to detect, identify, and quantify cells or biochemical molecules. The thesis proposed a system-on-chip sensing system that must meet certain requirements in terms of electronic interfaces for IDE to maintain and integrate new capabilities. In addition, this includes reducing power consumption, small footprint, and signal conditioning to enhance signal-to-noise ratios (SNR) and recovering signals whose amplitudes are extremely low, usually submerged in high levels of noise, In view of the above considerations, it is necessary to employ a lock-in amplifier (LIA) based technique called coherent detection to achieve the desired results. With this technique, it is possible to detect and measure the amplitude and phase of very small signals.

The primary objective of this thesis is to design a complete sensor interface based on the previously mentioned LIA technique and its accompanying relevant circuit building blocks, including the backend NS-ADCs, the BGR, and the LDO. In conventional analog lock-in amplifiers shown in Fig.1.2 (a), analog elements such as simple RC LPF filters, voltage-controlled oscillators, and mixers are used for signal processing. ADCs build the interface between the analog and digital world.

To increase the signal-to-noise ratio (SNR) and thus recover very low amplitude signals, This thesis proposes a fully integrated single-channel, analog LIA (shown in Fig.1.2 (b)) to reduce power consumption and the size of passive components by taking advantage of a new signal power detection scheme based on 2nd order harmonic extraction and automatic phase alignment technique. The proposed LIA utilizes $2\omega_c$ harmonic instead of DC signal to improve the transient response of the LIA and overcome the 1/f flicker noise limitation with a built-in chopping technique to improve the SNR of the entire system. The automatic phase tuning mechanism for phase alignment between the reference and input signals is also proposed.

This thesis also proposes a second-order, low-power, passive-active NS-SAR ADC architecture for analog-to-digital conversion to overcome the previously mentioned problems. In contrast to prior works, passive-active integrators based on low-gain open-loop opamps are used in the loop filter instead of conventional opamp-based active integrators. Moreover, a resonator is introduced in the loop to achieve wide noise-shaped bandwidth. Zeros in the system are determined solely by capacitor ratio and positive feedback compensation, insensitive to process, voltage, or temperature (PVT) variations. Aside from noise shaping techniques, the choice of capacitive CDACs is also of critical importance. It has been demonstrated that DAC switching schemes, such as monotonic switching (MS) provide very good energy efficiency. Compared to conventional structures, this topology reduces switching-related energy losses by 81% [40]. The MS structure degrades ADC performance due to variations in the common-mode level offset within the comparator. To stabilize the dynamic amplier's input common-mode (CM) level, a common-mode-stabilization (CMS) circuit is proposed within the NS SAR ADC architecture.

To maintain high reference voltage and power supply insensitive to PVT variations and supply noise degradation. A Bandgap reference (BGR) circuit with a new high-order curvature-compensation technique is proposed in this paper. The curvature method operates by adding up two correction voltages. The first one is proportional to the difference in gate-source voltages of two MOS transistors (ΔV_{GS}) operating in weak inversion mode, while the second one (V_{NL}) is generated using a nonlinear current created by a piecewise-linear circuit. To improve the power supply rejection ratio (PSRR) and the line regulation performance, a low-power pre-regulator isolates the circuit power supply and BGR output. An ultra-high-speed, wide dynamic range, low dropout (LDO) regulator is used in high-speed digital Systems on Chips (SoCs) applications. The

piecewise speed improvement is employed in the proposed LDO to ensure ultra-high-speed operation, which divides the LDO loop dynamics into three phases.

1.3 DESIGN SPECIFICATIONS FRONT-END LIA BASED SENSOR ESTIMATION:

Using an LIA-based front-end sensor is necessary because coherent detection is an excellent method for measuring these low-level periodic signals in the presence of large amounts of noise and disturbance. The design specifications in this thesis proposal are derived as the following:

Desired Signal needed to be measured: 1uV at the center frequency at 100Hz

Some pre-amplification has to be introduced before it can be measured. Whether it is an AC amplitude meter, oscilloscope, or lock-in amplifier. However, all the amplifiers will introduce additional circuits noise to the signal,

$$\text{Input referred noise} < 400\text{nV}/\sqrt{Hz}$$

Bandwidth 1MHz and gain $= 1000$

For the above signal, the output signal of the amplifier will be:

1uV * 1000 = 1mV **(Amplifier output, by using front-end amplifier)**

However, the noise accompanied by the amplifier should be:

$$V_{n,inrefer} = \sqrt{1M} * \frac{400\text{nV}}{\sqrt{Hz}} * 1000 = 400mV \text{ (Broadband integrated noise)}$$

It is impossible to measure the signal power of interest in the presence of this noise level. The proposed architecture adopts bandpass pre-filtering (BPF) to improve the SNR of the input signal.

If the signal of interest first passes through the band-pass filter with the following:

A center frequency of 100Hz and Quality factor Q of 20 implies the 3dB bandwidth = 5Hz, a challenging specification to obtain.

The signal bandwidth = 5Hz, and the overall noise within 5Hz bandwidth will be:

$$V_{n,BPF} = \sqrt{5} * \frac{400\text{nV}}{\sqrt{Hz}} * 1000 = 890uV \textbf{ (Narrowband integrated noise by BPF)}$$

If only using the coherent detection principle by LIA, the bandwidth can be further narrowed to ideally 0.25 Hz.

$$V_{n,BPF} = \sqrt{0.25} * \frac{400\text{nV}}{\sqrt{Hz}} * 1000 = 200uV \textbf{ (LIA integrated noise)}$$

This implied that it would be possible to measure 1uV signal at the center frequency at 100Hz using the LIA technique; performance can be further improved by longer settling time, and the signal has been recovered from burying under the noise level. One of the most significant novelties of this thesis's proposed sensor architecture is combining hybrid BPF pre-filtering and coherent detection principle simultaneously to achieve high sensitivity and fast transient response since the pre-filtering technique will significantly reduce the LIA noise equivalent bandwidth required. Meanwhile, a 2nd harmonic detection method is applied, thus resulting in significant performance improvements in the proposed architecture.

1.4 TABLES OF IMPORTANT CIRCUITS PERFORMANCE ESTIMATIONS SUMMARY

Table. 1 front-end LIA sensor design parameters

Parameters	This work
Technology	180nm CMOS
Supply	1.8 V
Frequency	100 Hz
Dynamic Range	$5\mu V - 1\text{mV}$
Detection bandwidth	50 Hz
Dynamic reserve	65 dB
LIA type	Single-phase & calibration
Power consumption	$< 1\text{mW}$
Input referred noise	$< 400\text{nV}/\sqrt{Hz}$

Table. 2 backend noise shaping SAR-ADC design parameters

Parameters	This work
Technology	180nm CMOS
Order	2
ADC bits	>14 bit
bandwidth	1MHz
Fs (sampling frequency)	10MS/s
SNDR	> 80dB
Power(µW)	< 1mW

Table. 3 Driver amplifier design parameters

THD[2,3] @ (1MHz output swing (1V)	>16bit

Table. 4 Bandgap reference design parameters

TC(ppm/ºC)	5-15
Supply (V)	3.3-2.7
Reference votlage (V)	1.2
Power (µW)	<150
Line regulation(%/V)	0.005
Noise	< 100 µV (average noise)
PSRR(dB @ DC)	-80

Table. 5 LDO design parameters

Dropout (V)	0.1
Settling time	< 4us
Capacitor range	0-10nF
Technology	180nm CMOS
Supply (V)	3.3-2.2
Vout (V)	1.8
Imax (mA)	100
IQ (µA)	<500
Output capacitor (µF)	Cap-free

Fig. 1.2 (b) shows the proposed analog front-end architecture's proposed block diagram. Sensor interfaces convert measurements (i.e., temperature, pressure, humidity) into electrical signals, usually of low amplitude and carrying some noise. Afterward, the signal conditioning circuit, namely the LIA, which generally relies on operational amplifiers, performs some or all of the following tasks in the analog domain: sensor output to voltage conversion, amplification, filtering, linearization, and demodulation. The resulting analog signal is then digitized via an analog-to-digital converter (ADC) through the driver Opamp. Low noise, high-resolution BGR, and high-performance LDO are required to provide high-precision reference voltages and a clean power supply without sacrificing excessive area. Lastly, a digital system acquires, stores, processes, controls, communicates (with other devices or systems), and displays data with measurements.

The main components of such a structure are described in more detail in the following:

- Input data sensing interface system, i.e., lock-in amplifier (LIA) sensor system, performs the input sensing data through amplification, filtering, linearization, and demodulation process.

- Driving amplifiers with low distortion and strong capacitive driving ability are required to drive high-resolution (>16-bit) analog-to-digital converters (ADCs),

- Noise shaping successive approximation ADC (NS SAR-ADC) has the characteristics of a SAR ADC in terms of low power consumption and considerable potential to achieve high precision, like sigma-delta ADC.

- Low noise, high-resolution BGR, The voltage reference is essential for the proposed analog interface design, which relies on voltage references with low-temperature coefficient (T.C.) and high-power supply rejection ratio (PSRR). Moreover, high line/load regulation, low noise, and robustness against the impact of fabrication process effects are also highly desired.

- High-performance LDOs design, The high-speed low-dropout regulator is an essential on-chip power management solution for mobile and battery-operated devices requiring a clean supply voltage and a small CMOS area.

1.5 THESIS CONTRIBUTION

This thesis proposes analog front-end sensor interface primary circuit building blocks designed for biomedical applications or smart sensors within wireless sensor networks (WSN) . The thesis contribution extends across four published journals, where the first one [A] proposes Lock-In Amplifier for Sensor Application Using Second Order Harmonic Frequency With Automatic Background Phase Calibration. While the second [B] proposes A 14.5-Bit ENOB, 10MS/s SAR-ADC With 2nd Order Hybrid Passive-Active Resonator Noise Shaping. The third [C] proposes A High Bandwidth-Power Efficiency, Low THD2,3 Driver Amplifier with Dual-Loop Active Frequency Compensation for High-Speed Applications. The fourth one [D] Low noise, High PSRR, High-order piecewise curvature compensated CMOS Bandgap Reference. The contributions within each of the four works are listed in well-defined chapters 2-6 as follows:

- Lock-In Amplifier for Sensor Application Using Second Order Harmonic Frequency With Automatic Background Phase Calibration is presented in chapter 2.

- A 14.5-Bit ENOB, 10MS/s SAR-ADC With 2nd Order Hybrid Passive-Active Resonator Noise Shaping is presented in chapter 3.

- A High Bandwidth-Power Efficiency, Low THD[2,3] Driver Amplifier with Dual-Loop Active Frequency Compensation for High-Speed Applications is presented in chapter 4.

- Low noise, High PSRR, and High-order piecewise curvature compensated CMOS Bandgap Reference is presented in chapter 5.

- An Ultra-High-Speed, Wide Dynamic Range LDO Using Piecewise Speed Enhancement is presented in chapter 6.

An abstract of each thesis chapter's problem statement and contribution is presented. As such, the specific objectives of this thesis are written as follows:

1. For the analog front-end sensors to achieve high sensitivity and high integration, An analog lock-in amplifier (LIA) designed to be used in portable sensing applications for high-resolution signal recovery is presented. This work explores an alternative implementation of an analog LIA. Lock-in amplifiers (LIAs) are specialized amplifiers based on second harmonic detection that measure small signals' amplitude and/or phase at a known frequency f_0 and reject unwanted signals, even in noisy environments.

[A] X. Fu, D. M. Colombo, H. H. Alamdari, Y. Yin and K. El-Sankary, "Lock-In Amplifier for Sensor Application Using Second Order Harmonic Frequency With Automatic Background Phase Calibration," in IEEE Sensors Journal, vol. 22, no. 16, pp. 16067-16080, 15 Aug.15, 2022, doi: 10.1109/JSEN.2022.3191128.

2. A low-power, passive-active, second-order NS-SAR ADC designed to overcome the high-resolution and process scalability challenges. In the past decade, Noise-Shaping SAR (NS-SAR) has emerged as one of the most promising hybrid architectures. SAR and DSM architectures are combined in NS-SAR to provide both advantages: NS SAR-ADC has low power consumption and low cost similar to SAR-ADC and offers a high SNR similar to conventional DSM. In addition, the NS-SAR process is highly scalable, which makes it an attractive option for long-term development.

[B] X. Fu and K. El-Sankary, "A 14.5-Bit ENOB, 10MS/s SAR-ADC With 2nd Order Hybrid Passive-Active Resonator Noise Shaping," in IEEE Access, vol. 10, pp. 54589-54598, 2022, doi: 10.1109/ACCESS.2022.3176359.

3. To overcome the distortion barrier within the sensor node, a driver amplifier with high bandwidth-power efficiency, high capacitor-driving capacity, and low total harmonic distortion (THD). One complementary differential pair composed of self-cascode transistors is incorporated to obtain a full input voltage swing. Flipped voltage follower (FVF) buffers are applied as the second stage to drive the last class-AB output stage. Moreover, a dual-loop active-feedback frequency compensation (DLAFC) is presented, which can stabilize the proposed multistage amplifier and keep the dominant pole on high frequency to obtain high-frequency total harmonic distortion (THD) suppression.

[C] Fu, X.; El-Sankary, K.; Yin, Y. A High Bandwidth-Power Efficiency, Low THD[2,3] Driver Amplifier with Dual-Loop Active Frequency Compensation for High-Speed Applications. *Electronics* 2021, *10*, 2311. https://doi.org/10.3390/electronics10182311

4. Bandgap reference (BGR) circuits equipped with a new curvature compensation technique and a low dropout (LDO) regulator that can operate at high speed and with a wide dynamic range are proposed in this thesis. We are able to improve the power supply rejection ratio (PSRR) and line regulation performance while maintaining reference voltage PVT insensitivity and strong supply noise suppression. An LDO regulator is typically used to translate voltage levels or provide a stable output voltage, which has been considered an essential component in the power management of sensors and high-performance data converters. The sensors are very sensitive to the noise present in the power supply. Additionally, when switching DC-DC converters to step down voltage from the main supply, LDOs are frequently employed as post-regulators to suppress voltage ripples. Low dropout voltage regulators are used in most sensitive circuit applications to provide a regulated power supply.

[D] X. Fu, D. M. Colombo, Y. Yin and K. El-Sankary, "Low noise, High PSRR, High-order piecewise curvature compensated CMOS Bandgap Reference," in IEEE Access, 2022, doi: 10.1109/ACCESS.2022.3215544.

1.6 THESIS OUTLINE

This thesis is organized as follows. Chapter 2 introduces a fully integrated single-channel, analog LIA to reduce power consumption and the size of passive components by taking advantage of a new signal power detection scheme based on 2nd order harmonic extraction and automatic phase alignment technique. A comprehensive review of the various LIA architectures from the literature and their corresponding performance limitations is presented. Next, chapter 3 proposes A 14.5-Bit ENOB, 10MS/s SAR-ADC With 2nd Order Hybrid Passive-Active Resonator Noise Shaping. While the conventional SAR-ADC has low power consumption and a small area, the comparator's noise and offset, quantization noise, and complimentary DAC (CDAC) thermal noise limit its accuracy. On the other hand, the sigma-delta ADC is the most used structure to achieve high precision, but due to the need for many opamps in this structure, its power consumption is high, and the area is large. The NS-SAR ADC structure is a hybrid SAR-ADC and sigma-delta modulator (SDM) that inherits both advantages. Chapter 4 A High Bandwidth-Power Efficiency, Low THD[2,3] Driver Amplifier with Dual-Loop Active Frequency Compensation for High-Speed Applications. the proposed amplifier will result in high gain-bandwidth products (GBW), high total harmonic distortion (THD) suppression and fast settling time. An Ultra-High-Speed, Wide

Dynamic Range LDO Using Piecewise Speed Enhancement is presented in chapter 6. This paper presents an ultra-high-speed, wide dynamic range, low dropout (LDO) regulator that is used in applications for high-speed digital Systems on Chips (SoCs). The piecewise speed improvement is employed in the proposed LDO to ensure ultra-high-speed operation, which divides the LDO loop dynamics into three phases. Finally, the conclusion is presented in chapter 7, which also includes suggestions for future research work.

CHAPTER 2 LOCK-IN AMPLIFIER FOR SENSOR APPLICATION USING 2ND ORDER HARMONIC FREQUENCY WITH AUTOMATIC BACKGROUND PHASE CALIBRATION

Ximing Fu[1], Dalton M. Colombo[2], Hamed Hanafi Alamdari[1,4], Yadong Yin[3], and Kamal El-Sankary[1], Senior Member, IEEE

[1]Electrical and Computer Engineering, Dalhousie University, Halifax, Nova Scotia, Canada
[2]Electrical Engineering Department, Federal University of Minas Gerais, Belo Horizonte, Brazil
[3]School of Physics and Information Engineering, Fuzhou University, Fujian, China
[4]NovaResp Technologies Inc, Halifax, NS, Canada

ABSTRACT

An integrated lock-in amplifier (LIA) with automatic phase tuning and second-order harmonic frequency extraction is presented in this paper. The automatic phase alignment loop implemented in the proposed single-channel LIA can directly align the phases of an input signal with a reference signal. Furthermore, the proposed LIA system also includes an enhanced signal detection method in which the 2nd harmonics of the carrier frequency (ω_{ref}) is applied. As opposed to conventional LIA, this method reduces flicker noise and input offset effects that limit the signal-to-noise ratio (SNR). In terms of signal power detection, the proposed single-channel LIA architecture does not require phase synchronization between input and reference signals. The circuit is designed for a reference frequency of 100 Hz, suitable for biomedical applications. The LIA is implemented using 0.18-μm CMOS technology with a single power supply voltage of 1.8 V. The system consumes 360 μW at an operating frequency of 100 Hz and presents a high input sensitivity dynamic range for a detection bandwidth of 50 Hz and a FOM of 55.4 nW/Hz.

2.1 INTRODUCTION

One of the most common techniques to reduce drift and offsets in front-end sensor design is signal modulation and demodulation. Coherent detection is a powerful approach that can be used to detect weak signals buried under ambient noise and disturbing signals [1]. The essence behind this significant advantage is the fact that coherent detection is only sensitive within a small bandwidth around the operating frequency (ω_{ref}) and hence it can suppress the out-of-band signals [2]. Receivers based on coherent detection can achieve very low bandwidth and are independent of the operating frequency. As a typical low-frequency application, Lock-in Amplifier (LIA) has employed coherent detection techniques to achieve high sensitivity to detect weak signals buried under noise while achieving high dynamic reserve (maximum signal-to-noise ratio). The lock-in amplifiers are currently available as commercial products are unsuitable for portable instrumentation applications due to their cost, bulkiness, and excessive power usage [3]-[5].
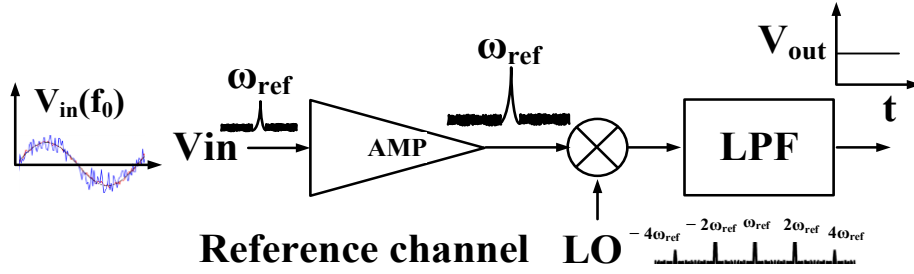
Fig. 2.1. Block diagram of a conventional single-phase LIA.
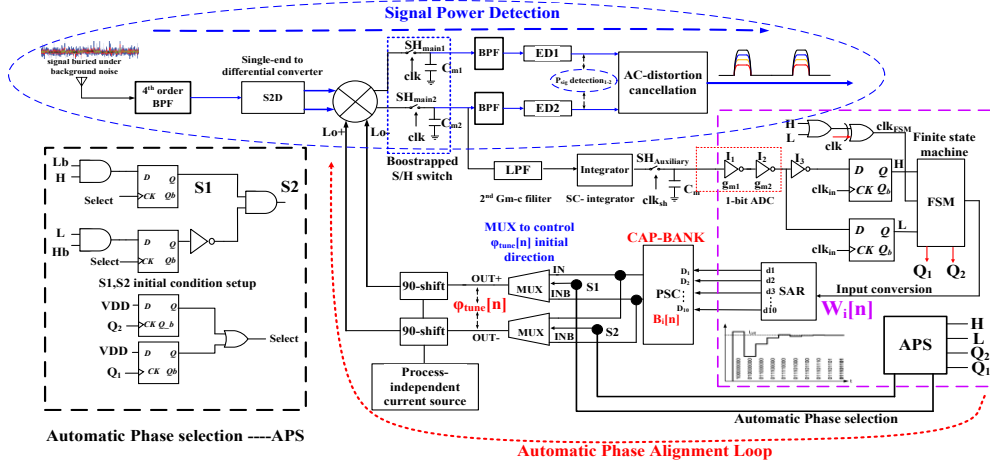
Fig. 2.2. Block diagram of the proposed integrated LIA with semi-digital phase alignment architecture.

Most integrated LIAs in the literature exhibit high-power consumption in milliwatts [6–9]; Consequently, it is difficult to be compatible with mobile devices or other electronics. There is, therefore, a growing need for integrated low-power (i.e., μW) LIAs enabling new innovative applications, such as respiratory system monitoring and impedance measurement [10-11].

As shown in Fig. 2.1, the conventional LIA consists of a front-end instrumentation amplifier, a mixer, and a low pass filter (LPF). In conventional LIAs, the output is represented by a DC signal that is passed through the correlator (mixer) and demodulated by the LPF. The weak signal buried under the ambient noise is generally pre-amplified using an instrumentation amplifier to increase further the signal-to-noise ratio (SNR). The mixer, acting as a correlator, performs the multiplication between the input signal frequency (ω_{ref}) and reference signal of the same frequency. The mixer's output representing the harmonic content of the LO will be filtered by a low-pass filter (LPF), resulting in a DC voltage which is the amplitude linearly proportional to the desired signal. The fundamental challenge in this single channel-based LIA scheme is that it

17

necessitates highly accurate phase adjustments between the reference and incoming signals to ensure maximum sensitivity.

Recent technique to achieve precise phase alignment using voltage control signal and switches [3] results in an excessive error. It prevents retrieving the input signal properly due to the lack of a negative feedback loop mechanism to track the output signal and adjust the phase difference relative to the reference signal. Alternatively, dual-phase lock-in amplifiers can extract the signal amplitude independently, regardless of phase shift [4]-[7]. This system's internal feedback scheme comprises a phase-sensitive detection (PSD) channel and a 90° phase shift channel. The phase-matching circuits are not required for this type of detection since they utilize the I/Q signal detections. This solution doubles area and power consumption and requires the use of highly specialized and complex analog and digital circuits to overcome the phase error. An on-chip LIA featuring automatic phase alignment between the reference signal and the input signal is presented in [8]. The system estimates and calibrates the carrier phase based on the sum of I/Q channel vectors. In this case, operational transconductance amplifiers (OTAs) and passive components were employed, which resulted in relatively high-power consumption and area consumption, especially for applications involving low frequencies.

Many internal and external noises affect the LIA system's SNR, including ambient noise, flicker noise, shot noise, and thermal noise [12-14]. Consequently, the Lock-in amplifier requires a front-end detection system that minimizes the impact of multiple noise sources. Previous works that used a shunt resistor and a band-pass filter (BPF) showed that a modulation technique could be employed to detect the current signal generated by an optical sensor [15]. However, it has a specific limitation when detecting weak signals due to the minimal gain and slow transient response.

This paper proposes a fully integrated single-channel, analog LIA to reduce power consumption and the size of passive components by taking advantage of a new signal power detection scheme based on 2nd order harmonic extraction and automatic phase alignment technique. The proposed LIA utilizes $2\omega_c$ Harmonic instead of DC signal to improve the transient response of the LIA and overcome the 1/f flicker noise limitation with a built-in chopping technique to improve the SNR of the entire system. The automatic phase tuning mechanism for phase alignment between the reference and input signals is also proposed. The paper is organized as follows: the overall LIA system architecture and its operation principle are discussed in section II, while the complete design of the LIA is described in detail in section III. Section IV presents the experimental performance, and section V concludes the paper.

2.2 FUNDMATAL THEORY ANALYSIS AND DESIGN CONSIDERATIONS OF THE PROPOSED LIA

2.2.1 SYSTEM-LEVEL SNR CONSIDERATIONS

For lock-in amplifiers, in addition to the sensitivity, linearity, and resolution, the most used design specifications are described in Table 2.1:
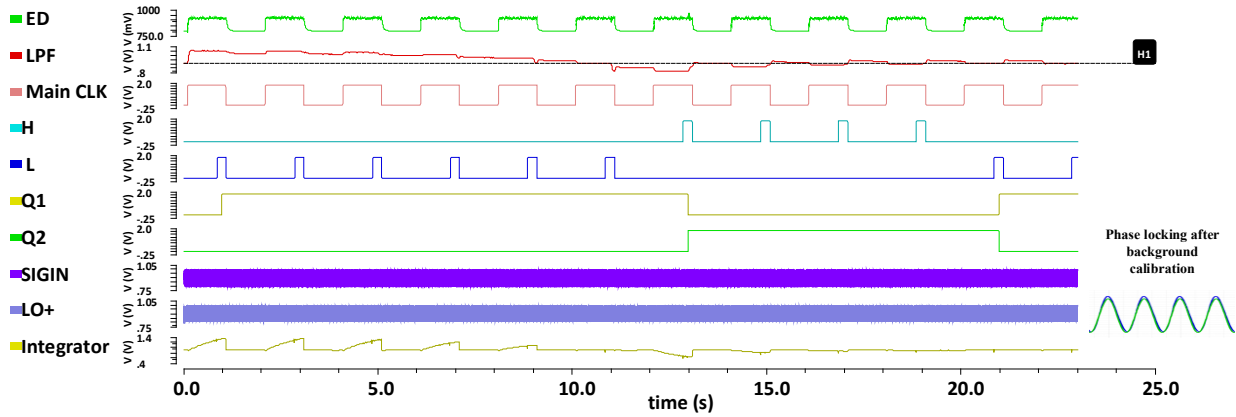
Fig. 2.3. Circuits level Simulation of proposed custom integrated LIA with 2nd order harmonic power extraction & automatic phase alignment architecture

(a)

19
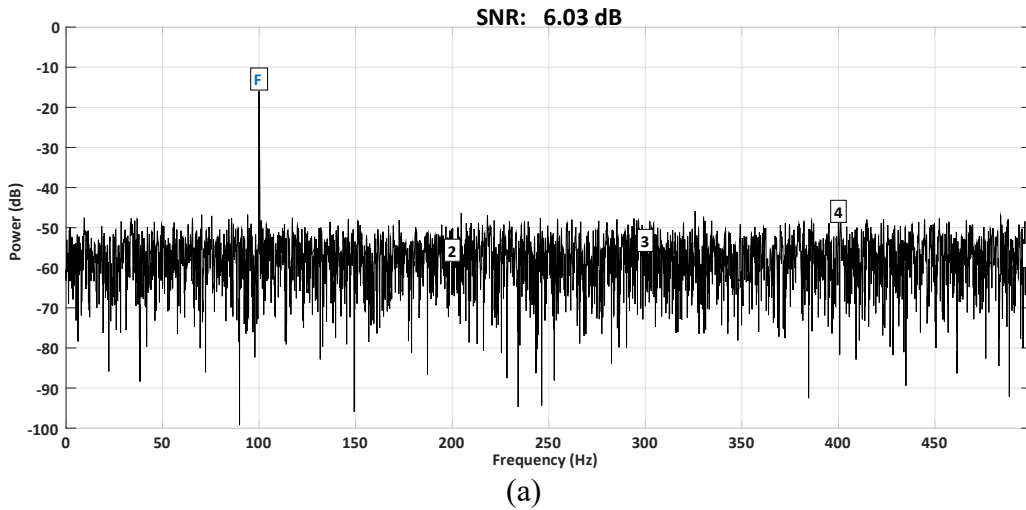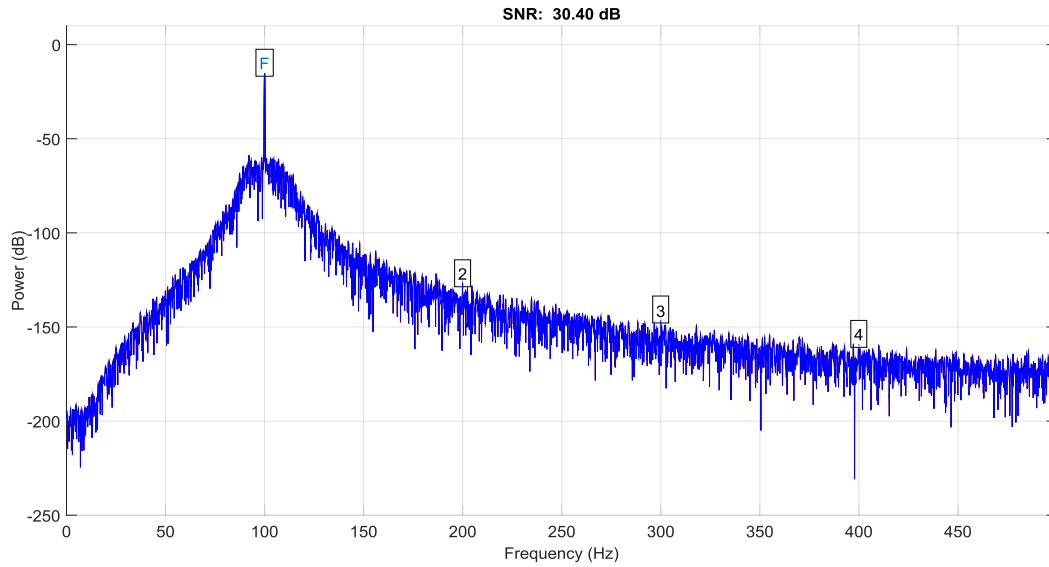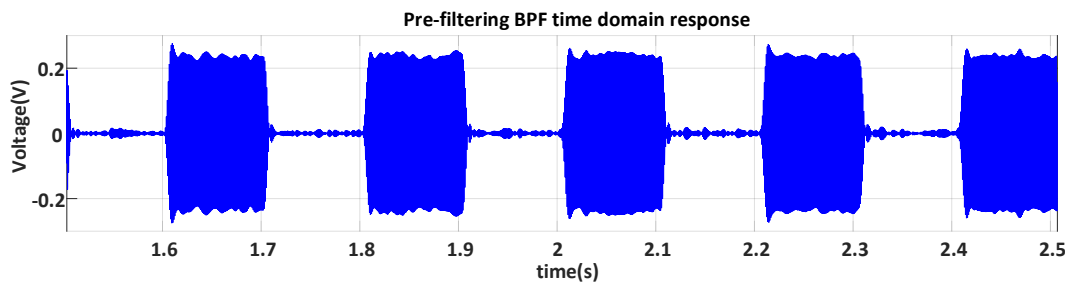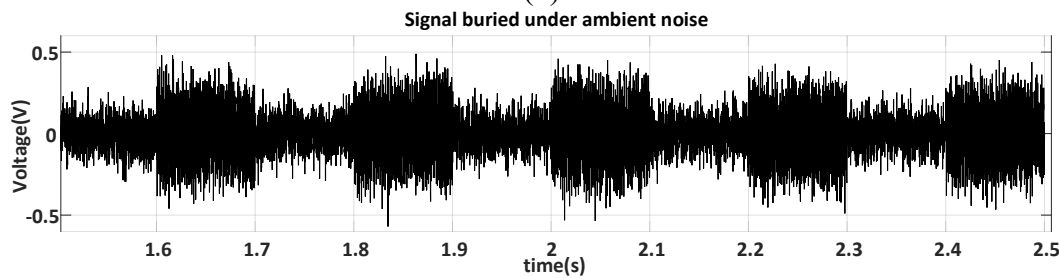
Fig. 2.4 (a) SNR for input signal buried under the noise without filtering (b) SNR improvement for input signal though BPF prefiltering (c) time-domain response with BPF filtering characteristic

TABLE 2.1
MAIN DESIGN SPECIFICATIONS OF THE LOCK-IN AMPLIFIER

Parameters	FS	OVL	MDS	IDR	ODR	DR
Definitions	$\dfrac{V_{sat}}{(A_{tot})}$	V_{nmax}	V_{smin}	$20log\dfrac{OVL}{(MDS)}$	$20log\dfrac{FS}{(MDS)}$	$20log\dfrac{OVL}{(FS)}$
FS	Full-scale input level					
OVL	OverLoad					
MDS	Minimum discernible signal					
IDR	Input Dynamic Range					
ODR	Output Dynamic Range					
DR	Dynamic Reserve					
V_{sat}	Output swing when the LIA output is saturated					
A_{tot}	Total gain of the LIA signal chain					
V_{nmax}	Maximum input noise voltage level that the system allows					
V_{smin}	The minimum input signal recognized on the output can be interpreted as the resolution of the system					

The main objective of the LIA is to improve the SNR of a weak signal that is typically buried under considerable ambient noise. In most instrumentation applications, analog signals always require a filtering process. The commonly used noise suppression filters are low-pass (LPF) and a band-pass filter (BPF). In conventional LIA design, the LPF can effectively suppress high-frequency noise and is often used to recover the desired low-frequency or DC signals. Unfortunately, for low-frequency noise (such as 1/f noise, offset drift, and temperature drift), LPF cannot further improve the SNR without substantially increasing the order of the filter. Moreover, for LPF-based LIA to achieve the same SNR after demodulation, the cut-off frequency required is very narrow, substantially reducing the system's transient speed. The proposed LIA architecture implements a band-pass filtering front-end stage, unlike the traditional approach. Therefore, the noise power outside the passband of the BPF will be significantly attenuated. As a result, the input SNR is improved. The noise figure of the LIA can be written as:

$$NF = \frac{S_i/N_i}{S_o/N_o} = \sqrt{\frac{\Delta f_{No}}{\Delta f_{Ni}}} \tag{2-1}$$

Where S_i/N_i and S_o/N_o refers to the input/output signal-to-noise ratio. Δf_{Ni} and Δf_{No} are the system equivalent input/output noise bandwidth, respectively. To improve the input SNR and the

noise figure, it would be an appropriate choice to enhance the overload (OVL) signal and input Dynamic Range (IDR) (refer to Table 2.1).

Figure 2.4 (a) and (b) show a simulation of the SNR of the input signal buried under ambient noise with and without BPF filtering. As can be seen, the BPF filtering significantly improved the SNR. It is also evident from the time domain transient simulation in Fig.2.4 (c) that when the input signal is off, the prefiltered signal has drastic noise reduction. Assume the BPF has a passband $\omega_c \pm \pi B$. We can evaluate the output noise power spectrum density through ideal BPF as the following:

$$P_o(\omega) = n_0|H(\omega)|^2 = \begin{cases} A^2 n_0, & \omega_c - \pi B/2 < |\omega| < \omega_c + \pi B/2 \\ 0, & \text{elsewhere} \end{cases} \qquad (2\text{-}2)$$

The time-domain autocorrelation function, which corresponds to the inverse Fourier transform of the output noise power spectrum density, can be written as:

$$R_o(\tau) = \frac{1}{2\pi} \left[\int_{-\omega_c - \Delta\omega/2}^{-\omega_c + \Delta\omega/2} 2A^2 n_0 e^{j\omega\tau} d\omega + \int_{\omega_c - \Delta\omega/2}^{\omega_c + \Delta\omega/2} 2A^2 n_0 e^{j\omega\tau} d\omega \right]$$

$$(2\text{-}3)$$

with $H(\omega) = G\left(\frac{\omega}{B}\right) * (\delta(\omega + \omega_c) + \delta(\omega - \omega_c))$

$$R_o(\tau) = \frac{1}{2\pi} \left[\int_{\omega_c - \Delta\omega/2}^{\omega_c + \Delta\omega/2} A^2 n_0 \cos(\omega\tau) d\omega = \frac{A^2 n_0 \Delta\omega}{2\pi} \sin\left(\frac{\Delta\omega\tau/2}{\Delta\omega\tau/2}\right) \cos(\omega_c \tau) \right.$$

$$= A^2 n_0 B Sa(\pi B\tau) \cos(\omega_c \tau) \qquad (2\text{-}4)$$

where $Sa(x) = \frac{\sin(x)}{x}$, $G\left(\frac{\omega}{B}\right)$ is the Fourier transform of a rectangular signal with bandwidth B. Therefore, the average output noise power spectral density will be

$$R_o(0) = A^2 n_0 B \qquad (2\text{-}5)$$

(a)

22

SNR: 42.36 dB
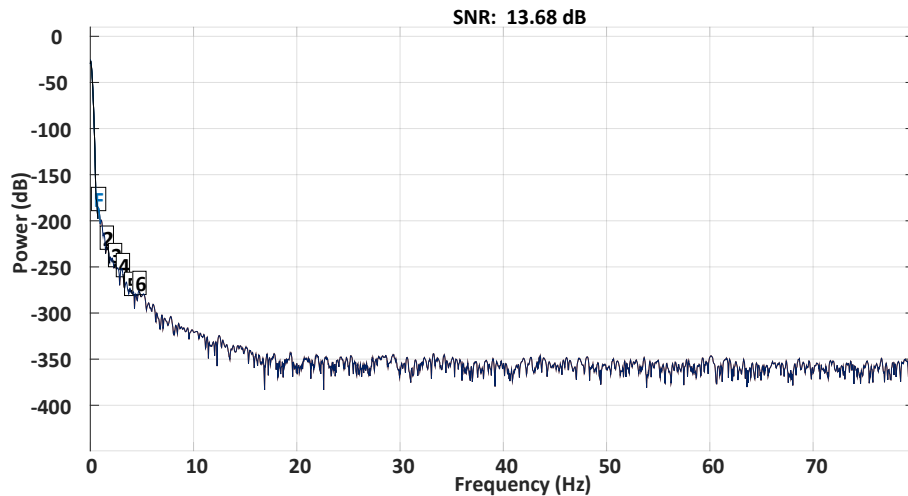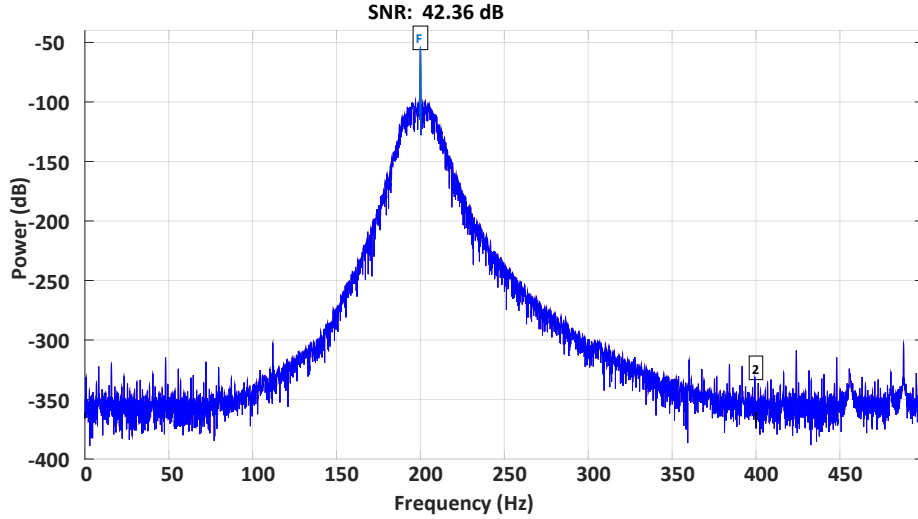
(b)

Fig. 2.5 System-level comparison between (a) conventional LIA utilizing DC-based LPF demodulation scheme without prefiltering, (b) SNR improvement for the proposed LIA with BPF-prefiltering & 2nd order harmonic extraction-based demodulation stage.

The overload level OVL of the LIA is defined as the input voltage level being overloaded or critically overloaded due to the excessive noise beyond the overload level. Hence, the system will cause nonlinear distortion. To prevent noise peaks from overloading the LIA and causing nonlinear distortion, the front-end BPF is essential to improve the Minimum Discernible Signal（MDS）of the LIA.

Fig. 2.5 shows the final system-level simulation comparison between a conventional LIA based on the DC-LPF demodulation method without BPF-prefiltering and the designed LIA with BPF-prefiltering. The SNR of the LIA system has been significantly improved, and, more importantly, the proposed LIA will have significant improvement in transient speed advantages due to the 2nd order harmonic extraction demodulation method.

2.2.2 SEMI-DIGITAL LIA ARCHITECTURE

The block diagram of the proposed LIA and its circuit-level simulation results are shown in Figures 2.2 and 2.3, respectively. The fundamental principle of operation relies on two independent loops. Namely the *signal power detection path* and the *automatic phase alignment loop*. The input signal power detection is based on 2nd order harmonic $(2\omega_c)$ instead of a DC signal. Moreover, the

proposed phase aligning peripheral loop is used to align the input signal phase relative to the reference signal by tuning the phase calibration coefficients $\sum_{i=1}^{10} B_i[n]$ (in Fig. 2.2) until the input signal and local reference signal are phase-locked. Therefore, the phase information of the input signal can be retrieved. Fig. 2.3 shows the entire system circuits level simulation with key signals labeled in the graph.
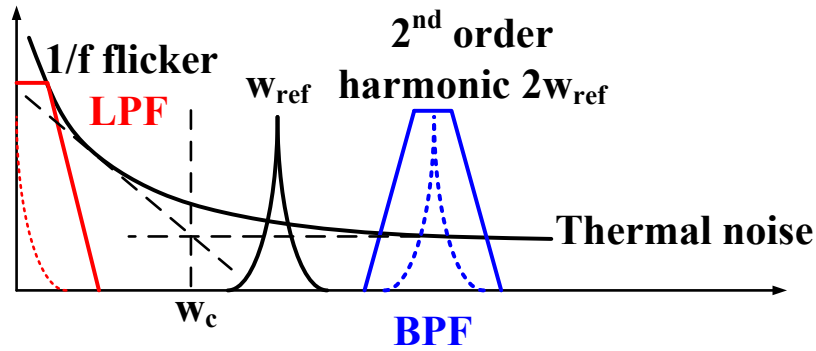
Fig. 2.6 Signal and noise distribution in a lock-in detection system
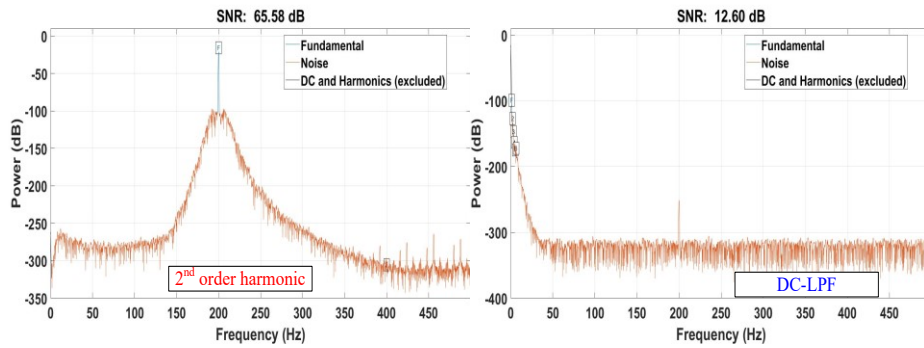
Fig. 2.7 SNR comparison between 2nd order harmonic power detection and DC-based LPF (compared under (1) same flicker noise & white Gaussian noise. (2) same output power)
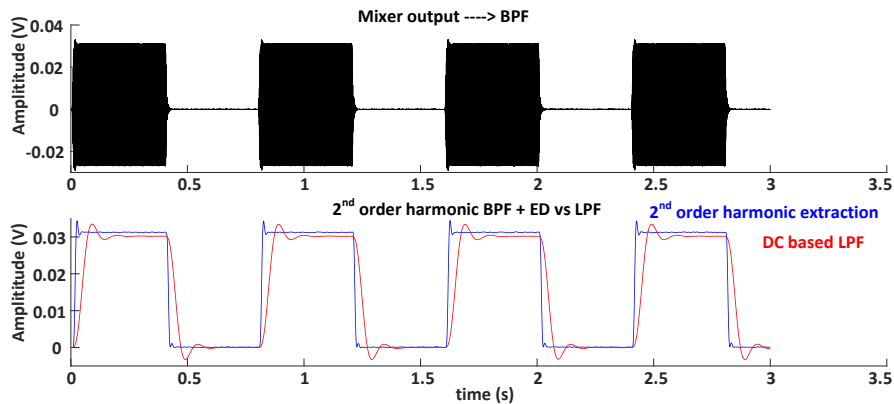
Fig. 2.8 transient speed advantage between 2nd order harmonic signal power detection vs. DC-LPF compared under same SNR

The *signal power detection (SPD) path* operates as follows. The input voltage signal is prefiltered with a BPF to attenuate unwanted harmonics and increase SNR. A single-ended-to-differential converter (S2D) is applied to generate fully differential voltage for the mixer. The output of the S2D is then fed into a phase-sensitive detector (PSD) (e.g., an active mixer). A bootstrapped S/H is adopted to quench the mixer output in the time domain to reduce power consumption for the proposed LIA. Quenching operation for the proposed LIA is allowed because of the significant transient speed improvement from the subsequent 2nd order harmonic extraction stage. The harmonic extraction stage is implemented as an envelope detector (ED) with AC variations cancellation.

The *automatic phase alignment (APA) loop* operation is described next. Before that, it is worth noting that *SPD* path is not influencing the *APA* loop, and concurrent operation between both loops can be achieved; hence, the transient speed is improved. The output of the PSD will pass through the LPF to only differentiate the phase error ($\theta_{error} = \theta_{sig} - \theta_{ref}$) between the input signal and reference signal. The phase error (θ_{error}) is converted back into the voltage domain and integrated by switched capacitor-based integrator used as phase error amplification before the digital calibration algorithm. The digital calibration circuits, including an inverter-based comparator, a finite state machine (FSM), a successive approximation register (SAR), a phase shifter, and an automatic phase selection MUX, help the LIA control system to tune the feedback phase to track that of the input signal. Finally, the phase information of the input signal will also be extracted after a few calibration cycles of the signal detection.

2.2.3 ADVANTAGES OF 2ND ORDER HARMONIC EXTRACTION

From the noise perspective, the first stage of the sensing amplifier is the dominant noise contributor, and it is challenging to have significant noise reduction for low-frequency applications. In applications that require the detection of weak signals, the key issue is to minimize the observation noise introduced during the measurement process. Typically, the low-noise preamplifier is the first stage of the LIA, which amplifies the signal's power. It is essential that the preamplifier has a low noise performance. As a result, the preamplifier's noise will bury the signal under the noise, making the effect even more pronounced.

Conventionally, the dominant flicker (1/f) noise in an amplifier is removed using the chopping technique with the modulator placed before the gate of the input pair and the demodulator at the output of the OTA [22]. The 2nd order harmonic extraction method works similarly to the chopping technique, effectively avoiding the influence of large flicker noise in the DC frequency domain. The 1/f flicker noise power spectrum density $S_{vflicker}(f)$ can be approximated as:

$$S_{vflicker}(f) = A^2 K_F I_{DC}^\gamma / f^\beta \, \text{Hz} \tag{2-7}$$

Where K_F, α, and β are constants particular to each device's <u>fabrication</u> technology, and I_{DC} is the DC current through the device. f is the frequency, the parameter A is determined by the technology characteristic, and $\gamma \approx \beta \approx 1$. Therefore, the output noise mean square voltage ($E_{nflicker}$) can be written as:

$$E_{nflicker} = K_F \sqrt{ln(f_2 - f_1)} \tag{2-8}$$

Equation (2-8) shows that the flicker noise decreases as the frequency increases. If the proposed technique is employed, the 1/f flicker noise impact on the LIA circuit will be much smaller. Figures 6 and 7 show the power spectrum of a general LIA system. For the proposed topology, the BPF filter detects the signal of interest and reduces the influence of the 1/f noise, thus enlarging the minimum detectable range and improving the SNR. Figure 2.7 shows a comparison between the conventional and the proposed approach for given signal power and the same noise input applied.

Figure 2.8 shows the transient speed advantage of the proposed 2nd order harmonic signal power detection technique that will allow faster processing, thus reducing the chip area (no need for large area LPF) and providing precise signal extraction.

LPF in traditional LIA architectures is usually implemented by an Opamp-based integrator. The time constant (τ_{LPF}) of the integrator determines the equivalent noise bandwidth of LIA and the SNR improvement. The larger the time constant of the integrator, the narrower the equivalent noise bandwidth, and the larger the SNR. However, the longer the measurement time required, the lower the transient speed - a drawback for several applications. Consider that input and reference signals are given by (2-9) and (2-10). The output signal of the PSD ideally has both the DC term and 2nd order harmonic of the input signal by ideal mixer operation.

$$V_{sig\,=\,} A_{sig}\, cos(\omega_c\, t + \theta_{sig}\,), V_{ref\,=\,} A_{ref}\, cos(\omega_c\, t + \theta_{ref}\,) \qquad (2\text{-}9)$$
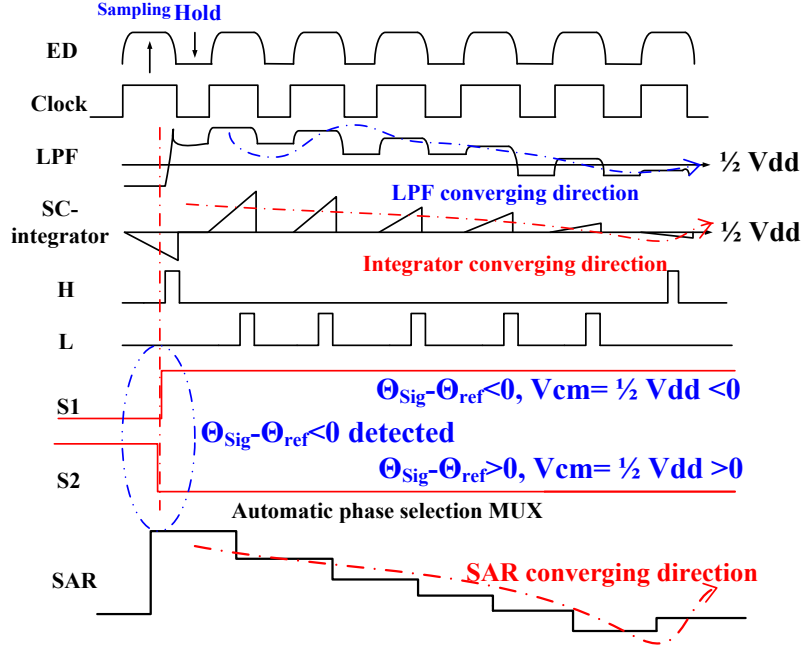
Fig. 2.9 Proposed custom phase alignment circuits timing diagram.

$$V_{mix\,=\,} A_{sig}\, cos(\omega_c\, t + \theta_{sig}\,) * A_{ref}\, cos(\omega_c\, t + \theta_{ref}\,) \qquad (2\text{-}10)$$

When $\theta_{sig}\,\neq\theta_{ref}$

$$V_{mix\,=\,} 0.5 * A_{sig}\, A_{ref}\, (\, cos(\theta_{sig}\, - \theta_{ref}\,) \, + \, cos(2\omega_c\, t + \theta_{sig}\, + \theta_{ref}\,) \qquad (2\text{-}11)$$

When $\theta_{sig}\,=\theta_{ref}$

$$V_{mix\,=\,} 0.5 * A_{sig}\, A_{ref}\, + 0.5 * cos(2\omega_c\, t + \theta_{sig}\, + \theta_{ref}\,) \qquad (2\text{-}12)$$

In the proposed APA loop in the LIA system, the feedback phase compensation from the phase shifter circuits is shifted by 90°. Thus, (2-11) can be rewritten as the following:

$$V_{mix\,=\,} 0.5 * A_{sig}\, A_{ref}\, (\, sin(\theta_{sig}\, - \theta_{ref}\,) \, + \, sin(2\omega_c\, t + \theta_{sig}\, + \theta_{ref}\,) \qquad (2\text{-}13)$$

where $2\omega_c$ is the 2nd order harmonic frequency of the input signal. If the phase difference between the input and reference signal is zero, the PSD output can be expressed as in (2-13) with a precise known DC value (namely, common-mode level $V_{cm} = \frac{V_{dd}}{2}$) without being affected by the phase error.

An LPF is used to detect weak signals by obtaining the DC signal under phase match conditions in a conventional LIA system. Equations (2-11)-(2-13) demonstrate that the DC output signal varies when the phase difference is not zero. Therefore, the proposed automatic phase alignment loop is essential in a single channel LIA to allow proper signal extraction. The system complexity increases significantly for a dual-channel LIA that can calculate the vector sum of the I and Q channels. The system becomes more complex when memory elements are necessarily required to digitize the input signal and compute the vector sum. Additionally, the modulation/demodulation nature of the proposed SPD path can significantly improve the SNR if we use the harmonic frequency ($2\omega_c$). This idea is technically a simplified solution compared with the chopping technique.

However, two significant challenges must be addressed and solved to implement 2nd order harmonic extraction at the circuits level:

(i) designing the BPF in the low-frequency domain without sacrificing area is very challenging. To effectively extract the signal power of $2\omega_c$, an RF energy harvesting on-chip rectifier was designed to behave as a signal power extraction element with AC variations cancellation. Since the 2nd order harmonic term is a purely sinusoidal wave independent with phase mismatch, RF down to DC converter will extract the envelope of the $2\omega_c$ and a differential source follower will cancel the differential signal leakage.

(ii) The PSD used in the proposed LIA is designed using an analog active mixer. An active mixer as an analog multiplier will ideally have no harmonics other than $2\omega_c$. PSDs based on switching mixers, such as single and double-balanced mixers [21-22], can produce multiple other harmonic signals. Moreover, such switch mixers are extremely sensitive to phase-matching and thus inhibit the ability to detect harmonic signals.

2.2.4 AUTOMATIC PHASE ALIGNMENT LOOP OPERATING PRINCIPLE

The timing diagram of the proposed APA loop operating principle is shown in Fig. 2.9. The proposed phase tuning scheme is based on a negative feedback loop to automatically tune the phase shift of the phase shifter to achieve automatic phase alignment. The proposed LPF based on a linear G_m-attenuated network is applied to achieve good linearity of the LIA and transfer $\theta_{error} = \theta_{sig} - \theta_{ref}$ into the SC-integrator to amplify the deviations and average out the random noise in the time domain. A PVT (Process, Voltage, Temperature) compensated inverter-based comparator is utilized to precisely detect the previous phase error and transfer "1" or "0" to the following FSM and SAR controller.

The phase shift circuits behave as an all-pass filter and comprise 10-bit capacitor bank elements. The outputs of the phase shifter circuits can provide $\pm 2\pi$ phase shift difference. The phase shifter can be understood as a digitally controlled phase interpolator that generates the compensation phase $\psi_{tune}[n]$ (Fig. 2.2). Digital controlling words (d_{1-10}) are translated by the phase shifter from the LPF and SC integrator combination through the FSM into an analog phase. The phase shifter generates N quantized phase steps between the phase angles ψ_{tune} [n] to ψ_{tune} [n+1]. The phase deviation $\Delta[n]$ is extracted by the LPF+SC integrator. $\Delta[n]$ is used to update the weighting coefficients $W_i[n]$ implemented within the inverter-based comparator, FSM, SAR, and the CAP-bank (Fig.2.2) to generate and tune the phase compensation $\psi_{tune}[n]$ during the calibration. The proposed technique recursively updates the weight coefficients:

$$W_i[n + 1] = W_i[n] + \mu\Delta[n] \tag{2-14}$$

where μ is the adapting coefficient and $\mu\Delta[n]$ is proportional to the dynamic error signal (deviation function) in each estimation period. When $\Delta[n]$ between the two consecutive estimation periods approaches 0, the updated weighting coefficients $W_i[n]$ will converge to constant values. This will, in turn, lead the compensation phase $\psi_{tune}[n]$ of the phase shifter to converge to its optimal value since:

$$|W_i[n+1] - W_i[n]| = |\psi_{tune}[n+1] - \psi_{tune}[n]| \approx 0 \qquad (2\text{-}15)$$

The phase compensation, including the calibrated phase shift, is given by:

$$\psi_{tune}[n+1] = \psi_{tune}[n] + \psi_{initial} = \psi_{LSB}(\textstyle\sum_{i=1}^{10} B_i[n] * 2^i) + \psi_{initial} \qquad (2\text{-}16)$$

where ψ_{LSB} is the LSB value for capacitor bank, $\psi_{initial}$ is the original reference signal phase.

The output of the phase shifter is fed into the negative feedback loop through the mixer. By sending the mixer outputs to the LPF, we can obtain the low-frequency components of the demodulated signal and then filter out the higher-frequency components. This process continues until the reference signal is in phase with the input signal. The LPF and SC-integrator will converge to V_{cm} Hence, the input signal and reference signal will have a phase difference close to 0. Then, the input signal phase information can be calculated by the proposed automatic phase alignment loop.

2.3. ESSENTIAL BUILDING BLOCKS AND THEIR CUSTOM IMPLEMENTATION.

2.3.1 PSEUDO-RESISTOR-BASED BPF WITH PVT COMPENSATION
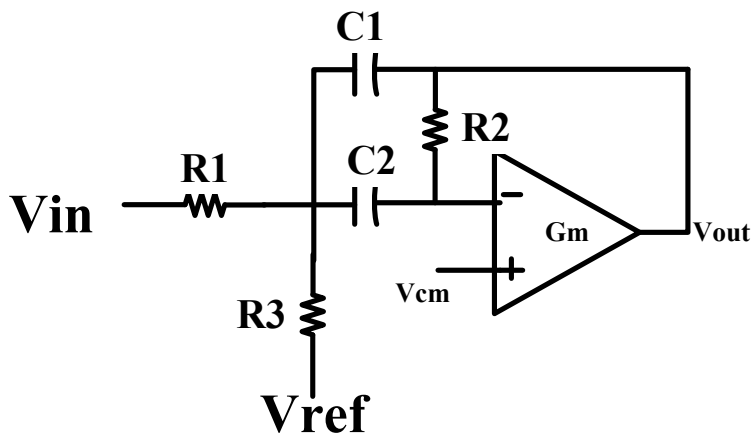
Fig. 2.10 (a) Multiple Feedback Topology Band-pass Filter (MFT-BPF)
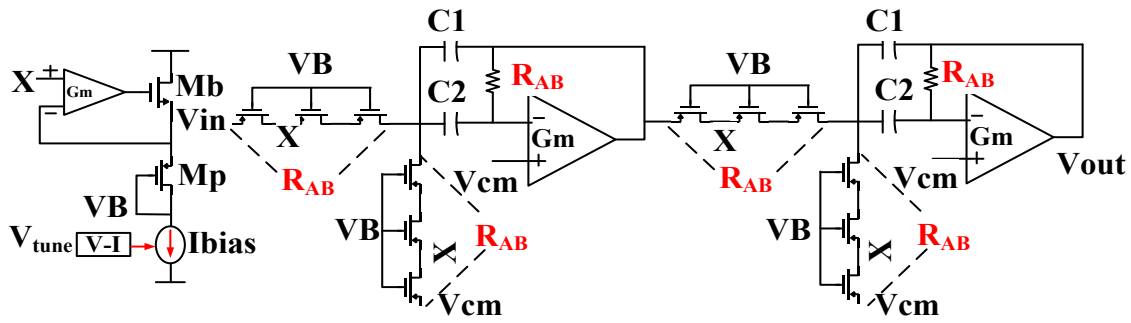
Fig. 2.10 (b) proposed PVT compensated biasing circuit for 4th order BPF
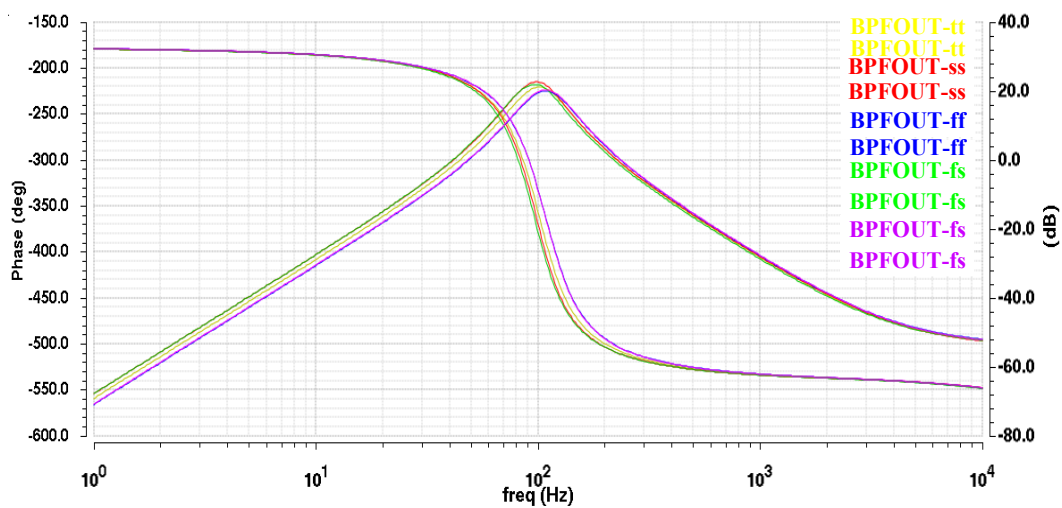
(a)
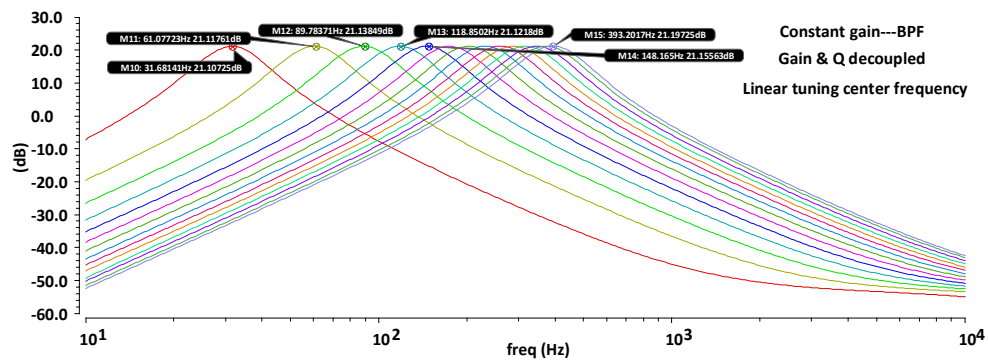
(b)

Fig. 2.11(a) proposed PVT compensated biasing 4th order BPF AC response (b) frequency response of the 4th-order filter with center frequency tuning from 30 Hz to 400Hz

The proposed LIA using the 4th order BPF in the front-end is responsible for prefiltering and attenuating any unwanted harmonics and ambient noise to increase SNR. As shown in Fig. 2.10, a pseudo resistor with a PVT compensated biasing scheme can improve performance against process variations. The use of a matched structure allows for achieving an order of magnitude better than conventional voltage biasing, as shown in the simulation results in Fig.2. 11(a). A process insensitive V–I converter [28] is employed to precisely control the tuning voltage V_{tune} to control the center frequency of the BPF, allowing the proposed SPD path to achieve higher SNR and harmonic filtering. Fig.2.11(b) also demonstrates the decoupling parameters between Gain, Q & f$_m$ of the 4th-order filter. This is because due to the synchronous tuning of PRs in the BPF, the quality factor Q and filter Gain are only related to the relative ratios of the resistors, which are process independent. The critical design parameters of Multi-feedback BPF can be written as the following:

$$H(s) = \frac{V_{out}}{V_{in}}(s) = -\frac{s\frac{1}{R_1 C}}{s^2 + s\frac{2}{R_2 C} + \frac{1}{R_2 C^2}(\frac{1}{R_1} + \frac{1}{R_3})} \tag{2-17a}$$

$$f_m = \frac{1}{2\pi}\sqrt{\frac{R_1 + R_3}{C_1 C_2 R_1 R_2 R_3}} \tag{2-17b}$$

When $C_1 = C_2$, Equation (2a) can be simplified as:

$$f_m = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} \tag{2-17c}$$

$$H(2\pi f_m) = A_m = -\frac{R_2}{2R_1} \tag{2-17d}$$

$$Q = \frac{f_m}{B} = f_m \pi R_2 C \tag{2-17e}$$

Where the filter's parameters are : f_m refers to the middle (center) frequency in Hz; A$_m$ is the gain at the middle frequency in V/V. B is the bandwidth between half-power frequencies in Hz. Q is the quality factor. The pseudo resistor with process compensation was designed to emulate a tunable resistor whose resistance can be set in the range 25MΩ – 1GΩ. The proposed biasing current I_{bias} operating in weak inversion can be written as:

$$I_{bias} \approx kI_o exp^{\frac{q}{nkT}(Vgs-Vth)} exp^{\frac{\delta Vds}{nVT}} \tag{2-18a}$$

$$V_{gs(Mp)} \approx V_{th} + \frac{nkT}{q} ln \frac{I_{bias}}{kI_o} \tag{2-18b}$$

$$r_{ds} = \frac{\partial Vds}{\partial I_{bias}} \approx \frac{1}{KI_o \, exp^{\frac{q}{nkT}(V_{gs(Mp)}-Vth)}\frac{\delta}{nVT}exp^{\frac{\delta Vds}{nVT}}} \tag{2-19}$$

$$R_{AB}(V_{AB}=0) \approx \frac{1}{KI_0\frac{\delta}{nVT}} exp^{-\frac{Vgs-Vth}{nVT}} \approx \frac{1}{KI_0\frac{\delta}{nVT}}(\frac{KI_o}{I_{bias}}) \tag{2-20}$$

where I_o is the specific current. $V_{gs(Mp)}$ is feedback voltage to the pseudo resistor voltage $V_{gs(PR)}$ to cancel the dependence of V_{th} on the pseudo resistor. Therefore, the pseudo resistor with the proposed biasing scheme will be ideally process-independent. Equations (2-18)-(2-20) show that the emulated resistance is inversely proportional to I_{bias}, which means a constant I_{bias} is very important to maintain the process independent relationship of the proposed pseudo resistor.

2.3.2 SECOND ORDER HARMONIC EXTRACTION USING TWO-STAGE INTER-STAGE VTH COMPENSATION RECTIFIER.
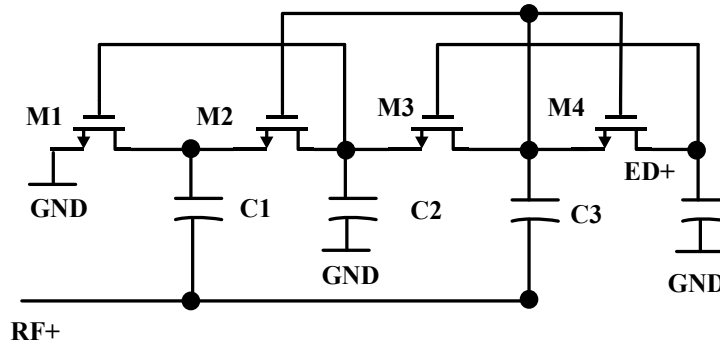
Fig. 2.12 A Two-stage inter-stage V_{TH} compensation rectifier.
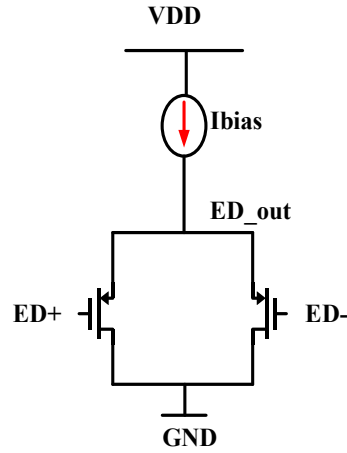
Fig. 2.13 A source follower-based AC cancellation circuits.
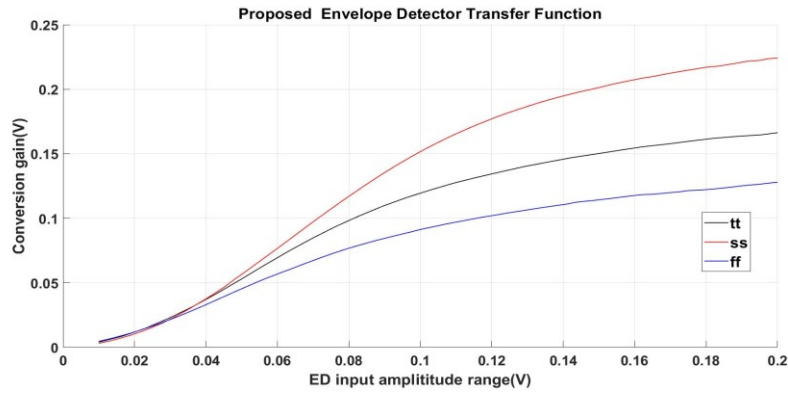
Fig. 2.14 RF-DC rectifier conversion gain

Based on (2-9)-(2-13), the signal power detection can be extracted from the envelope detector (ED) because the amplitude of the mixer output has a direct linear relationship with the ED variations. As shown in Figs.2.12 and 2.13, a two-stage RF to DC converter with AC leakage cancellation pseudo-BPF demodulation stage is adopted. Fig. 2.14 shows the conversion gain of the proposed ED under different process variations. For an envelope detector, the maximum output ripple V_r can be approximated as:

$$V_r = V_p(1 - exp^{\frac{-T}{\tau}}) \approx \frac{V_p}{f\tau} \tag{2-21}$$

where T refers to the period of the 2nd order harmonic frequency of the input signal, V_p voltage refers to the oscillation peak of the 2nd order harmonic signal, and τ refers to the designed time constant of the ED. The bypass capacitor removes the DC offset generated from the circuits before the signal amplitude detection. The RF-DC rectifier does not generate offset voltage. It is clearly shown in (21) that due to the increased frequency of the input signal, the time constant required of the ED is much smaller under the same ripple voltage, which enables a faster transient response under acceptable ripples. An inter-stage V_{TH} compensation scheme was introduced in [26-27]. The compensation was achieved by connecting the gate terminal to the post-stages, eliminating the large additional capacitors in the Inter Vth Cancellation (IVC). Meanwhile, the ac variations leakage of the from 2nd order harmonic detection will be canceled by differential source follower to allow precise power detection. NMOS transistors within deep n-well provide individual bulk biasing and reduce threshold voltage variation between different rectifier stages.

2.3.3 TRANSCONDUCTANCE REDUCTION TECHNIQUE FOR VERY LOW-FREQUENCY GM-C FILTERS
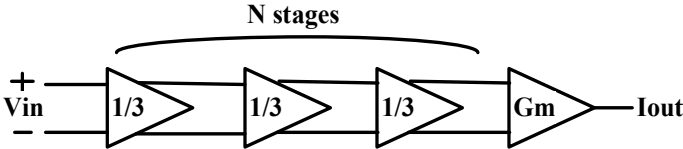
Fig 2.15. Low- Gm transconductor using voltage attenuation [147].
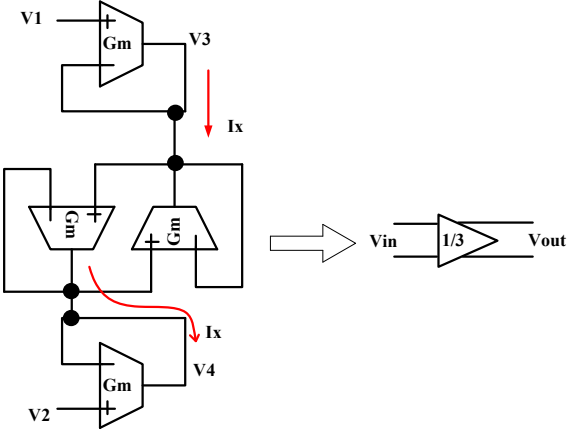
Fig 2.16. Nonlinear Gm network implementing a linear voltage attenuator [147].
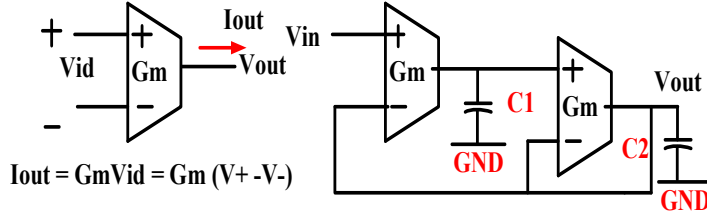
Fig 2.17. Gm attenuated network-based 2nd order Gm -c low pass filter

Fig. 2.15 shows the macro-model of the proposed transconductor. A cascading stage consists of 3-stages of 1/3 (one-third) linear attenuators and a normal G_m stage. Doing so will attenuate the input voltage Vin by a factor of 3^3 at the input port of *Gm*. Since the voltage amplitude after the mixer will eventually have a nonlinear element, applying the proposed Gm attenuated network-based low pass filter will effectively lead to an input linear range extension and a transconductance reduction by a factor of 3^N. Fig. 2.16 illustrates how linear attenuation can be implemented. Assuming each transconductor has a strictly monotonic nonlinear odd-symmetry voltage-current relationship, I_{out} and I_X are described by:

$$I_{out} = f(V_+ - V_-) = -f(V_+ - V_-) \tag{2-22}$$

$$I_x = f(V_1 - V_3) = f(V_3 - V_4) = f(V_4 - V_2) \tag{2-23}$$

A linear relationship between input and output voltages is thus found as:

$$V_{out} = V_3 - V_4 = \frac{V_1 - V_2}{3} = \frac{V_{in}}{3} \tag{2-24}$$

In this work, a 2nd-order Gm-C LPF in Fig. 2.17 provides a transfer function as described by (20):

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{G_{m1}G_{m2}}{C_1C_2} \frac{1}{s^2 + s\frac{G_{m2}}{C_2} + \frac{G_{m1}G_{m2}}{C_1C_2}} \tag{2-25}$$

It is possible to make $G_{m1} = G_{m2} = G_m$ if all stages are biased with the same bias current *IB*. Also, note that the cut-off frequency is $\omega_H = \frac{G_m}{\sqrt{C_1 C_2}}$ while the quality factor is $Q = \sqrt{\frac{C_1}{C_2}}$. Due to the transient speed enhancement from the proposed LIA, the LPF is not necessary to be designed in a very narrow cut-off frequency to retrieve the phase information. Since the LIA is targeting a frequency range around 100 Hz, a total on-chip capacitor of 50 pF can be used ($C1 = 2C2 = 25$ pF), and the entire filter circuit is fully integrable.

2.3.4 PVT-COMPENSATED INVERTER-BASED COMPARATOR.
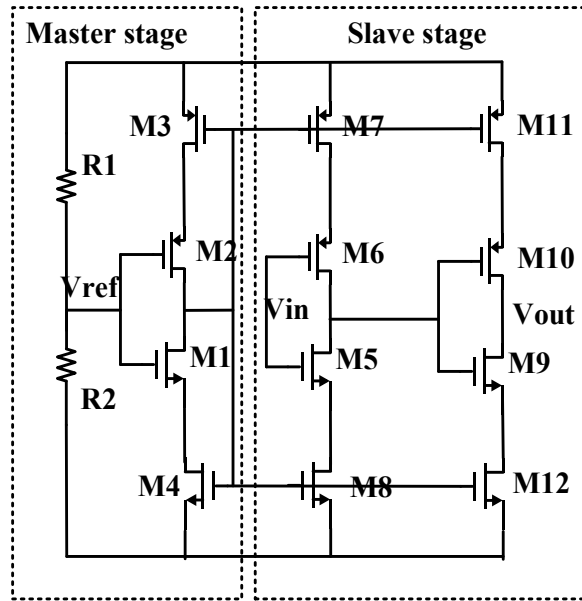
Fig. 2.18 The PVT-compensated inverter-based comparator.

In the proposed LIA, the inverter-based comparator shown in Fig. 2.18 [25] is used to produce precise feedback decisions to the FSM after the SC-integrator. A one-bit digital output is generated by forcing the input voltage to be compared with the inverter's switching threshold. Master stages are formed by R_{1-2}, M_{1-4}, while slave stages are formed by M_{5-12}. Transistors M_{7-8} and M_{11-12} operate in the triode region and acts like voltage-controlled resistors. Inverters consisting of M_{5-6} and M_{9-10} are tuned by triode region transistors to set their switching thresholds. The transistors M_{1-2}, that forms an inverter in the master stage, which are the same size as those in the slave stage.

Resistors R_{1-2} generate an input voltage of V_{ref} to the master stage inverter, and the output voltage tunes M_{3-4}.

The master stage generates a negative feedback mechanism. The intuitive analysis is described as follows. When the threshold voltage of the master stage inverter goes lower than V_{ref} due to the PVT change, the output voltage of the master stage inverter will decrease. This will cause a decrease in the resistance of r_{ds} of M_3 and an increase in the resistance of r_{ds} of M_4. To counteract this change, the switching threshold will shift back to V_{ref}. When the switching threshold goes higher than V_{ref}, the negative feedback will shift it back to V_{ref} since $M_{7,11,}$ and $M_{8,12}$ are voltage-controlled resistors that have their own resistance R_p and R_n. We derive a simple inverter swing threshold voltage V_M without the proposed process compensation biasing network as the following:

$$R_p = \frac{1}{\mu_p C_{ox}(W/L)(|V_{GS,p7,11}-|V_{th,p7,11}|)} \tag{2-26}$$

$$R_n = \frac{1}{\mu_n C_{ox}(W/L)(|V_{GS,n8,12}-|V_{th,n8,12}|)} \tag{2-27}$$

$$I_D = \frac{\mu_n C_{ox}(W/L)}{2}(V_{GS,n} - V_{th,n})^2 = \frac{\mu_p C_{ox}(W/L)}{2}(V_{GS,p} - V_{th,p})^2 \tag{2-28}$$

The process compensation network based on the compensation factors generated from $M_{7,11,}$ and $M_{8,12}$ is mathematically proven in the switching threshold given in (26)-(30).

$$V_M = \frac{V_{th,n}+R_{n2}I+\sqrt{\frac{\mu_p(W/L)p}{\mu_n(W/L)n}}(V_{dd}-V_{th,p}-R_{p2}I)}{1+\sqrt{\frac{\mu_p(W/L)p}{\mu_n(W/L)n}}} \tag{2-29}$$

$$\text{Assume } \sqrt{\frac{\mu_p(W/L)p}{\mu_n(W/L)n}} = 1$$

$$V_M = \frac{V_{th,n}+R_{n2}I+(V_{dd}-V_{th,p}-R_{p2}I)}{2} = \frac{V_{dd}+(V_{th,n}-V_{th,p})+(R_{n2}I-R_{p2}I)}{2} \tag{2-30}$$

If the switching threshold voltage ($V_{th,n} - V_{th,p}$) increases, while the V_{ref} maintains constant, the output of the master voltage will increase because the V_{ref} will be recognized as voltage level "low". Moreover, ($R_{n2}I - R_{p2}I$) will decrease to compensate the process variations ($V_{th,n} - V_{th,p}$) and vice versa.

2.3.5 SWITCH-CAPACITOR-BASED PRECISE PHASE SHIFTER
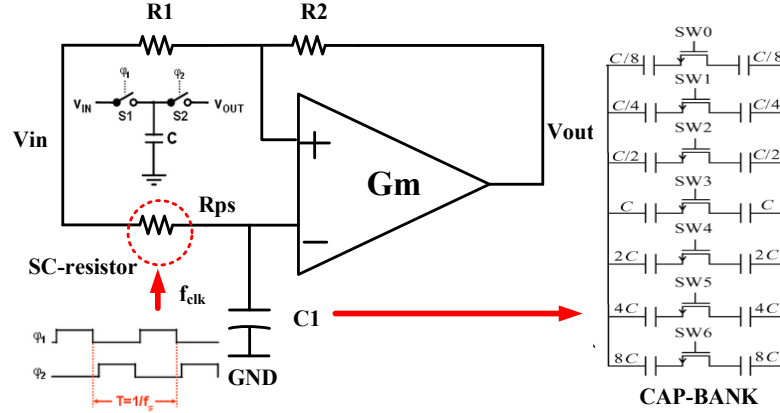
Fig. 2.19 Programmable Phase Shifter for the Generation of the reference signal with phase compensation

The phase shifter provides a shifted replica of the input signal at the output. The designed phase shifter used in this work is shown in Fig.2.19 and is based on [6]. However, our implementation replaces the resistor Rps with a switched capacitor. This resistance dominates the phase shifter output time, and the switched capacitor implementation allows the phase adjustment independently of process variations. The phase shifter core topology is a first-order opamp-based all-pass filter whose transfer function is described by (2-31):

$$\frac{V_{out}}{V_{in}} = \frac{1 - sCR}{1 + sCR} \tag{2-31}$$

According to (2-31), the phase shift between the input and the output can be described by:

$$\varphi = 180 - 2arctan(2\pi R_{ps}Cf_0) = 180 - 2arctan(2\pi f_0 \frac{\sum_{i=1}^{10} B_i[n]}{f_{clk}}) \tag{2-32}$$

where $\sum_{i=1}^{10} B_i[n]$ represents the final calibration coefficients by tuning the switches from the capacitor bank. The phase shift depends on the clocked switch capacitor-based R_{ps} and C_1 as well as on the operation frequency f_0. A sampling clock frequency $f_{clk} = 1\text{KHz}$ was chosen to reduce the PVT variations of the RC time constant and cancel the capacitor ratio to reduce the capacitor mismatch. Consequently, the resulting phase angle of the entire adjustment block only depends on the compensation coefficients from the previous SAR controller, which is precise.

2.3.6 IMPLEMENTATION FOR THE OTHER CIRCUITS

SAR control logic and FSMs are implemented based on synchronous static D-flip flop. Fig. 2.20 shows the architecture of the SAR control logic, and Fig. 2.21 shows its subsystem design. The signal *control* is generated as SAR input based on FSM from the previous stage. To initialize the SAR for the phase calibration, all registers in the SAR need to be cleared by the signal *start*. The MSB bit, b_{10}, is set to high on the first rising edge of this clock. Additionally, the MSB value will either remain the same or change to low based on the value input. So long as the LSB of the SAR controller is not determined, the process repeats.
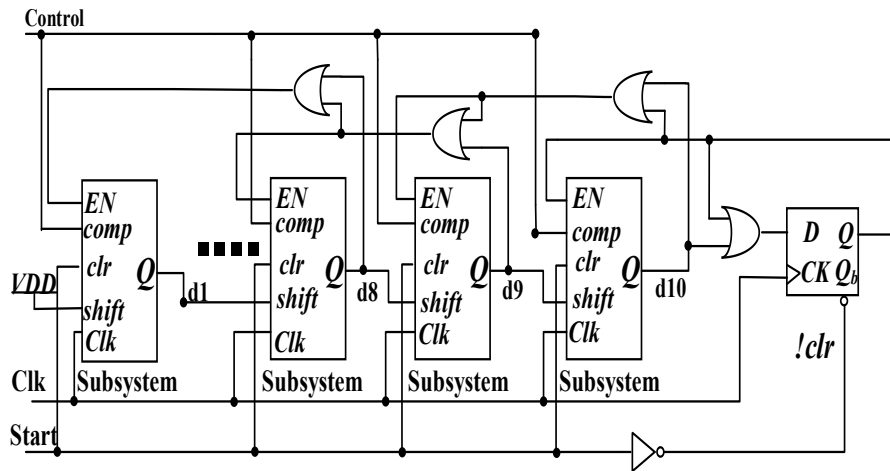
Fig. 2.20 Proposed synchronous static SAR register
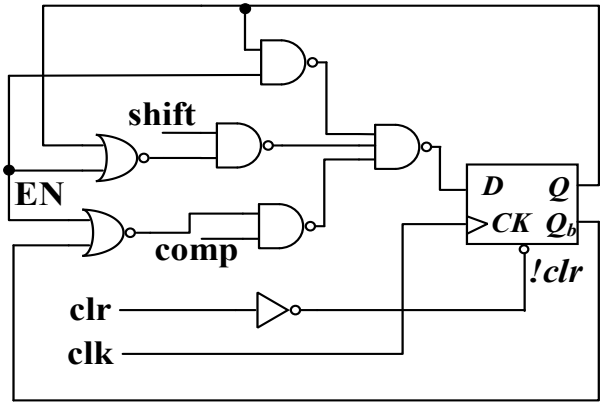
Fig. 2.21 Subsystem of SAR logic

B.
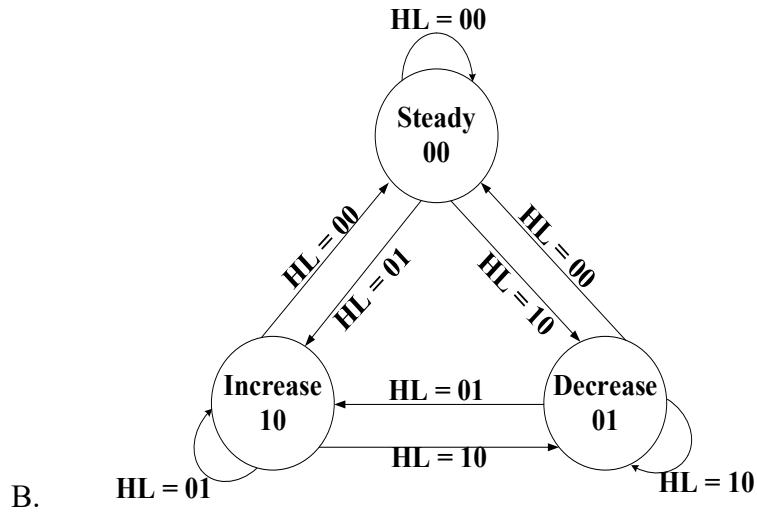
Fig. 2.22 State diagram of proposed automatic -Gm controller.
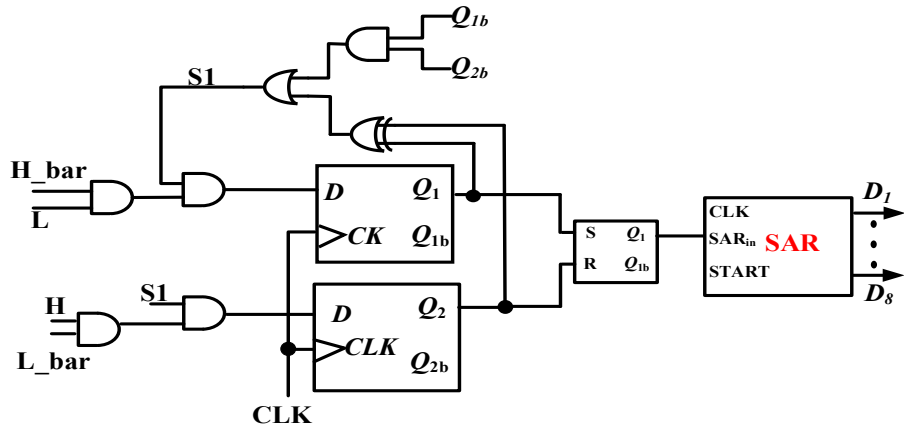
Fig. 2.23 Proposed Finite state machine (FSM)
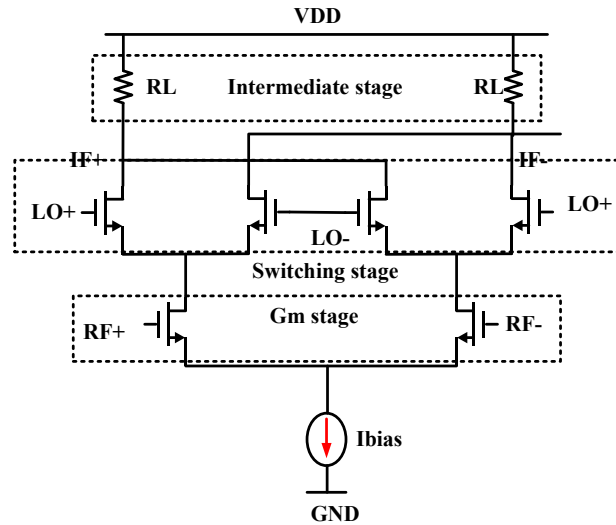
Fig. 2.24 Architecture of a conventional active Gilbert cell mixer.
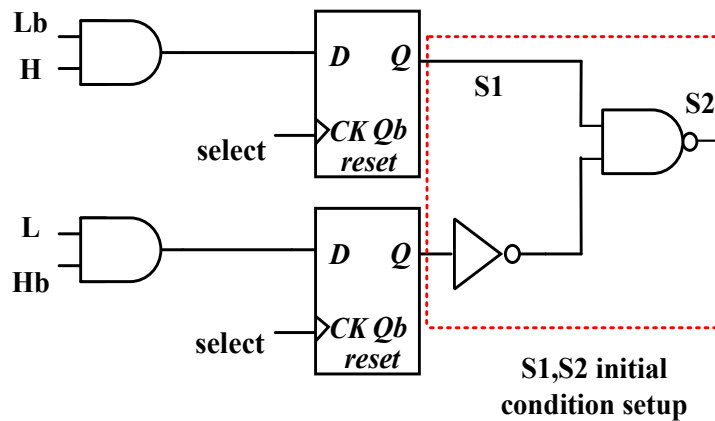
Fig. 2.25 Automatic phase quadrant selection MUX

Fig.2.22 and 2.23 depict the FSM diagram and architecture for the proposed phase compensation controller circuit. The FSM is controlled by the signals "H" and "L" generated by the inverter-based comparator and the 1-bit conversion. This state diagram presents three states: the *Steady* state, the *Increase* state, and the *Decrease* state. The state *Steady* indicates that automatic phase calibration has been completed or that the calibration loop is keeping its previous state while waiting for the next estimation period. In *Increase* state, the input signal's current phase lags, indicating an uncompensated phase that must be increased. In the state *Decrease*, the reference signal phase will be leading in the presence of a phase comparison, which must therefore be decreased.

The direct-conversion receiver topology shown in Fig. 2.24 is often the preferred option for LIAs. Its performance is critical because it directly affects the performance of the entire LIA. The

conventional double-balanced Gilbert cell is the most used mixer in direct-conversion receivers. The major advantages are good port-to-port isolation and low even-order harmonic distortion.

Finally, the automatic phase selection (APS) shown in Fig. 2.25 is essential to be added along with the programmable phase shifter to perform initial phase error $\Delta\varphi$ monitoring. The initial condition of S_1 and S_2 controls the phase shifter's positive and negative output sequence (refer to Fig. 2.2 and system-level simulation in Fig.2.3). If the input signal phase leads to the local signal phase, the output of the LPF is positive (above V_{cm}); thus, an automatic phase calibration will perform the phase calibration normally. Otherwise, if $\Delta\varphi < 0$, which means the local signal is leading the input signal, a much longer calibration process will occur, or the LIA might even enter the calibration "dead zone." This is because the SAR controller controls the phase shifter tuning coefficients from the CAP-bank, namely $[0: \sum_{i=1}^{10} B_i[n]]$, always be in the positive direction.

The operating principle of the proposed automatic phase selection will work as follows. When the phase error $\Delta\varphi > 0$, the CAP-bank from the phase shifter will be set into the initial condition between $[0: \sum_{i=1}^{10} B_i[n]]$ for phase calibration. When $\Delta\varphi < 0$, the S_1 and S_2 control switches will swap the phase shift to initialize the condition $\Delta\varphi > 0$ by adding a 180° phase shift initially in the proposed LIA architecture. It is good to recall the $\Delta\varphi = \theta_{sig} - \theta_{ref}$, and the change is directly reflected on the LPF as (2-33):

$$V_{LPF =} 0.5 * A_{sig} \ A_{ref} \ sin \ (\theta_{sig} \ - \theta_{ref}) \tag{2-33}$$

where $\Delta\varphi = \ sin \ (\theta_{sig} \ - \theta_{ref})$.

2.4 EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed LIA was implemented in 0.18 μm standard CMOS technology, with a power supply voltage of 1.8V, and its microphotograph is presented in Fig. 2.26. The entire chip area is 1.8 mm x 2.4 mm. The Signal Power Detection (SPD) path and automatic phase alignment loop (APA) are labeled in the photo with the other different blocks. The LIA is designed for a 100Hz operation frequency with a tunable bandwidth 50Hz. The integrated die had mounted in a PCB along with the input generated from the function generator and two channels with/without noise testing environment for signal buried under the ambient noise. All the circuits had a common ground, with

the same supply voltage. The input biasing voltages are generated from LDO on the PCB. The input signal is generated from a Agilent 3352A function generator, and the transient input and output signals were measured using the DPO4104 Tektronix oscilloscope.
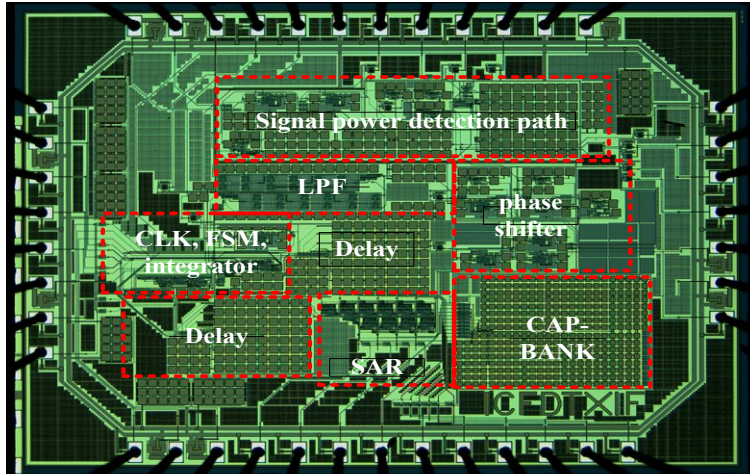
Fig. 2.26. The microchip of the proposed LIA, including the SPD path and APA loop
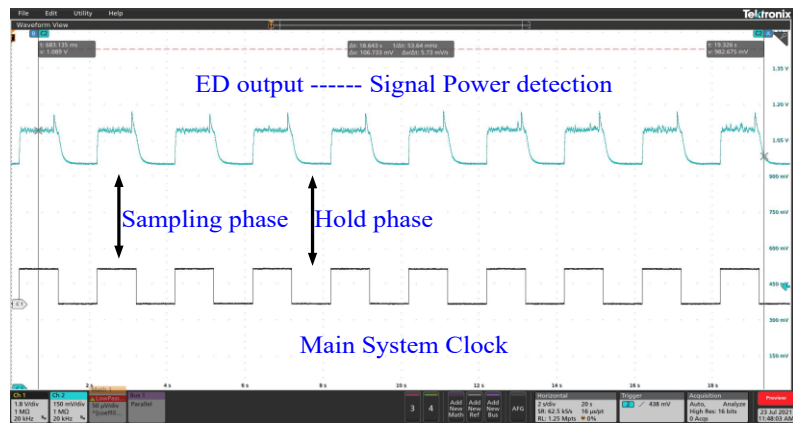
Fig. 2.27 Experimental results of $2\omega_c$ based on signal power detection LIA respects to the input signal power.
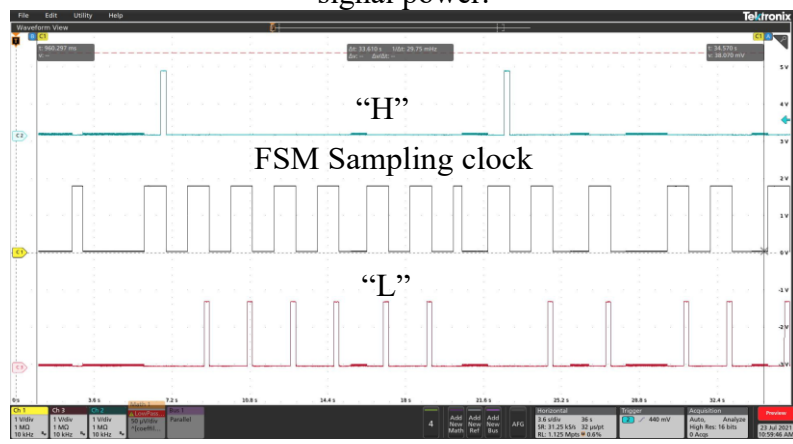
Fig. 2.28 Finite state machine input "H", "L" with the built-in FSM clock
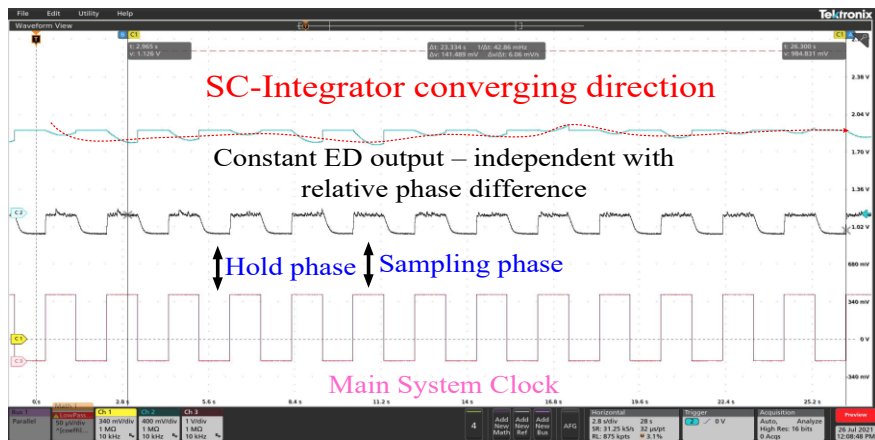
Fig. 2.29 SC-integrator converging process to V_{cm} at every sampling phase of the Main system clock
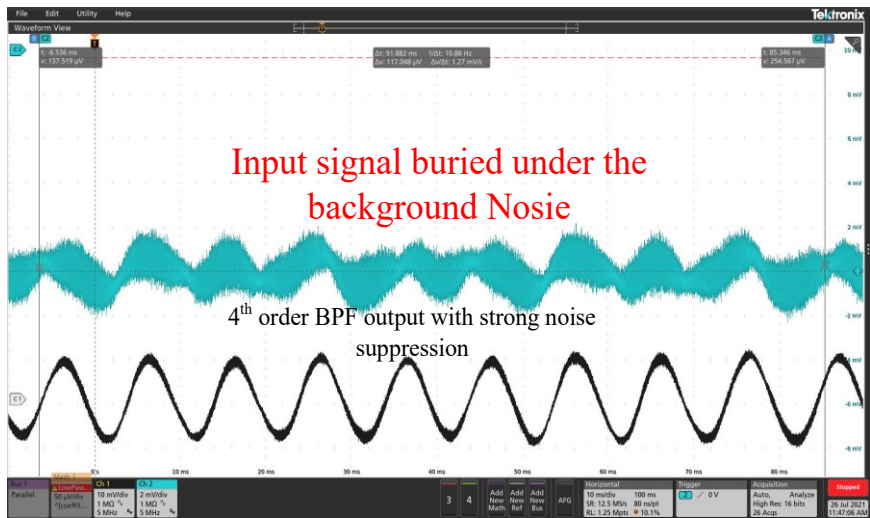
Fig. 2.30 Proposed BPF with strong filtering effect against input signal buried under ambient noise and flicker noise
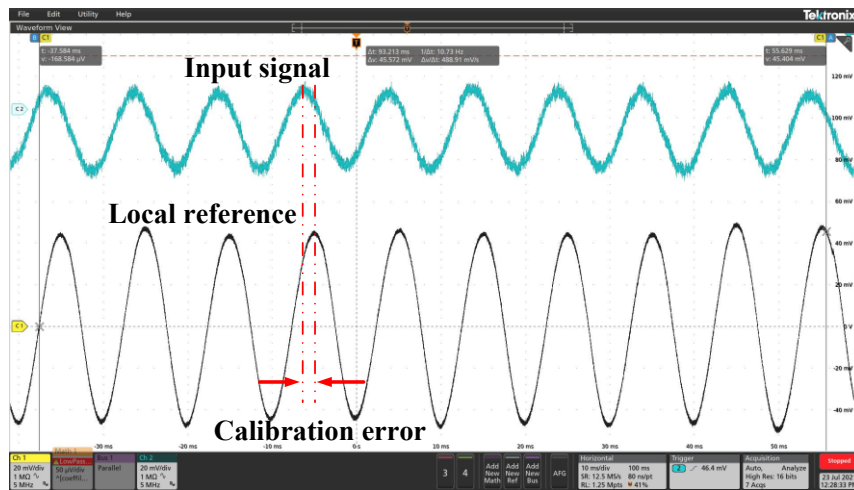
Fig. 2.31 Input signal vs local reference achieves approximate automatic phase alignment by background calibration
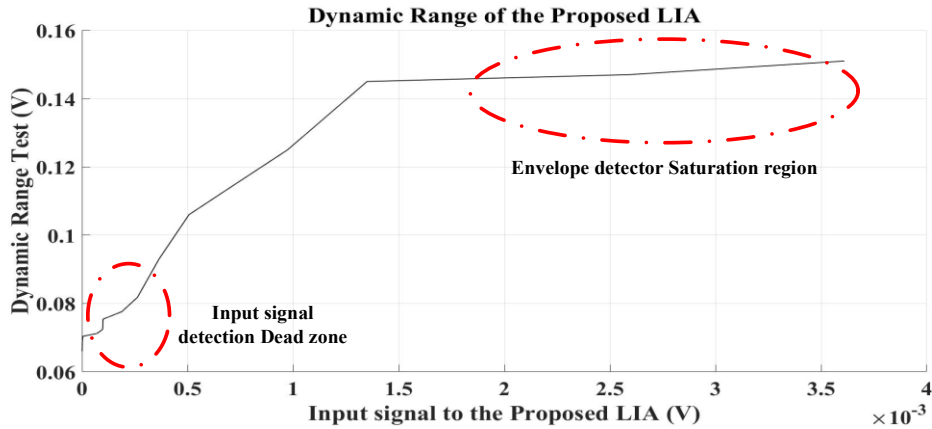
Fig. 2.32 Proposed LIA Dynamic Range measurement test

The performance of the proposed LIA is evaluated through the transient input and output signals. As shown in Fig.2.27, the 2nd harmonic frequency method properly works, allowing the signal detection in the designed LIA.

The signal power detection is directly proportional to the input signal power, which is constant, as indicated by the constant ED output voltage. Furthermore, it shows that the input signal power detection through the envelope detector is constant and independent of any phase difference along with the central system clock – an essential advantage of the proposed technique.

Figure 2.28 shows the measured waveforms of the FSM sampling clock and the input of the signal "H," and "L" of the FSM generated by the inverter-based comparator & 1-bit conversion. The dynamic phase calibration is based on the indicator of "H" and "L". If "H L" = "1 0", the phase offset is below V_{cm}, while if "H L" = "0 1", the phase offset is above V_{cm}. The presented results show the dynamic process of the phase calibration of the proposed phase alignment loop. Fig. 2.29 shows the SC integrator will converge to a value very close to V_{cm} upon completion of the calibration. This work's entire phase calibration process takes approximately 15-20 s.

Fig. 2.30 shows the proposed band-pass filtering capacity to suppress the input signal buried under the ambient noise. It indicates that the input signal is prefiltered using a band-pass filter (BPF) to increase the SNR further before it passes through the mixer. Fig. 2.31 shows the input signal and local reference signal can achieve phase alignment after automatic phase alignment with slight offset calibration error ($<5°$-$10°$). The phase information will be automatically reflected on the digital codes on the SAR controller.

Fig. 2.32 shows a dynamic range (50 µV – 3 mV) with a minimum resolution of 25 µV. The minimum detection range for the proposed LIA is measured when its output is saturated under ambient noise without triggering the input signal. The maximum detection range is defined as the LIA saturation point when the output swing is limited. The proposed LIA can also achieve fast phase calibration (< 20 s), a small silicon area, and power consumption. Thus, it constitutes a more versatile, hardware efficient, and power-efficient solution for phase adjustment without degrading the performance on integrated LIAs prototypes. A new figure of merit (FOM), described by (34), is proposed to mensurate the trade-off between the performance parameters and make it possible to compare the power, frequency, and dynamic reserve trade-off among state-of-art reported LIAs.

$$FOM_{LIA} = DR(dB) + 10log \frac{BW(Hz)}{Power(w)} \tag{2-34}$$

Where *power* is the total power consumption of the LIA, *f* is the operating frequency, and *DR* is the dynamic reserve (minimum signal power detection). BW is the LIA detection bandwidth. The higher is the FOM_{LIA}, the better the power-frequency trade-off is. The proposed LIA clearly can extract very low-input-power signals (amplitude/phase information) buried under the background noise, presenting a high dynamic reserve (maximum SNR). The main characteristics of the proposed LIA are summarized and compared with previous works in Table II. The proposed LIA exhibits the FOM_{LIA} of 116 dB among recently published designs.

TABLE 2.2
SUMMARY OF RESULTS AND COMPARISON WITH OTHER WORKS

Parameters	This work	[5]	[6]	[8]
Technology	0.18-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.35-μm CMOS
Supply	1.8 V	1.8V	1.8 V, 3.3V	3.3V
Frequency	100 Hz	11 Hz	1 KHz	20 KHz
Dynamic Range	$25\mu V - 3mV$	35-700nV	4.5mV-17mV	NA
Detection bandwidth	50 Hz	2.5-25 Hz	125KHz	13-25 KHz
Dynamic reserve	65 dB	34 dB	35.5 dB	NA
LIA type	Single-phase & calibration	Single-phase & calibration	Dual-phase no calibration	Single-phase no calibration
Power consumption	360 μW	2 mW	7 mW	13 mW
FOM $_{LIA}$	116 dB	74.5 dB	117 dB	98.8 dB

2.5 CONCLUSION

This paper presents a single-channel LIA based on 2nd order harmonic extraction and an automatic phase alignment scheme. The signal power detection path based on 2nd order harmonic extraction can extract the signal power independent of the phase difference between the input and local reference signals. Moreover, the proposed technique increases the transient speed of the system. The proposed LIA presents the best FOM (55.4 nW/Hz) among compared works, while its dynamic reserve is as high as 65 dB over a detection bandwidth of 50 Hz. The proposed automatic phase alignment technique monitors the relative phase difference between the input and reference signals and performs a calibration phase using a phase shifter. Finally, the proposed fully on-chip LIA system operates with a single supply dedicated to high-accuracy, low-speed, low-power (<mW), and portable measurement systems, for instance, biomedical applications.

CHAPTER 3 A 14.5-BIT ENOB, 10MS/S SAR-ADC WITH 2ND ORDER HYBRID PASSIVE-ACTIVE RESONATOR NOISE SHAPING

Ximing Fu[1], Kamal El-Sankary[1], Senior Member, IEEE

[1]Electrical and Computer Engineering, Dalhousie University, Halifax, NS, Canada

ABSTRACT

A new 2nd order noise shaping (NS) based successive approximation register (SAR) ADC is presented in this paper. In comparison to earlier research, this paper considers hybrid passive-active integrators to compensate for the phase error of the passive integrator. To realize the resonator noise shaping in a high-speed asynchronous SAR-ADC, the hybrid passive-active sigma-delta modulator (SDM) is introduced as a multi-input, feed-forward loop filter. This overcomes the conventional asynchronous SAR-ADC noise barrier generated from the CDAC, quantizer, and dynamic comparator. The proposed noise shaping technique significantly reduces the ADC power consumption and area compared with the active SDM noise shaping approach. This circumvents the shortcomings of passive SDM, such as a large area, low resolution, and low speed. It consists of very low power, forward gain G and positive feedback path across a 1st order passive switch capacitor (SC) integrator that desensitizes capacitor ratios under PVT variations. Extensive circuit simulation verifications and system-level results have been used to validate the effectiveness of the proposed NS SAR-ADC. The simulation results show that the proposed SAR ADC consumes 0.88mW at 10MS/s, with an SNDR of 89.43 dB and SFDR 98.64 dB within 0.1 fs oversampling frequency.

3.1 INTRODUCTION

In modern communication systems, several high-precision analog-to-digital converters (ADCs) need to be used. To meet the requirements of high precision and wide bandwidth, a series of new ADC structures have successively appeared. Noise shaping successive approximation ADC (NS SAR-ADC) is one of the most popular structures studied in recent five years. While the conventional SAR-ADC has low power consumption and a small area [33–35], the comparator's noise and offset, quantization noise, and complimentary DAC (CDAC) thermal noise limit its accuracy. On the other hand, the sigma-delta ADC is the most used structure to achieve high precision, but due to the need for many opamps in this structure, its power consumption is high, and the area is large. The NS-SAR ADC structure is a hybrid SAR-ADC and sigma-delta modulator (SDM) that inherits both advantages. It has the characteristics of a SAR ADC in terms of low power consumption and considerable potential to achieve high precision, like sigma-delta ADC. Moreover, NS SAR-ADC requires a lower oversampling ratio (OSR) than the traditional sigma-delta modulator, thus increasing bandwidth.

References [35-37] described methods for reducing the input-referred noise and offset of SAR ADC using a time-domain comparator to reduce the total power at the cost of a slow conversion, which makes it less desirable for high-speed applications. The SDM is the most critical candidate architecture considering oversampling and noise shaping techniques from a high-resolution perspective. An active integrator based on opamps is the critical component, typically power-hungry and challenging to scale. SAR ADC with an SDM significantly improves the capability of a NS SAR-ADC to overcome the deficiencies mentioned above, making it a preferred approach for delivery of both high resolutions and low power consumption simultaneously [29-30]. The authors in [29] proposed a noise-shaping technique using FIR and IIR filters. For sampling the residue voltage, a two-tap charge-domain FIR filter is utilized. An IIR noise shaping filter constructed from operational amplifiers serves as an integrator to enhance noise shaping. Nevertheless, an active integrator is introduced, which inevitably deteriorates the energy efficiency and scalability of the circuits. In [31], the authors have proposed a first-order noise shaping without the requirement of opamps using passive integrators, the design has high efficiency without interrupting the normal SAR-ADC operation. In this case, the zero in [31] is set at 0.5, indicating poor noise shaping and resulting signal attenuation of 6 dB. Furthermore, in recent research publications [35-37], second-order passive noise shaping techniques are proposed to increase the DC attenuation in the noise transfer function (NTF). The values of α and k (which refer to the capacitor ratios and comparator gain respectively), are increased significantly, as explained in Section II-A, which inevitably increases the power and area of the chip. Therefore, the loop dynamics in terms of ADC speed and stability will be significantly impacted, as the CDAC settling time is one of the most apparent bottlenecks for high-speed SAR-ADC.

This paper proposes a second-order low-power hybrid passive-active NS-SAR ADC architecture to overcome the previous problems. In contrast to prior works, passive-active integrators based on low gain open-loop opamps are used in the loop filter instead of conventional opamp-based active integrators. Zeros in the system are determined solely by capacitor ratio and positive feedback compensation, insensitive to process, voltage, or temperature (PVT) variations. Moreover, a resonator is introduced in the loop to achieve wide noise-shaped bandwidth.

Aside from noise shaping techniques, the choice of capacitive CDACs is also of critical importance. It has been demonstrated that DAC switching schemes such as monotonic switching (MS) provide very good energy efficiency. Compared to conventional structures, this topology reduces switching-related

energy losses by 81% [38]. The MS structure degrades ADC performance due to variations in the common-mode level offset within the comparator. To stabilize the dynamic amplifier's input common-mode (CM) level, a common-mode-stabilization (CMS) circuit is proposed within the NS SAR ADC architecture.

This paper is organized as follows; Section 3.2 focuses on the fundamental theory of noise-shaping SAR-ADC and design considerations. Section 3.3 details the proposed NS SAR-ADC architecture, including proposed noise shaping architecture and detailed circuit implementations. Section 3.4 describes the extensive simulation results at the circuit and system levels, while Section 3.5 summarizes the paper's conclusions.

3.2. FUNEDMENTAL THEORY ANALYSIS OF NOISE SHAPING AND DESIGN CONSIDERATIONS

3.2.1 PASSIVE INTEGRATOR VS. ACTIVE INTEGRATOR

Fig.3.1 illustrates the active and passive integrators. The transfer functions for the 1st order active and passive integrators are written as:
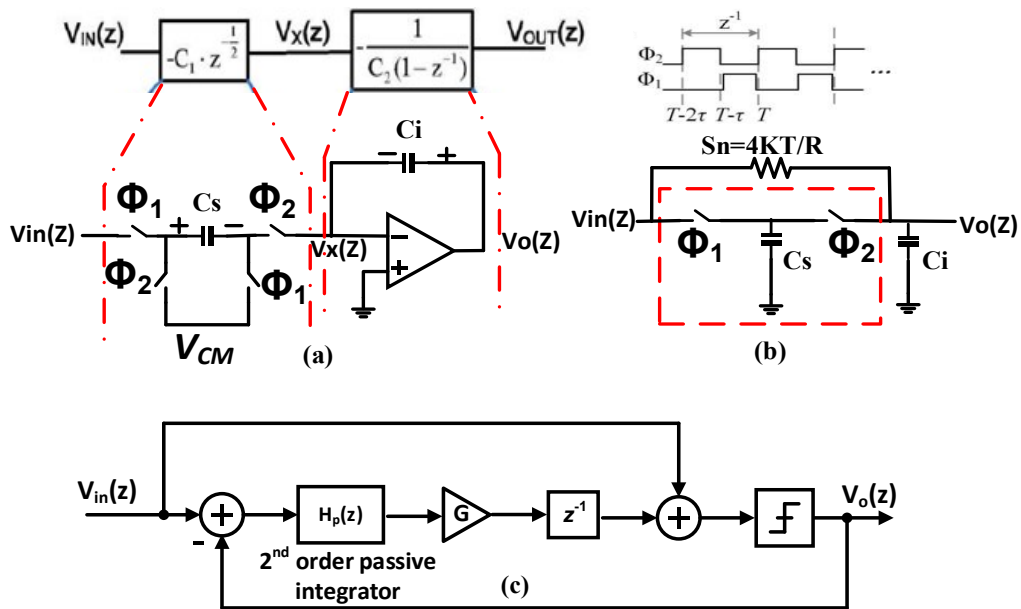
Fig 3.1. (a) 1st order active integrator (b) 1st order passive integrator, (c) 2nd order passive noise-shaping SAR ADC [33-34],[37],

$$H_{\text{active}}(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{C_S}{C_i}\frac{z^{-1}}{1-z^{-1}} \qquad (3\text{-}1)$$

$$H_{\text{passive}}(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{\alpha z^{-1}}{1-(1-\alpha)z^{-1}}, \text{ where } \alpha = \frac{C_S}{C_S+C_i} \qquad (3\text{-}2)$$

where C_S is sampling capacitor and C_i is integrating capacitor. As opposed to the ideal active integrator transfer function (1), the passive integrator's transfer function (2) exhibits both gain and phase error. Due to the built-in analog trade-offs, the passive transfer function cannot be modified to resemble an ideal active transfer function. First, to reduce gain error, C_S must be greater than C_i, which results in an increase in phase error. However, C_i should be greater than C_S to reduce phase error, which leads to increased gain error. Thus, there is a trade-off between sizing C_i and C_S. The feedforward gain of the comparator can usually compensate for the gain error in an NS SAR-ADC, though noise shaping is not properly performed if excessive phase error occurs. Since the phase error is crucial, it shifts the pole of the integrator and, therefore, the zero of the NTF of the loop filter as well, according to (3). This pole shift flattens the low-frequency part of the noise transfer function, which in turn significantly reduces the effect of noise shaping within the passband.

$$NTF(z) = \frac{1}{1+H(z)} = \frac{1-(1-\alpha)z^{-1}}{1-(1-2\alpha)z^{-1}}, z = 1, NTF(z) = 0.5 \qquad (3\text{-}3)$$

Similarly, as shown in Fig.3.1(c), the works published in [33-34],[37], use 2nd order passive noise shaping and have severe limitations i.e., DC suppression and stability. To satisfy the noise shaping capability and stability requirements, the 2nd order passive noise shaping requires excessive capacitor ratios, α_{1-2} and comparator gain, G for noise-shaping. These parameters dramatically reduce the ADC's speed, with a large area penalty. This inevitably introduces considerable kickback noise and dynamic power requirements for the comparator, as discussed below.
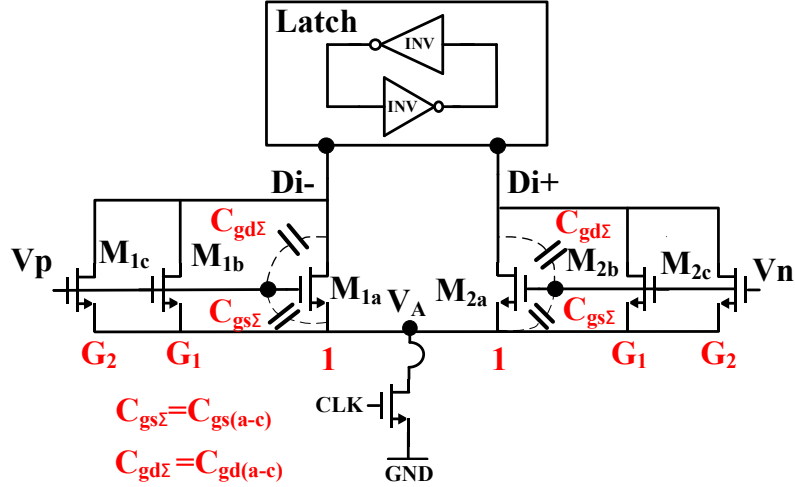
Fig 3.2. The general model of the impact of kickback noise on multi-input dynamic latch comparator

Assume the CDAC has a capacitor value equal to C, and the 2nd order passive integrators have capacitor values $\alpha_1 C$, and $\alpha_2 C$. the NTF(z) can be rewritten as:

$$H_{2nd\ passive}(z) = z^{-1}G\,\frac{1}{1+\alpha_1(1-z^{-1})}\,\frac{1}{1+\alpha_2(1-z^{-1})} = \frac{z^{-1}G}{p_1(z)p_2(z)} \tag{3-4a}$$

$$NTF(z) = \frac{1}{1+H_{2nd\ passive}(z)} = \frac{p_1(z)p_2(z)}{p_1(z)p_2(z)+z^{-1}G} \tag{3-4b}$$

$$= \frac{[z(1+\alpha_2)-\alpha_2][z(1+\alpha_1)-\alpha_1]}{z^2(1+\alpha_1\alpha_2+\alpha_1+\alpha_2)+(-\alpha_1-\alpha_2-2\alpha_1\alpha_2+G)z+\alpha_1\alpha_2}$$

$$z=1,\ NTF(z) = \frac{1}{1+G} \tag{3-4c}$$

Stability analysis from the Jury array gives:

$$G < 2(\alpha_1+\alpha_2)+4\alpha_1\alpha_2+1 \tag{3-4d}$$

To reduce the phase error, α_1 and α_2 must assume large values. Also, to reduce gain error and ensure stability, the comparator gain G must be large. In the passive NS SAR multi-input latch comparator, as depicted in Fig.3.2, the gain G is provided by the input transistors. Increasing the gain, G at the expense of increasing the size of the input transistors has severe limitations. Resolution of passive NS SAR

ADC's is limited due to non-idealities associated with the multi-input dynamic latched comparator. These non-idealities in multi-input dynamic latched comparator include offset voltage, thermal noise, and kickback noise. The kickback noise can be problematic when it comes to a high-speed SAR ADC, causing the settling time and accuracy of the decision to be significantly affected. While upsizing the input MOS pair $M_{1,2(a\text{-}c)}$ of the comparator can increase the gain, G and reduce thermal noise, it will adversely increase the kickback noise due to higher drain-gate parasitic capacitances of the input MOS pair.

The Kickback noise is dynamic in nature, as the input MOS pair in the whole comparison process can operate in a variety of regions (such as cut-off, saturation, or triode), which will have a significant impact on the accuracy of the decision [50]. The full expression of kickback noise of multi-input latched comparator can be written as:

$$Q_{cut-off} = V_{cm}C_{gb} + V_{GS}C_{gs} + (V_{cm} - V_{DD})C_{gd} \tag{3-5a}$$

$$Q_{G,sat}(t) = \frac{2}{3}(1 + G_1 + G_2)WLC_{ox}(V_{cm} - V_A(t) - V_{th}) + (V_{cm} - V_A(t))C_{gs} + (V_{cm} - D_{i+}(t))C_{gd} \tag{3-5b}$$

$$Q_{G,triode}(t) = (1 + G_1 + G_2)WLC_{ox}(V_{cm} - V_A(t) - V_{th}) + (V_{cm} - V_A(t))C_{gsS} + (V_{cm} - D_{i+}(t))C_{gd} \tag{3-5c}$$

where V_{cm} is the common-mode level of V_p and V_n. Cgb is the equivalent capacitance between the gate and substrate, Cgs and Cgd are the gate-source and gate-drain overlap capacitances, respectively. WLCox refers to the gate oxide capacitance that includes the input pair (M_{1a}-M_{2a}) used for the normal SAR conversion and input pairs (M_{1b}-M_{2b}, M_{1c}-M_{2c}) used for noise-shaping. In the passive noise-shaping techniques described in the literature, the feedforward gains $G_{1,2}$ implemented at the inputs of the comparator need to be substantially large to guarantee stability according to (4d), while high α_1 and α_2 must be large to reduce the passive integrator's phase error. Since increasing gain results in increased kickback noise charges induced at the gate of the input MOS pair $M_{1\text{-}2}$, ADC resolution suffers during both comparison and latch operations.

The previous analysis concludes that the multi-input comparator gains $G_{1,2}$ must be large enough to improve the NTF(z) at its DC suppression, satisfying the stability requirement while maintaining small enough gate capacitance to reduce dynamic power and kickback noise, leading to a design trade-off. We can find in the available 2nd order passive NS SAR ADC in the literature, the area of the integrator capacitor is around four times larger than the CDAC capacitor ($\alpha_{1,2} \cong 4$) and that limits the speed and increases power consumption. Also, the resolution of the ADC is limited by the kickback noise of the multi-input comparator due to high gains $G_{1,2}$ values.

3.2.2   DIRECT 2ND ORDER SDM IMPLEMENTATION-BASED NOISE SHAPING ANALYSIS AND ITS LIMITATIONS

To improve the noise shaping performance compared to passive implementation, direct noise shaping is derived from an ideal 2nd order SDM. The ideal noise transfer function, $\text{NTF}_{\text{ideal}}(z)$, is implemented as shown in Fig.3.3 (a)-(b). Since the ideal noise transfer function has no stability issues, it is used directly. Its corresponding loop filter transfer function is:

$$\text{NTF}_{\text{ideal}}(z) = (1 - z^{-1})^2 \tag{3-6}$$

$$\text{H}_{\text{ideal}}(z) = \frac{2z^{-1} - z^{-2}}{(1 - z^{-1})^2} \tag{3-7}$$
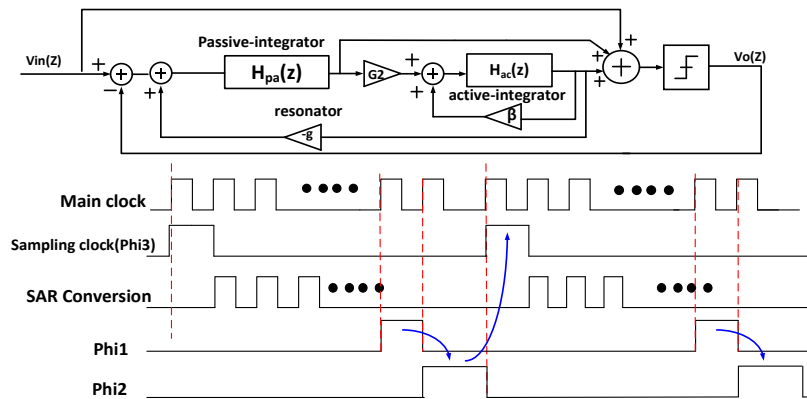
Fig 3.5. Proposed hybrid Passive-Active noise-shaping SAR ADC system-level implementation and timing diagra
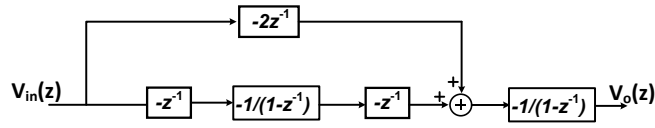
(a)
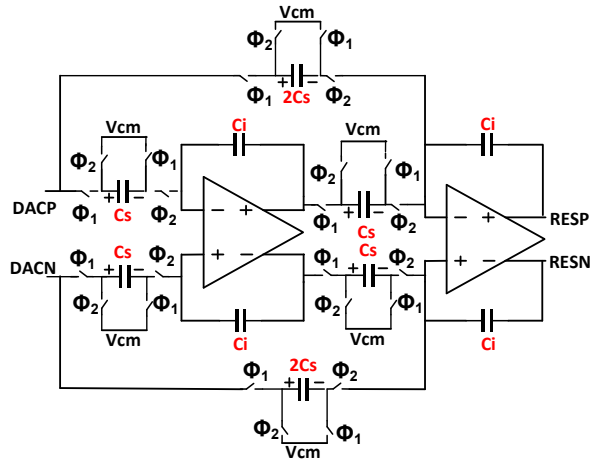
(b)

Fig 3.3. Direct 2nd order noise shaping (a) implementation block diagram. (b): circuits implementation.

When the normal SAR-ADC conversion is done, the input signal V_{in} is converted directly into digital outputs through the comparator. Therefore, the STF is always equal to 1 in the NS SAR-ADC. Note that the normal SAR-ADC residue after conversion is a low-frequency DC signal, which dictates the SDM architecture's choice. Two main strategies can be applied in the NS SAR-ADC design. The first strategy, refers to a direct implementation method, is to use a lower-resolution SAR-ADC ($<$ 8bit) with a noise-shaping module with a strong shaping capability. This strategy is implemented with an active opamp-based integrator, including multiple high-performance opamps, which consume high quiescent power. The second strategy is to use a medium-resolution SAR-ADC ($\sim$10-bit) with an intermediate noise-shaping module with medium-shaping capability, composed of a very low-power active or passive integrator and consumes less power. Fig.3.3(a)-(b) shows system-level and circuit-level implementations of the direct implementation strategy. When clock $\varphi1$ is high, the first stage includes the feedforward path sample the normal SAR-ADC conversion residue. The second integrator stage samples the previous value from the first stage integrator output. When the clock $\varphi2$ is high, the first stage integrator starts its integration, and at the same time, the second stage integrator and the feedforward path transfer the

57

sampled value in the first half cycle through the output. Unlike opamp-based sigma-delta modulator design trade-offs, the proposed SAR-ADC constrains the SDM input signal to be a DC value, and the amplitude is around 1 LSB of the standard 10-bit SAR ADC without NS, which significantly relieves the slew rate requirement of the opamp. The integration phase must have a fast settling response during noise shaping before the comparator works in the following conversion cycle. Consequently, the approximated unity-gain bandwidth of the opamp must be very high, leading to high power consumption. In addition, an opamp with a finite DC gain will introduce higher-order harmonics at the ADC output. As a result, the opamp must have a fast-settling time and large DC gain, but with a relaxed slew rate requirement.

3.2.3 PROPOSED 2ND ORDER PASSIVE-ACTIVE INTEGRATOR-BASED NOISE SHAPING ANALYSIS
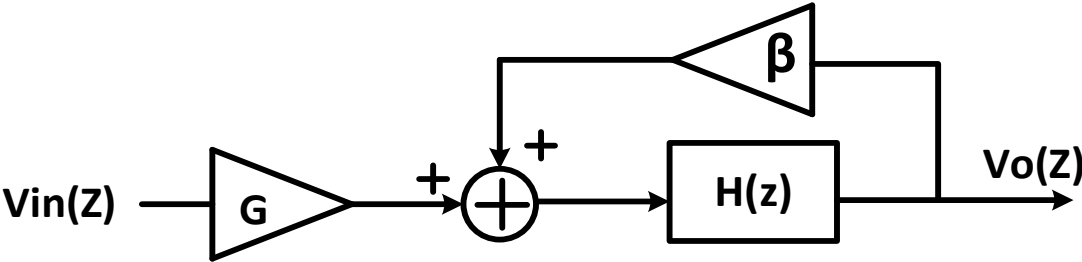
Fig 3.4. Proposed integrator phase error compensation technique model.
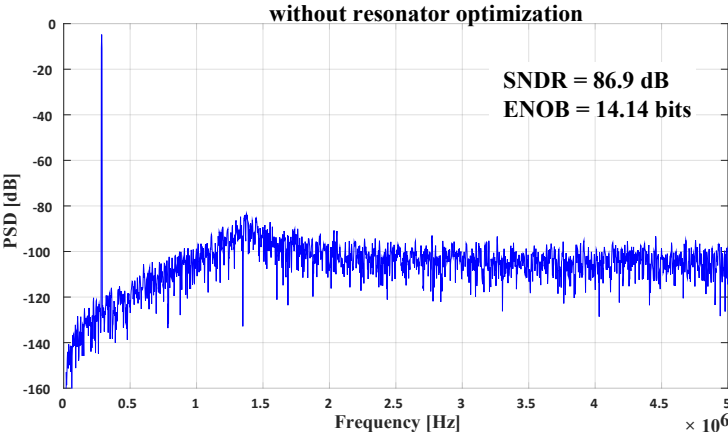
(a)
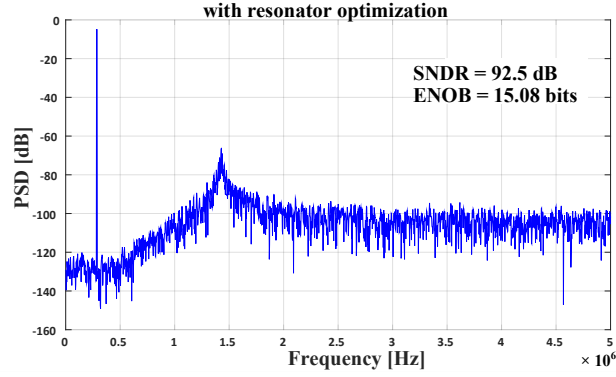
(b)

Fig 3.6. Proposed Passive-active noise-shaping SAR ADC system-level simulation (a) without resonator optimization (b) with resonator optimization

Fig. 3.4 illustrates a technique that utilizes positive feedback across a passive 1st order SC integrator, which is inspired by [17-18] and can compensate for the phase error. Moreover, it is possible to compensate for the second stage integrator phase error with an input gain G. A detailed illustration of the block diagram of the proposed SAR-ADC is shown in Fig. 3.5. Fig.3.6 shows the proposed NS SAR-ADC system-level simulation. To simplify the design strategy, first, we ignore the resonator feedback g and let $\alpha_{1,2} = \frac{c_{s1,2}}{c_{s1,2}+c_{i1,2}}$, and $c_{i1} = c_{DAC}$. The modulator transfer function analysis yields:

$$H_{passive}(z) = \frac{\alpha_1 z^{-1}}{1-(1-\alpha_1)z^{-1}} = \frac{\alpha_1 z^{-1}}{p_1(z)} \tag{3-8a}$$

$$H_{active}(z) = \frac{G\alpha_2 z^{-1}}{1-z^{-1}+\alpha_2(1-\beta)z^{-1}} = \frac{G\alpha_2 z^{-1}}{p_2(z)} \tag{3-8b}$$

$$H_{hybrid}(z) = H_{passive}(z)H_{active}(z) + H_{passive}(z) \tag{3-8c}$$

The proposed NTF (z) has the following transfer function:

$$\text{NTF }(z) = \frac{1}{1+H_{hybrid}(z)} = \frac{p_1(z)p_2(z)}{p_1(z)p_2(z)+p_2(z)\alpha_1 z^{-1}+G\alpha_1\alpha_2 z^{-2}} = \frac{p_1(z)p_2(z)}{Den(z)} \tag{3-8d}$$

where $p_1 = 1 - (1-\alpha_1)z^{-1}$, $p_2 = 1 - z^{-1} + \alpha_2(1-\beta)z^{-1}$

$$\text{NTF }(z = 1) = \frac{1-\beta}{2(1-\beta)+G} \tag{3-9a}$$

59

$$Den(z) = z^2 + (2\alpha_1 - 2 + \alpha_2 - \alpha_2\beta)z + (G\alpha_1\alpha_2 + 1 - 2\alpha_1 + 2\alpha_1\alpha_2(1-\beta) - \alpha_2(1-\beta))$$

<div align="right">(3-9b)</div>

Assume an ideal positive feedback compensation when $\beta = 1$:

$$Den(z) = z^2 + (-2 + 2\alpha_1)z + G\alpha_1\alpha_2 + 1 - 2\alpha_1$$
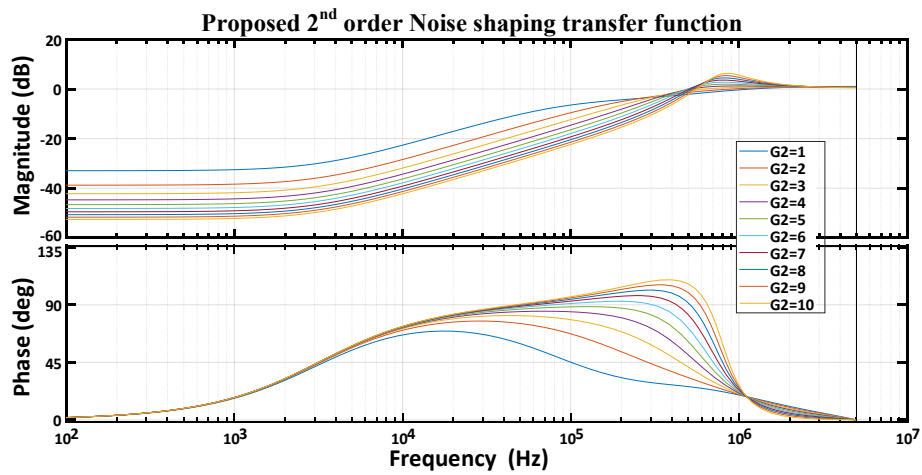
(a)
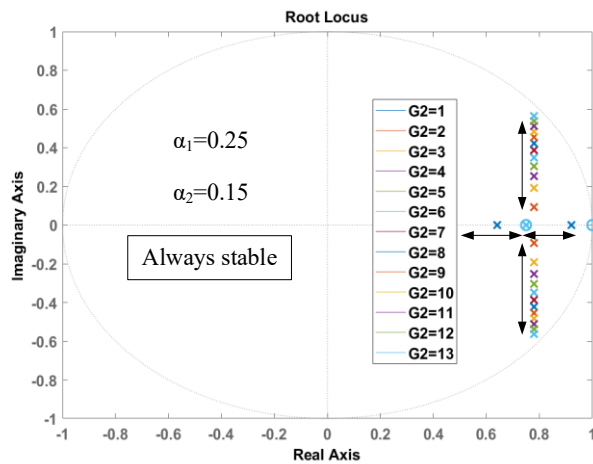
(b)

Fig 3.7. Proposed 2nd order Noise shaping transfer function (a) and pole-zero plot under OTA Gain variations (b).

Apply Jury Array for stability gives:

$$\begin{cases} Den\ (1)\ = \alpha_1\alpha_2 G > 0, \\ Den(-1)\ =\ \alpha_1\alpha_2 G - 4\alpha_1 + 4 > 0, \\ \quad \dfrac{-2}{\alpha_1} + 2 < G\alpha_2 < 2 \end{cases} \tag{3-9c}$$

The proposed NTF(z) has two zeros which refer to as $z_1 = 1 - \alpha_1$, and $z_2 = 1 - \alpha_2(1 - \beta)$. The closer the zero of the NTF(z) is to 1, the stronger the NS capability is, which means the integrator is closer to ideal. Compared with the entirely passive noise shaping techniques, the essential advantage of the proposed solution is that increasing G to improve the noise shaping capability will not inflict extra power and kickback noise to the comparator. The open loop gain G and compensation factor β simultaneously work toward achieving better shaping ability, significantly reducing the noise and improving the resolution of the ADC. A better shaping requires a smaller α_1 value that is limited by the kT/C noise. The zero location of z_2 is determined by β, while β is set at approximately one to minimize the phase error of the second-stage passive integrator. Moreover, the kT/C noise of the second-stage passive SC integrator is referred to as the input and will be divided by the opamp gain, so the size of the second-stage integrator capacitors has a negligible effect on the thermal noise.
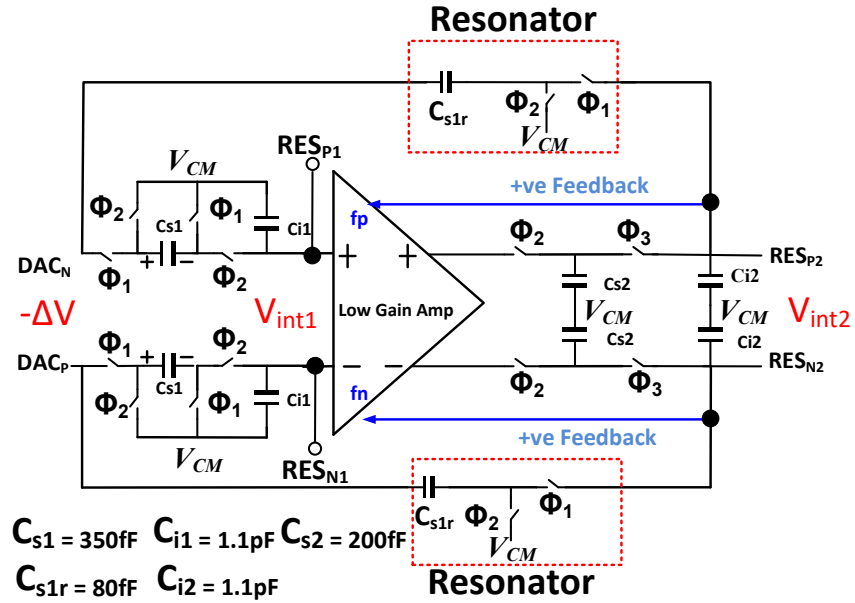
(a)
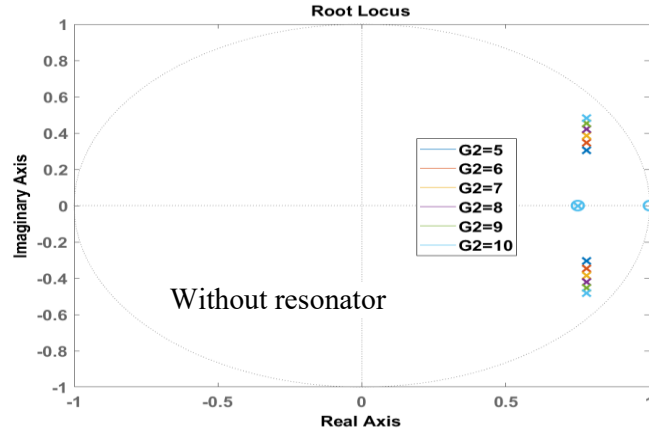
(b)
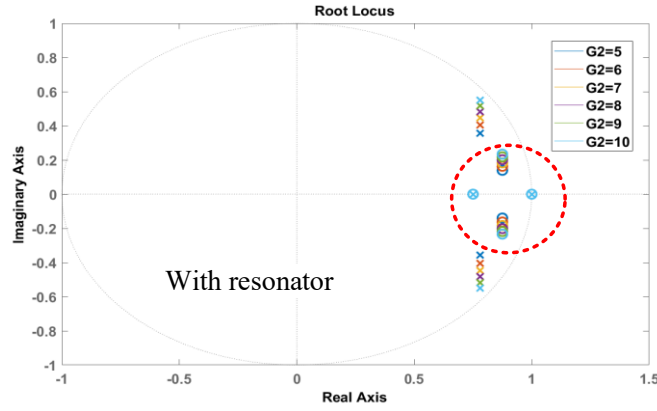
(c)

Fig 3.8. (a) Detailed implementation of proposed noise shaping scheme (b)-(c) Passive-active noise-shaping NTF(z) with/without zero optimization

The thermal noise is limited by the first stage of the passive integrator sampling capacitor C_{s1}. Since α_1, α_2 are designed to be around $0.15\sim0.25$ in the proposed ADC.

The minimum Cs_1 is given by:

$$C_{s1} = \frac{kT2^{2N}}{OSR(V_{FS})^2} \qquad (3\text{-}10a)$$
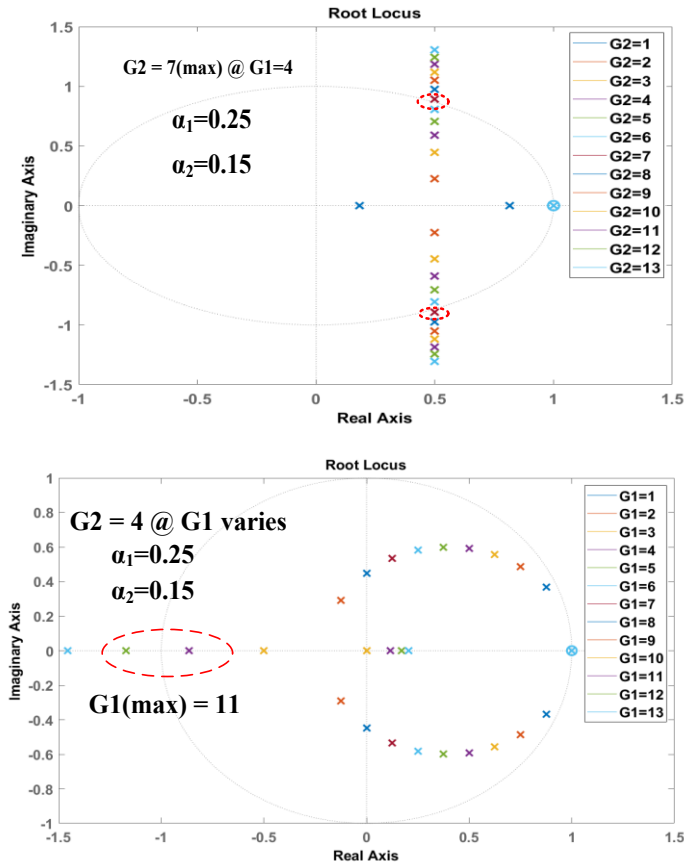
Fig 3.9. 2nd order active-active noise shaping pole-zero plot under OTA Gain variations.
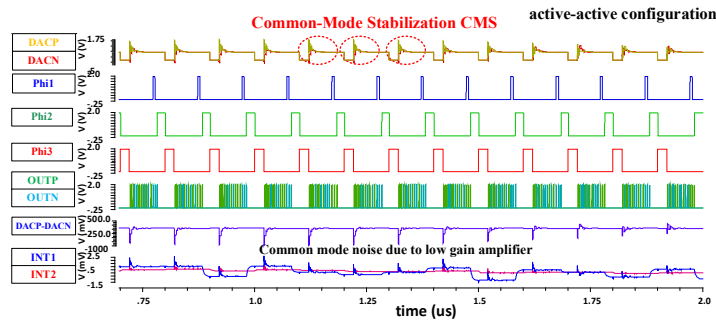
Fig 3.10. Common-mode noise leakage from DACP-DACN to proposed loop filter due to OTA low Gain for active-active configuration

where k represents the Boltzmann constant, T is the absolute temperature, N is the effective number of ADC bits and V_{FS} represents the full-scale input. The second stage output noise is simply equal to the equivalent RC integrator shown in Fig. 3.1 (b). Thus, the SC resistor R acts the same as a resistor in

terms of thermal noise power which will not influence the noise in the output spectrum. The second stage input-referred noise can be written as:

$$V_{in,2nd}^2 = \frac{1}{G} \int_0^\infty \frac{4kTR}{1+(2\pi RCf)^2} df = \frac{kT}{GC_{i2}}$$

(3-10b)

Fig.3.8 shows the proposed loop filter designed with passive-active architecture and resonator feedback to improve the ADC noise-shaping performance and the bandwidth further. In our proposed noise-shaping module, conjugate zeros are introduced in NTF(z) by adding a local negative feedback loop at the input and output of the two cascaded passive-active integrators. The local feedback shifts the loop filter poles away from DC to enhance the noise shaping performance. To evaluate the performance of the proposed noise shaping module with a resonator, the complete transfer function of the proposed sigma-delta modulator is written as the following, and the simulation of the resonator effect is shown in Fig.3.8 (b)-(c).

$$H_{hybrid-resonator}(z) = \frac{H_{passive}(z)H_{active}(z)+H_{passive}(z)}{1+gH_{passive}(z)H_{active}(z)}$$

(3-11)

Reference [45-46] uses a low-gain opamp with a positive feedback circuit in a discrete-time sigma-delta modulator to solve the gain and phase errors caused by the passive SC integrator. However, its input signal amplitude is limited to a small range. The ratio of rail-to-rail voltage swing to maximum input swing is 55%. In a noise-shaping SAR-ADC, the input signal is first converted fully by the conventional high-speed SAR-ADC, then it is integrated through the noise-shaping block, where the signal entering the noise-shaping block is small in amplitude. Therefore, this active-passive hybrid noise shaping technique is much more suitable for a noise-shaping SAR ADC as compared to a sigma-delta modulator. The capacitor ratios α_1 and α_2 are composed of capacitance ratios, which have high immunity to process variations. The opamp gain G is designed by simple common-source amplifiers. The proposed NTF and pole-zero stability analysis in Fig.3.7 shows the robustness of the circuits under gain variations. It demonstrates that with significant variations of G, the proposed NS SAR ADC can maintain its stability provided α_1 and α_2 can be small enough, and the limitation of parameters is dictated by the thermal noise of the ADC. Moreover, second-order noise-shaping designed in an active-active module, which realizes an ideal NTF, will not be a proper candidate for two reasons: (1) high sensitivity for the discrete-time

loop dynamics compared with the proposed hybrid passive-active solution and (2) common-mode noise leakage from the SAR regular conversion. Like the previous analysis, the stability analysis of active-active noise shaping arrangement is the following:

$$H_{active1}(z) = \frac{G_1\alpha_1 z^{-1}}{1 - z^{-1} + \alpha_1(1-\beta)z^{-1}} = \frac{G_1\alpha_1 z^{-1}}{p_1(z)}$$

$$H_{active2}(z) = \frac{G_2\alpha_2 z^{-1}}{1 - z^{-1} + \alpha_2(1-\beta)z^{-1}} = \frac{G_2\alpha_2 z^{-1}}{p_2(z)}$$

$$H_{ac}(z) = H_{active1}(z)H_{active2}(z) + H_{active1}(z)$$

$$NTF_{ac}(z) = \frac{p_1(z)p_2(z)}{p_1(z)p_2(z) + G_1\alpha_1 G_2\alpha_2 z^{-2} + p_2(z)G_1\alpha_1 z^{-1}} = \frac{p_1(z)p_2(z)}{Den(z)} \tag{3-12a}$$

$$NTF_{ac}(z=1) = \frac{(1-\beta)^2}{(1-\beta)^2 + G_1 G_2 + G_1(1-\beta)} \tag{3-12b}$$

Assume $1 - \beta = 0$ due to the positive feedback compensation.

$$Den(z) = z^2 + (G_1\alpha_1 - 2)z + 1 - G_1\alpha_1 + G_1\alpha_1 G_2\alpha_2$$

Apply Jury Array for stability gives:

$$\begin{cases} Den(1) = G_1\alpha_1 G_2\alpha_2 > 0 \\ Den(-1) => G_1\alpha_1 G_2\alpha_2 - 2G_1\alpha_1 + 4 > 0 \\ \frac{-2}{G_1\alpha_1} + 1 < G_2\alpha_2 < 1 \end{cases} \tag{3-12c}$$

The active-active module has more strict stability requirements compared with (9c) and (12c). Fig.3.9 and Fig.3.10 demonstrate the active-active module's stability variations and common-mode noise leakage problems. The system simulation of stability analysis shown in Fig.9 is performed while considering enough design margin of thermal noise from the switch capacitor integrator with, $\alpha_1 = 0.25$, $\alpha_2 = 0.15$, $\beta = 1$ as a typical example. Compared with the proposed technique stability plot in Fig.3.7,

the stability requirements are stricter, making the circuits more sensitive to PVT variations. Moreover, as shown in Fig.3.10, common mode (CM) noise leakage is severe due to the low opamp gain, which reduces the ADC noise shaping performance. Since the open-loop opamp with low gain will be greatly affected by the CM noise suppression of the SAR, the passive stage (based on bottom plate sampling) is selected as the first stage in the proposed design. While the ideal solution for a low-power NTF implementation is an active-active architecture using an open-loop opamp-based integrator, the variations in the integrator coefficients and the DC gain of the opamp will impact the stability of the entire discrete-time loop dynamics, and it will be sensitive to PVT variations. Equations (12a)-(12c) demonstrate that the gain coefficients $G_{1,2}$ are highly related to stability, which is relatively difficult to achieve compared to the proposed passive-active implementation.

3.3. CIRCUITS IMPLEMENTATIONS AND DISCUSSIONS

Fig.3.11 shows the proposed asynchronous SAR ADC architecture. This ADC design adopts the bottom-plate sampling method to minimize charge injection and clock feedthrough from the sampling capacitor during the sampling phase. The bottom-plate sampling mainly takes advantage of disconnecting the sampling capacitor bottom plate so that the leakage charge from the sampling switch will not be injected into the sampling capacitor top plate. Another advantage is that when the proposed NS-SAR-ADC is under the sampling phase, the noise-shaping module can still perform its 2nd integration (refer to Fig.3.10 and Fig.3.14) before the subsequent cycle conversion starts. That significantly improves the speed of the ADC. A multi-input-based comparator shown in Fig.3.12 (a) and a self-ring clock generator shown in Fig.3.12(b) are used to perform the summation function for the coefficients at the differential nodes DACP and DACN. Fig.3.13 shows the proposed low gain open-loop amplifier with the positive feedback. As the amplifier includes a built-in adding function for superimposing the signal in the positive feedback path, the required power is very low since gain and speed requirements are relaxed. Another important design aspect is that the biasing current is implemented with a constant-gm biasing to reduce the resistor process dependency according to (3-13a-3-13c) owing to the ratio of the resistors.
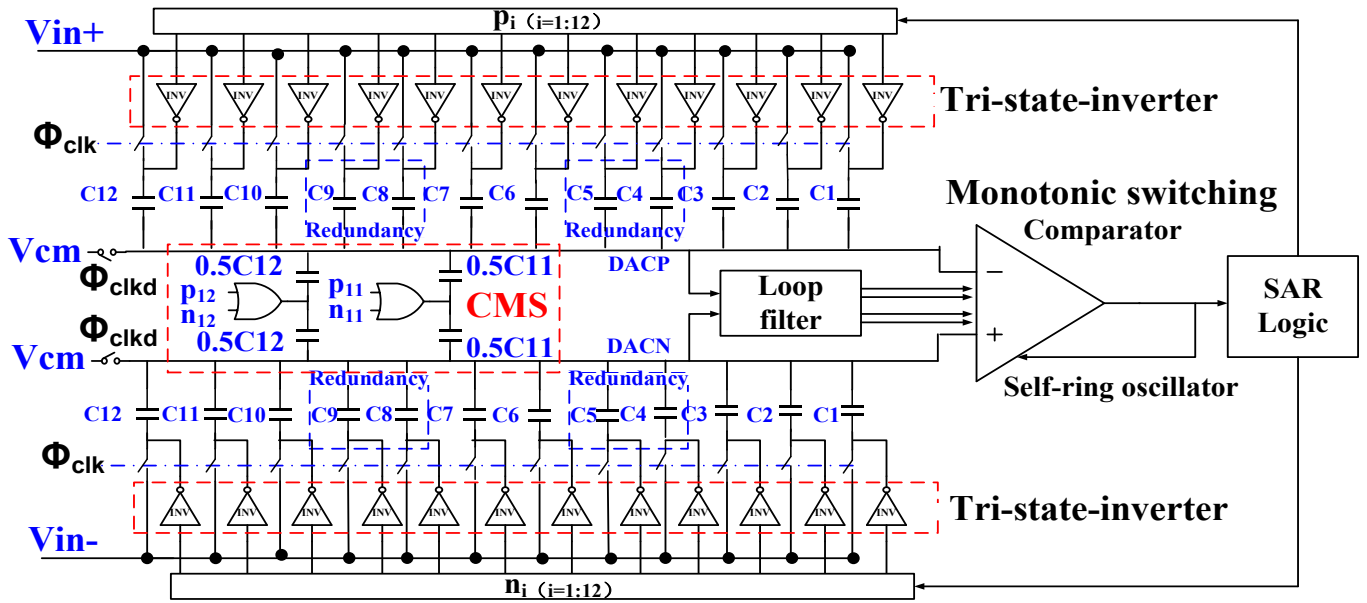
Fig 3.11. Detailed implementation of proposed SAR ADC
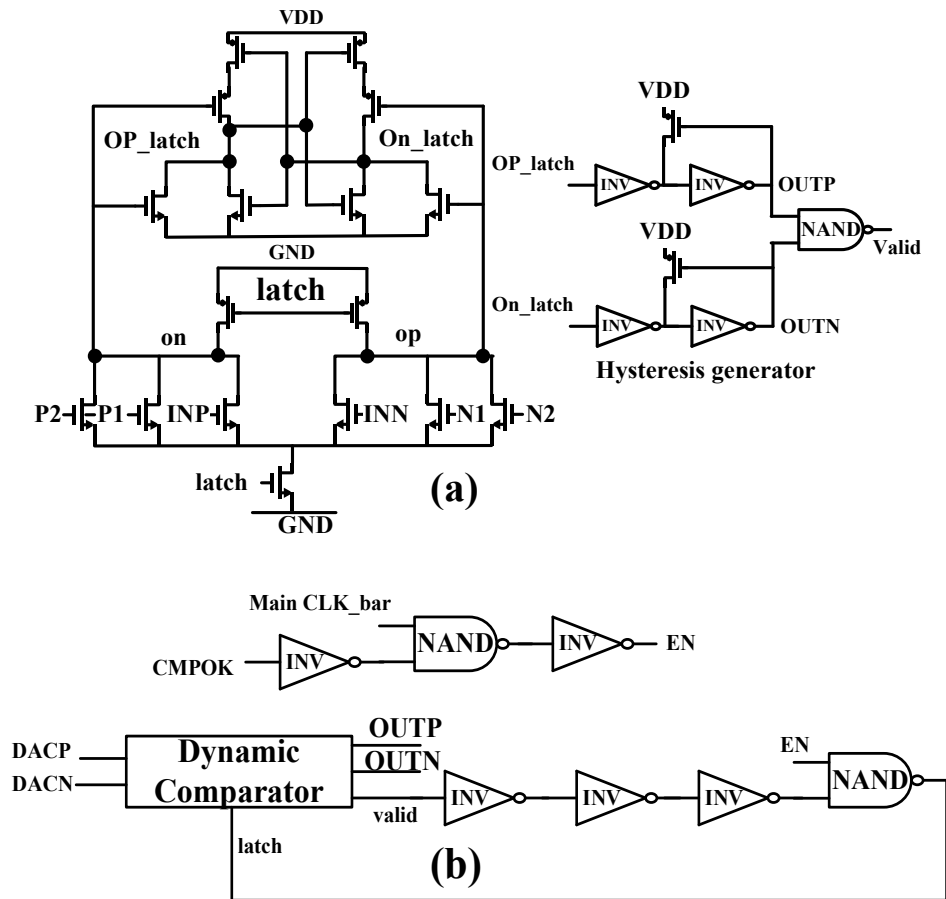
Fig 3.12. Circuit of the double tail dynamic comparator (a) self-ring high-speed clock generator (b)
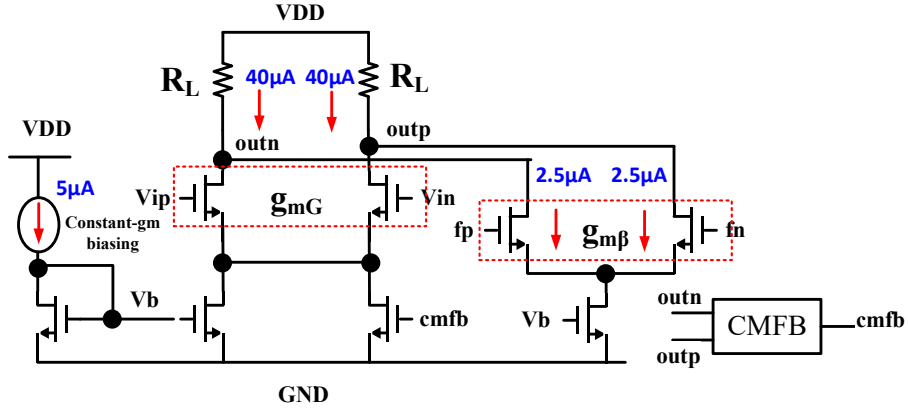
Fig 3.13. Circuit implementation of low gain open-loop amplifier

$$I_{const-gm} = \frac{2}{\mu_n C_{ox}(w/L)_n} \frac{1}{R_S^2}(1 - \frac{1}{\sqrt{k}})^2, \quad g_{mG,\beta} = \sqrt{2I_d \mu_n C_{ox}(w/L)_{G,\beta}} \tag{3-13a}$$

$$G = g_{mG}R_L \propto (1 - \frac{1}{\sqrt{k}})\frac{2R_L}{R_S} \tag{3-13b}$$

$$\beta = g_{m\beta}R_L \propto (1 - \frac{1}{\sqrt{k}})\frac{2R_L}{R_S} \tag{3-13c}$$

During the normal conversion process of the proposed SAR ADC, the conventional monotonic switching scheme moves the comparator input CM level monotonically towards V_{SS} or V_{DD}, causing the conversion gain of the comparator to vary with the input, which would introduce signal-dependent offset to the ADC, degrading the linearity and noise-shaping performance of the ADC. The comparator in the preamplification phase has a significant influence on the offset voltage of the comparator [12] and can be written as:

$$V_{os} = \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2}(\frac{\Delta S}{S} - \frac{\Delta R}{R}) \tag{3-14}$$

where ΔV_{TH} is the mismatch between the threshold voltages of the inputs, $\frac{\Delta S}{S}$ is the input pair size mismatch, and $\frac{\Delta R}{R}$ is the loading pair resistance mismatch. In accordance with (3-14), the offset voltage is affected by mismatches in the devices and their bias conditions. The static term in the expression does not impact the precision of the ADC. Moreover, the overdrive voltage has an impact on the second term.

68

Monotonic switching (MS) scheme results in a gradual decrease in the input CM level of the comparator and hence gain and offset variation in the comparator. To stabilize the comparator input CM voltage, [51–54] introduced an additional DC voltage source. The DC voltage reference buffer requires a large driving capacity, introducing extra power consumption. This work proposes the use of identical capacitors in the common-mode-stabilization (CMS) array whose bottom plates will undergo a transition from V_{SS} to V_{DD} to compensate for the CM drop of the MS CDAC as shown in Fig. 3.11. The CMS capacitors are approximately half the size of their MS DAC counterparts. The OR gate that implements the V_{SS} to V_{DD} transition has two inputs: 1P–2P and 1N–2N, respectively. Due to most of the CM variation is occurring around the MSB, CMS is only applied to the first two MSB bits. As a result of the ith comparison, the voltage swing on each side of the DAC is derived as follows:

$$\Delta V_{pi} = -B_i \frac{2^{n-i-1}C_u}{C_T} V_{DD} + \frac{2^{n-i-2}C_u}{C_T} V_{DD} \tag{3-15}$$

$$\Delta V_{ni} = (B_i - 1) \frac{2^{n-i-1}C_u}{C_T} V_{DD} + \frac{2^{n-i-2}C_u}{C_T} V_{DD} \tag{3-16}$$

where ΔV_{pi} and ΔV_{ni} are the ith positive and negative voltage swings on both sides of the DAC. C_u is the unit capacitance, C_T is the total capacitance of the DAC, and B_i is the ith binary comparison result. It should be noted in (3-15)-(3-16) that the MS network and CMS network are both represented in the first and second terms, respectively. Regardless of the value of B_i, the summation of ΔV_{pi} and ΔV_{ni} remains zero. Therefore, the input CM remains constant at the moment of comparison.

3.4 CIRCUITS SIMULATION RESULTS
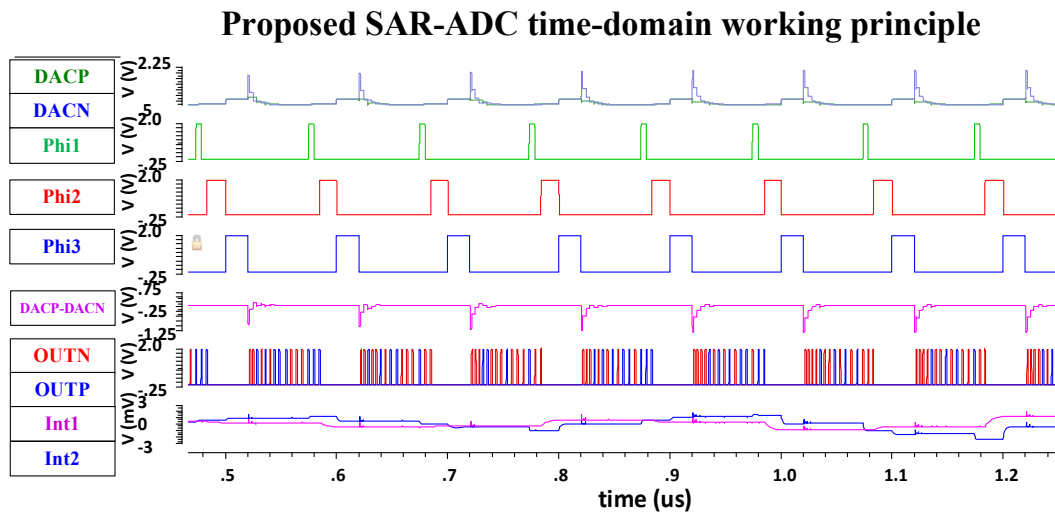
Fig 3.14. Proposed SAR-ADC time-domain working principle
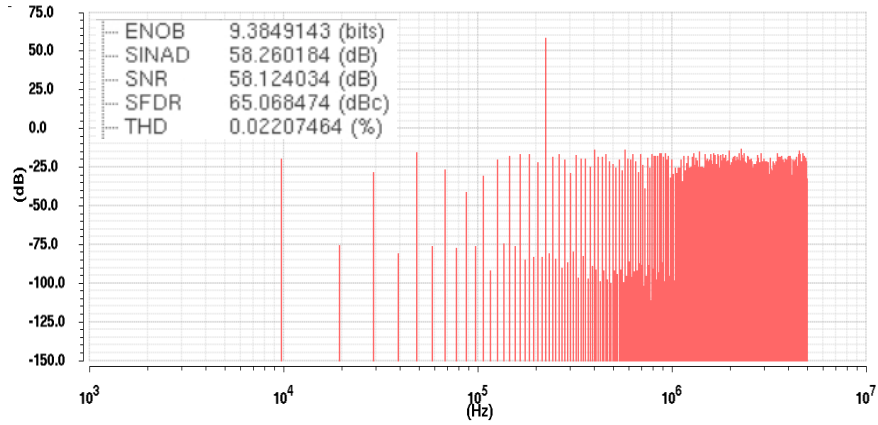
(a)
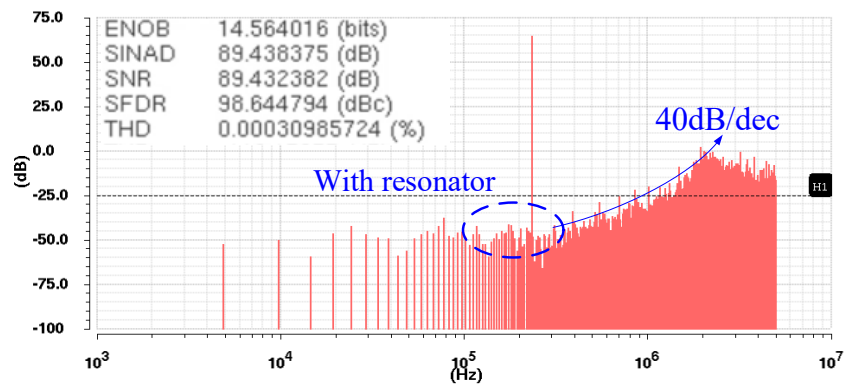
(b)
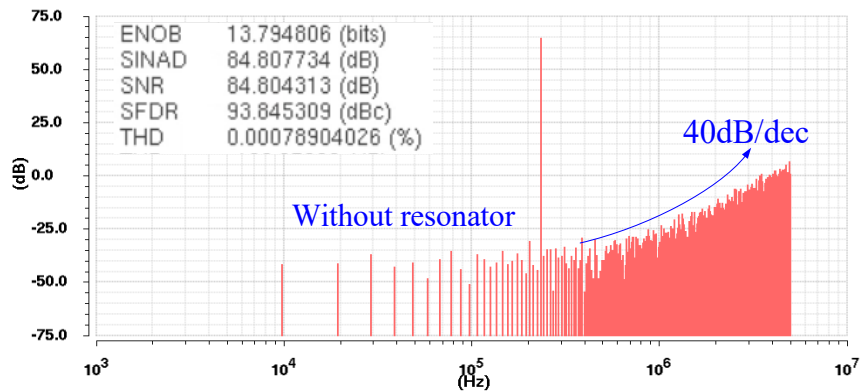
(c)

Fig 3.15. Proposed SAR-ADC: (a) without noise-shaping, (b) with noise-shaping + resonator, (c) without the resonator

Figure 3.14 shows the proposed NS SAR-ADC timing diagram where the normal SAR-ADC conversion is complete before phi_1. The common-mode level remains constant around $V_{DD}/2$, and the passive integrator1 and active integrator2 are operating when phi_1, phi_2, and phi_2, phi_3 are switched on, respectively. The CMS circuits allow the comparator to maintain a low offset and prevent metastability. Another advantage of the bottom-plate sampling is that the sampling clock phi_3 can also be used as the integrator2 integration clock since the new cycle has not yet started during the input sampling phase, and that increases the conversion time and improves the ADC speed. The proposed circuit-level implementation is working under a 1.8V power supply, 10MHz sampling clock rate, and the dynamic comparator is working under a 150MHz asynchronous clock. Fig. 3.15 shows the power spectrum before and after noise shaping, where the input signal frequency is about 250KHz, which is within 1/4 of the ADC bandwidth to include the 3rd order harmonics in the bandwidth.

The designed conventional high-speed asynchronous SAR-ADC without noise shaping shown in Fig.3.15(a) can achieve only a 9.38-bit effective number of bits (ENOB). Fig.3.15(b) and Fig.3.15(c) show the proposed 2nd order hybrid passive-active noise-shaping SAR-ADC with/without a resonator formed by a negative feedback path between the proposed two cascaded passive/active integrators. The negative feedback loop is introduced to change the position of the zeros of the NTF(z) so that the bandwidth of the ADC can be further improved, and noise suppression capability is strengthened. The signal-to-noise and distortion ratio (SNDR) is improved by 5dB, which demonstrates very good agreement with the system-level simulation results from Fig.3.6. The performance comparison with other works is summarized in Table 3.1.

TABLE 3.1

Results and Comparison with Other Works

Parameters	➢This work	*[32]	➢[33]	➢[34]	➢[36]
Technology	180nm CMOS	40nm CMOS	----	180nm CMOS	65nm CMOS
Order	2	2	3	2	2
integrator phase error optimization	Yes	No	No	No	No
NTF zero optimization	Yes	No	No	No	No
ADC bits	14.56	13	10	16.88	13.2
bandwidth	1MHz	262KHz	100KHz	-----	2MHz
Fs (sampling frequency)	10MS/s	8.4MS/s	20MS/s	576MS/s	100MS/s
SNDR	89.4	80	99.7	104	81.2
Power(μW)	880	143	-----	------	561

➢ Simulation Results *Measurement Results

3.5. CONCLUSION

The paper proposed a novel high-speed SAR-ADC with 2nd-order noise shaping. The noise shaping technique is designed as a passive-active arrangement, utilizing a low-gain, open-loop amplifier with positive feedback. This implementation reduces the area required for passive integrator noise shaping and compensates for the gain and phase errors from passive implementation. A common-mode stabilization technique is proposed along with the monotonic switching technique, which prevents the common-mode level shift during SAR conversion and helps to improve the circuit's performance. The circuits simulation results in 180nm achieving an SNDR of 89.4 dB, an SFDR of 98.6 dB, and a THD of 0.0003%. The power consumed is 880 μW at a supply voltage of 1.8V.

CHAPTER 4 A HIGH BANDWIDTH-POWER EFFICIENCY, LOW THD[2,3] DRIVER AMPLIFIER WITH DUAL-LOOP ACTIVE FREQUENCY COMPENSATION FOR HIGH-SPEED APPLICATIONS

Ximing Fu [1], Kamal El-Sankary [1], Yadong Yin [2,]*

[1]Department of Electrical and Computer Engineering, Dalhousie University, Halifax B3H 4R2, Canada; xm954365@dal.ca (X.F.); kamal.el-sankary@ dal.ca (K.E.-S.)

[2]School of Physics and Information Engineering, Fuzhou University, Fuzhou 350002, Fujian, China; yinyadong@fzu.edu.cn

ABSTRACT

This paper presents a driver amplifier suitable for integration in 16-18-bit high speed ADCs, liquid crystal display (LCD) drivers, or other similar applications. The amplifier incorporates dual complementary differential pairs, which are classified as main and auxiliary transconductance amplifiers to obtain a full input voltage swing. A flipped voltage follower (FVF) buffer is applied as second stage to drive the class-AB output stage. Moreover, a dual loop active-feedback frequency compensation (DLAFC) dedicated to multi-stage amplifiers which are targeting the driving of wide dynamic range of capacitive loads is presented. As opposed to previous nested miller (NMC), reverse nested schemes (RNMC), the proposed DLAFC scheme can stabilize the proposed amplifier by pushing the dominant pole into very high frequencies to allow the proposed amplifier to achieve high frequency total harmonic distortion (THD) suppression. To achieve a wide dynamic load range for the proposed ADC driver, the phase margin loss from the second non-dominant pole is compensated by introducing one left half plane (LHP) zero to achieve low frequency phase margin protection (PMP). High frequency phase margin boosting (PMB) is achieved by injecting two LHP zeros without the need of large compensation capacitors and hence significantly increase the amplifier settling time and integration area. Therefore, wide gain–bandwidth product (GBW) of the DLAFC amplifier can also be achieved under better power-bandwidth conditions compared with conventional multistage-amplifiers. This proposed amplifier is implemented in a standard DBH 0.18-μm 5V CMOS process, and it achieves over 115-dB dc gain, 150-300-MHz GBW under 0-100p load capacitors, ultra-high THD2,3 suppression ranges from 100kHz to 10MHz under 1V-2V output swing, and over 250 V/μs average slew rate, by only dissipating 12.5 mW at 5 V power supply.

4.1 INTRODUCTION

Diver amplifiers are widely used in many industrial and measurement applications, such as high resolution (>16-bit) analog-to-digital converters (ADCs) [55]-[59]. Drivers for SAR ADCs as an example must drive the switched capacitor load presented by the ADC itself while maintaining distortion and noise levels that are lower than that of the ADC. This problem is particularly severe for a high-resolution ADC because its input capacitance must be large to have low noise
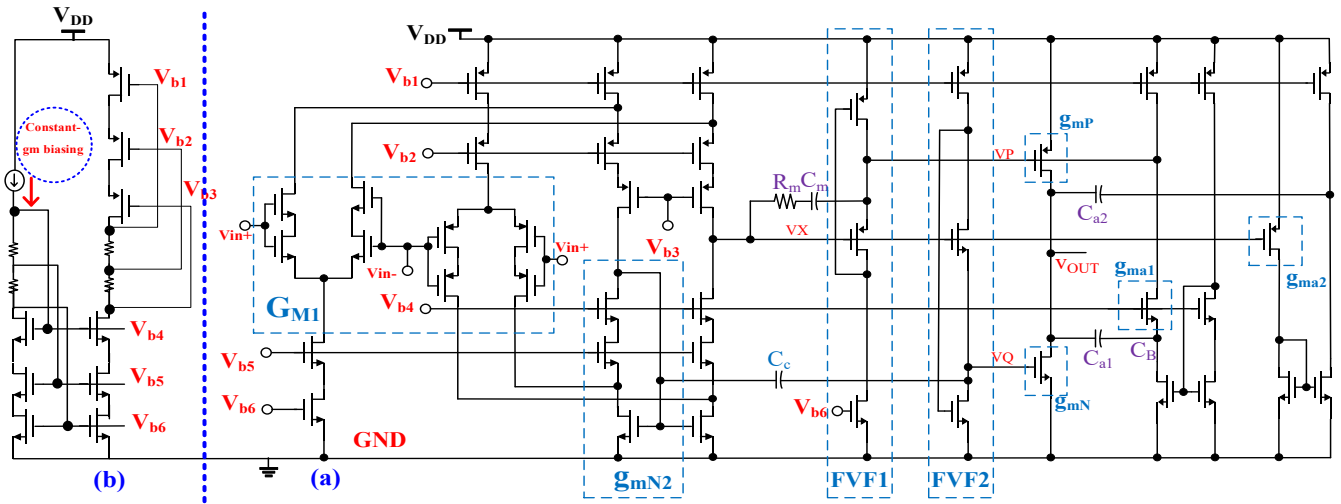
Fig 4.1. (a) Circuit implementation of the overall proposed driver amplifier and (b) biasing circuits.

and offset which brings the challenge and demand for the ADC driver amplifier design to drive wide range of capacitive load. High speed and high-resolution amplifiers design are not only applied in ADC field. With the advancement of liquid crystal display (LCD) drivers, there is a large demand for developing high-resolution and high color depth driver ICs [60]– [65]. LCD panels on multimedia products have become larger with higher definition, and their color quality requires more accuracy. For LCD-TV applications, the buffer amplifiers determine the speed, resolution, voltage swing, and power dissipation of the LCD drivers [61]– [64].

Multistage amplifier design has been proved to be very effective approach in driver amplifier design. As it is known， multistage amplifiers can be very power-efficient in driving a large capacitive load, and generally achieve a high bandwidth than single-stage amplifiers [66], [67]. The common challenge of multistage amplifiers is to achieve stability under wide range of load and high power-bandwidth efficiency. A three-stage amplifier has at least three high-impedance nodes, therefore, each contributes a pole. Without dedicated frequency compensation design could either easily place these poles at low frequency and cause stability problems or generating pole-splitting effect which would shrink the dominant pole to lower frequency and therefore reduce the bandwidth. In recent years, various frequency compensation techniques have been developed to ensure system stability， such as damping-factor-control frequency compensation (DFCFC) [66], active-feedback frequency-compensation (AFFC) [67], and nested/reversed Miller compensation (NMC, RNMC) [68], [69]. Most of these structures are derived from the nested Miller compensation (NMC). The major challenge of NMC is to maintain the balance between the complex-pole frequency and quality factor Q. In this work, the major contribution regarding

to the proposed DLAFC is it optimizes the complex conjugate poles by injecting two left half plane (LHP) zeros before the complex-pole frequency. Meanwhile, one extra LHP zero is generated to compensate for the negative phase shift caused by the non-dominant pole, which improves the phase margin protection. Finally, the proposed amplifier will have the resultant high unit gain frequency (ω_0), high total harmonic distortion (THD) suppression and fast settling time. This paper is organized as follows. In Section II, the detailed analysis in terms of architecture selection and proposed frequency compensation technique will be given for the proposed amplifier. In Section III, the simulations based on the proposed design and comparison table of state-of-art will be presented to validate the proposed design principles. In Section IV, the conclusion is drawn.

4.2 MULTISTAGE AMPLIFIER ARCHITECTURE

4.2.1 INPUT STAGE AND CLASS-AB OUTPUT STAGE
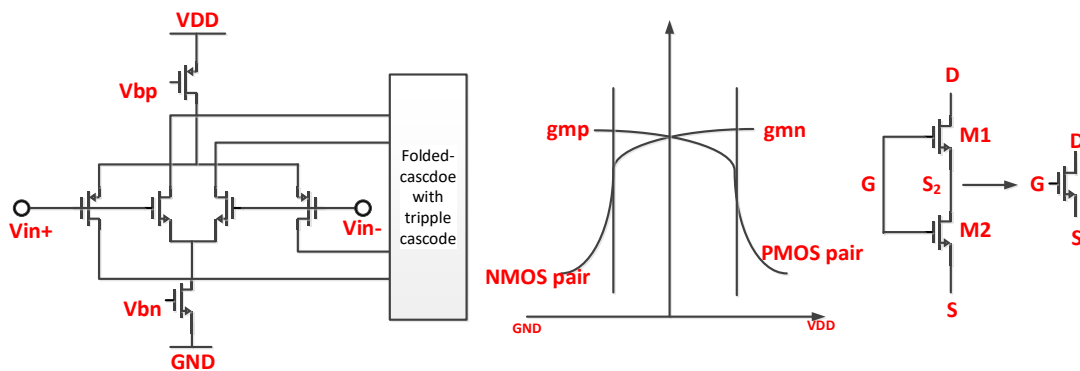
Fig 4.2 Rail-to-rail CMOS input stage with nMOS and pMOS differential pairs in parallel is adopted as input stage (a) Schematic. (b) Transconductance versus input common-mode range & self-cascode input transistors

The circuit's implementation shown in Figure.4.1 is proposed to prove the theoretical analysis and proposed amplifier design strategy. Due to the input voltage swing limitations, a traditional differential pair is not capable of processing signals with rail-to-rail common-mode levels. As shown in Figure. 4.2(a), a typical rail-to-rail CMOS input stage consists of an nMOS differential pair and a pMOS differential pair in parallel. When the input common-mode voltage is close to the positive (negative) power supply rail, only the n- (p-) channel input pair operates. When the input common-mode voltage is in mid-supply range, both pairs are active. Therefore, no matter where the input common-mode voltage is between the two supply rails, at least one differential pair remains active and contributes to the signal

amplification. It is worth to mention the first output stage is using triple cascode to achieve high DC gain rather than using regulated loop for gain boosting is because regulated loop will introduce more extra poles within the auxiliary amplifier which will create extra unnecessary difficulty and limitation on frequency compensation.

To further increase the input stage transconductance, the composite cascode structures are also referred as self-cascode structure is applied to replace with normal NMOS and PMOS transistors. The combination of the two transistors M1 and M2 shown in Fig. 4.2 is known as self-cascode input transistor technique. The ratio of channel width and length (W/L) of the transistor M2 is kept larger than M1, consequently, M2 will work in saturation region while M1 operates in triode region since the drain-source voltage of M1 in Fig. 4.2 (b) V_{S2}-V_S is smaller than its overdrive voltage. Therefore, the output resistance of the self-cascode transistors can be calculated as :

$$r_o = g_{m1}r_{o2}r_{o1} + r_{o1} + r_{o2} \tag{4-1}$$

Wherein g_{m2} and r_{o2} are the tranconductance and drain-source resistance of M2 respectively, r_{o1} is M1's drain-source resistance. Since M2 is in saturation region while M1 is in triode region, if the body effect of M2 is ignored, we can get that:

$$I_{M1} \cong \frac{1}{2}\beta_1(V_G - V_{s2} - V_{th1})^2 = \beta_2[(V_G - V_{th2})V_s - \frac{1}{2}V_s^2] \tag{4-2}$$

$$g_{m1} \cong \beta_1(V_G - V_{s2} - V_{th2}), \frac{1}{r_{o2}} = \beta_2[V_G - V_{th1} - V_s] \tag{4-3}$$

$$g_{m1}r_{o2} \approx \frac{(W/L)_1}{(W/L)_2} \tag{4-4}$$

Wherein $(W/L)_2$ and $(W/L)_1$ are the channel width and length ratios of M2 and M1 respectively. The output equivalent resistance of the self-cascode transistors can be rewritten as :

$$r_{oeq} = \left[\frac{(W/L)_1}{(W/L)_2} + 1\right]r_{o1} + r_{o2} \tag{4-5}$$

A push-pull class-AB output stage is often used as an output stage in CMOS buffer amplifiers. The push-pull stage consists of two complementary common-source transistors, allowing rail-to-rail output voltage swing. The gates of the two output transistors are normally driven by two in-phase ac signals separated by a dc voltage. The general purpose of driver amplifier is to buffer output which follows the

characteristics of the input signal with a large load. To achieve high THD suppression and therefore a class-A or class-B output stage will not be possible in terms of this application due to either their low AC efficiency or high distortion.

4.2.2 FLIPPED VOLTAGE FOLLOWER (FVF) BUFFER

Due to the final class-AB stage should be constructed with large transistors to supply large current. Among many existing topologies, flipped voltage follower (FVF) based amplifiers are an attractive topological choice to drive the output stage. The main advantage of the FVF is the reduced output impedance due to shunt feedback connection which is the key for obtaining fast transient response and minimal area requirements for implementing amplifiers for on chip applications. The schematic of a PMOS version of FVF is shown in Fig. 4.3(b). FVF consists of PMOS input transistor M_1 transistor with shunt feedback M_2 and bias-current-source transistor M_0.
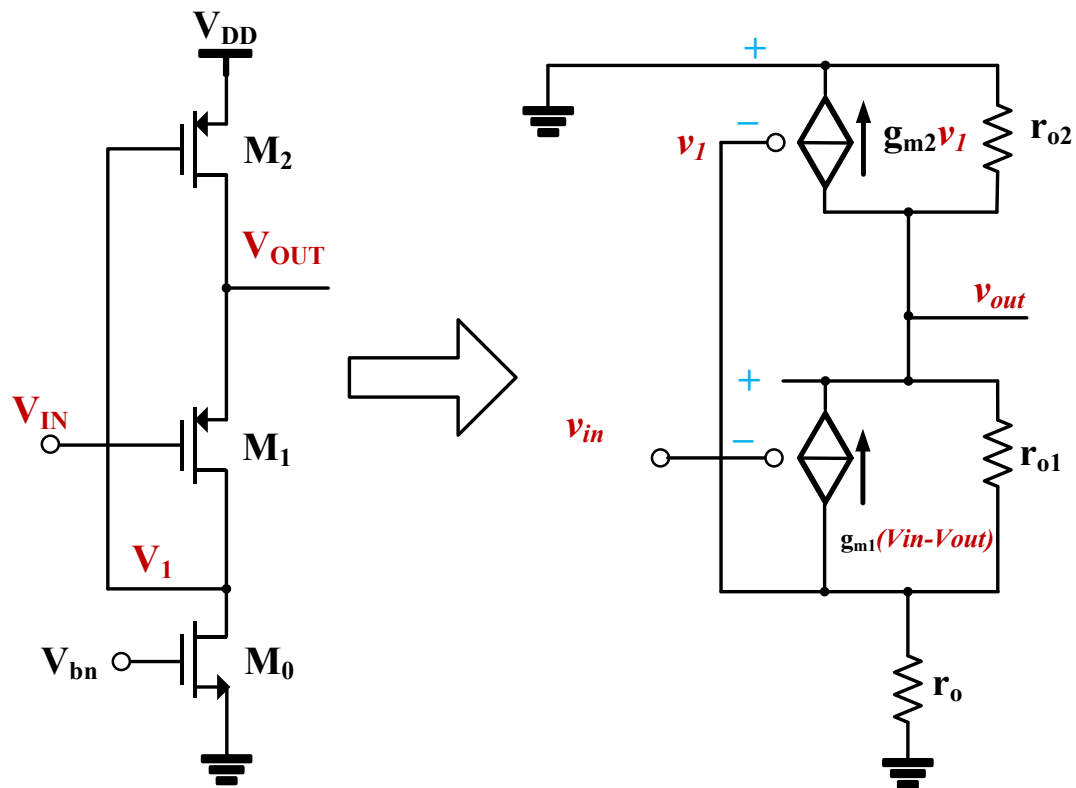
Fig 4.3 Voltage buffer topologies (a) common-drain source follower (b) flipped voltage follower buffer (c) output impendence calculation by breaking feedback network and apply testing voltage VT.

The output resistance of FVF buffer can be calculated as:

$$r_{FVF} = \frac{(r_o + r_{o1})r_{o2}}{(1 + g_{m1}r_{o1})(1 + g_{m2}r_o)r_{o2} + r_{o1} + r_o} \tag{4-6}$$

It is reasonable to assume that

$$g_{m1}r_{o1} \gg 1, g_{m2}r_o \gg 1$$

Therefore,

$$r_{FVF} \approx \frac{1}{g_{m1}g_{m2}\frac{r_{o1}r_o}{r_o+r_{o1}}} \tag{4-7}$$

4.2.3 PROPOSED DUAL-LOOP ACTIVE FREQUENCY COMPENSATION
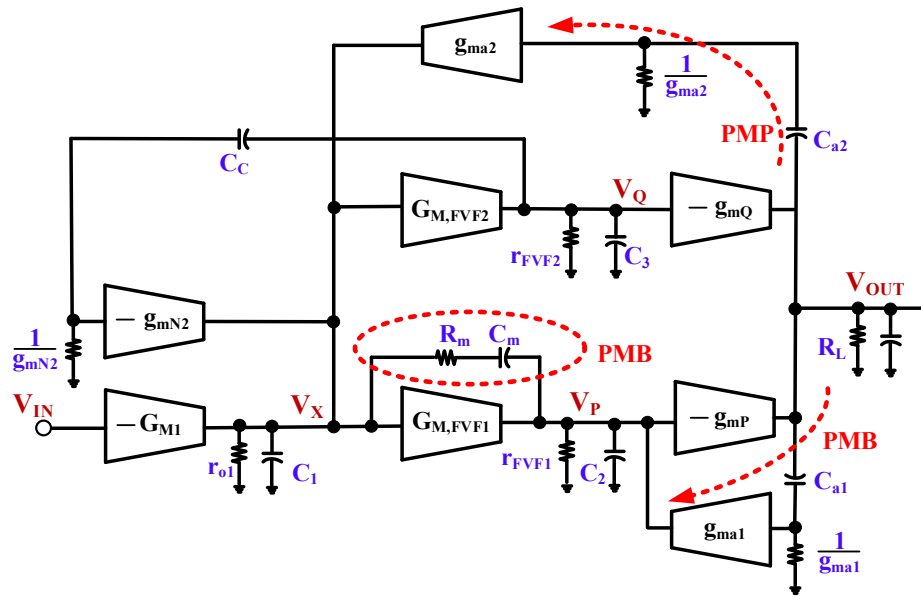
Fig 4.4 (a) Structure of the proposed DLAFC scheme
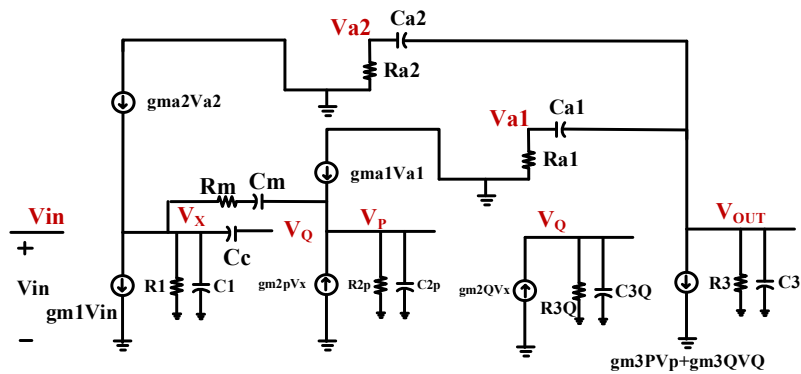
Fig 4.4 (b). Equivalent small-signal diagram of the proposed DLAFC amplifier

Figure. 4.4 (a) shows the structure of the proposed DLAFC for a three-stage amplifier, it consists of the two in-parallel signal path and two active feedback paths, namely (PMP and PMB). The amplifier dc gain is dominated by cascading gain stages A_{v1}, A_{v2}, and A_{v3} to achieve over 115 dB.(refer to Fig. 4.1) In the proposed design, the gain contribution is only related to A_{v1} and A_{v3}. Therefore, the dominant pole ω_{don} is occurred at the first stage while the non-dominant pole $\omega_{non-don}$ contributed by the last output stage because of the large capacitance load. The most important issue in driver amplifier is to maintain high bandwidth and high DC gain which can enhance the amplifier settling behavior and suppress THD respectively. However, due to the class-AB output stage simultaneously requires large transistor size and large supply current for high slew rate and large output swing, the non-dominant pole is very hard to move its own location. Hence a low frequency LHP zero ($z_1 = -\frac{gm_{a2}}{C_{a2}}$) is designed to compensate the phase loss and achieve phase margin protection (PMP) for the non-dominant pole is very necessary. Meanwhile, to achieve stability by mitigating the effect from the complex conjugate poles, two LHP zeros (z_{2-3}, one from Rm-Cm pair and other from current buffer $z_3 = -\frac{gm_{a1}}{C_{a1}+C_B}$) is generated to compensate the poles. It is important to realize that to protect the THD suppression and achieve high speed operation, the proposed DLAFC structure must prevent any direct connection between Miller capacitor from the output gain stage to first input gain stage (which refers to A_{v1} and A_{v3}). Therefore, the proposed DLAFC does not suffer from the bandwidth reduction caused by the Miller capacitive loading overhead at the amplifier output. The Amplifier uses the proposed DLAFC compensation network with the following key characteristic components:

(1) capacitor C_c is connected in current buffer configuration in the inner loop, the greatest advantage is to shift the dominant pole locations and without any pole splitting effect which protects the amplifier from PVT variations.

(2) Phase margin Boosting (PMB) is also introduced to achieve non-dominant pole compensation by creating 2 low frequency LHP zeros from the PMB feed-forward path. 1-pair of Miller capacitor C_m with nulling resistor R_m in parallel with $G_{M,FVF1}$ to effectively add 1-pole–zero pair to the inner loop. However, the extra pole (generated by capacitor C_m with nulling resistor R_m in the second stage) will not influence the amplifier stability because of the AFFC network connected between A_{v2} and A_{v3} in cascode frequency compensation to generate pole splitting to push this extra pole ω_{HF} into high frequencies. (Refer to the pole-zero placement relationship before and after compensation in Figure. 6) AFFC topology is adopted to reduce the value of C_c and push the dominant pole to higher frequency to achieve better THD+N in higher frequency. The major function of this RC pair is to effectively create

an extra zero along with the AFFC zero: $z_3 = -\frac{gm_{a1}}{C_{a1}+C_B}$ to achieve phase margin boosting (PMB) against the complex poles.

(3) Due to the phase margin loss from the second non-dominant pole, it is necessary to introduce an extra LHP zero to achieve low frequency phase margin protection (PMP). This is done through the PMP path which effectively add one more LHP zero ($z_1 = -\frac{gm_{a2}}{C_{a2}}$) to protect the phase margin.

The proposed DLAFC frequency compensation technique is to maintain high gain at the high frequency to achieve >16-bit resolution when the amplifier is in closed loop configuration. Based on the small signal model in Figure.5, The analysis will start from the transfer function of the proposed three-stage amplifier which can be characterized as

$$T(s) = \frac{A_{DC}(1+\frac{s}{z_1})(1+\frac{s}{z_2})(1+\frac{s}{z_3})}{(1+\frac{s}{\omega_{don}})(1+\frac{s}{\omega_{non-don}})(1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0})} \tag{4-8}$$

The small-signal model of the proposed DLAFC amplifier is shown in Figure. 4 (b). The small-signal transfer function should be investigated to analyze the stability of the DLAFC amplifier. The transfer function is derived under the assumptions of the capacitance C_1, C_2 C_3 , and are much smaller than C_c C_m and C_L. Given these assumptions, applying superposition theorem, the low-frequency gain and the dominant pole are given respectively.

As it is previously mentioned, the the extra pole influence (generated by capacitor C_m with nulling resistor R_m in the second stage) along with the proposed LHP zero z_2 will be analyzed from Fig. 4.5 in the following before the full analysis of the proposed DLAFC.
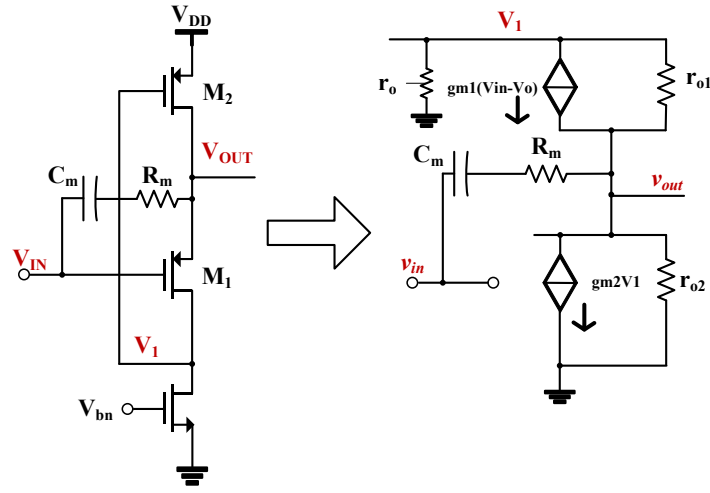
Fig 4.5 Equivalent small-signal diagram of the FVF buffer with proposed $R_m - C_m$ pair transfer function

$$g_{m1}(v_{in} - v_o) + \frac{V1 - Vo}{r_{o1}} + \frac{V1}{r_o} = 0 \tag{4-9}$$

$$g_{m2}v_1 + \frac{vo}{r_{o2}} = \frac{Vin - Vo}{Rm + \frac{1}{sCm}} + g_{m1}(Vin - Vo) + \frac{v1 - Vo}{r_{o1}} \tag{4-10}$$

Solving for the transfer function of Figure. 5 and the compensation zero z_2:

$$g_{m2}v_1 + \frac{vo}{r_{o2}} = \frac{Vin - Vo}{Rm + \frac{1}{sCm}} - \frac{V1}{r_o} \tag{4-11}$$

$$v_1 = -\frac{g_{m1}(Vin - Vo) - \frac{vo}{r_{o1}}}{\frac{1}{r_{o1}} + \frac{1}{r_o}} = -\frac{g_{m1}r_o r_{o1}(Vin - Vo) - Vo r_o}{r_o + r_{o1}} \tag{4-12}$$

Assume $r_o \approx r_{o1} \approx r_{o2}$

$$\left(-\frac{g_{m1}r_o r_{o1}(Vin - Vo) - Vo r_o}{r_o + r_{o1}}\right)\left(g_{m2} + \frac{1}{r_o}\right) + \frac{Vo}{ro2} = \frac{Vin - Vo}{Rm + \frac{1}{sCm}}$$

$$\left(-\frac{g_{m1}r_o r_{o1}v_{in}}{r_o + r_{o1}} + \frac{g_{m1}r_o r_{o1}Vo}{r_o + r_{o1}} + \frac{g_{m1}r_o r_{o1}Vo r_o}{r_o + r_{o1}}\right)\left(g_{m2} + \frac{1}{ro}\right) + \frac{Vo}{ro2} = \frac{Vin - Vo}{Rm + \frac{1}{sCm}}$$

$$-\frac{g_{m1}g_{m2}r_o v_{in}}{2} + \frac{g_{m1}g_{m2}r_o Vo}{2} + \frac{g_{m1}g_{m2}r_o^2 Vo}{2} + \frac{vo}{ro2} = \frac{Vin - Vo}{Rm + \frac{1}{sCm}} \quad \frac{v_{out}}{v_{in}} =$$

$$\frac{g_{m1}r_{o1}g_{m2}r_{o2}r_o}{g_{m1}r_{o1}g_{m2}r_{o2}r_o + r_{o1} + r_o} \frac{1 + sC_m\left(Rm + \frac{r_{o1} + r_o}{g_{m2}g_{m1}r_{o1}r_o}\right)}{1 + sC_m\left(Rm + \frac{r_{o1} + r_o}{g_{m1}r_{o1}g_{m2}r_o + \frac{r_{o1} + r_o}{r_{o2}}}\right)} \tag{4-13}$$

$$z_2 = -\frac{1}{C_m\left(R_m + \frac{r_{o1}+r_o}{g_{m2}g_{m1}r_{o1}r_o}\right)} \tag{4-14}$$

$$\omega_{extra} = -\frac{1}{C_m\left(R_m + \frac{r_{o1}+r_o}{g_{m1}r_{o1}g_{m2}r_o + \frac{r_{o1}+r_o}{r_{o2}}}\right)} \tag{4-15}$$

It is obvious that the z_2 and ω_{extra} are inevitably generated and the ω_{extra} must be removed in order to make the frequency compensation effective which only take advantage of the effect of z_2 rather than influenced by ω_{extra}.
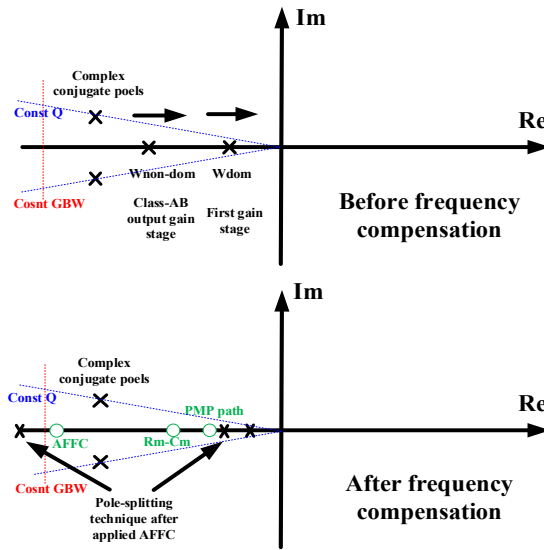
Fig 4.6. Diagram illustrating pole–zero locations.
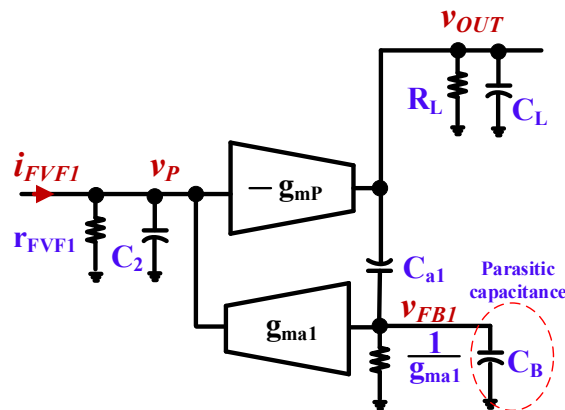
Fig 4.7. Cascode compensation due to AFFC to generating pole splitting effect to eliminate the one extra pole generated from Rm-Cm pair

The open-loop transfer function is

$$\begin{cases} (i_{FVF1} + g_{ma1}v_{FB1})\dfrac{r_{FVF1}}{1 + sC_2 r_{FVF1}} = v_P \\[3mm] -g_{mP}v_P\dfrac{\dfrac{R_L}{1 + sC_L R_L}\left(\dfrac{1}{g_{ma1}} + \dfrac{1}{sC_{a1}}\right)}{\dfrac{R_L}{1 + sC_L R_L} + \left(\dfrac{1}{g_{ma1}} + \dfrac{1}{sC_{a1}}\right)} = v_{OUT} \\[3mm] v_{FB1} = \dfrac{sC_{a1}}{sC_{a1} + g_{ma1}}v_{OUT} \end{cases}$$

$$v_P = -\frac{1}{g_{mP}}\frac{s^2 C_{a1}C_L R_L + s(C_L + C_{a1})g_{ma1}R_L + sC_{a1} + g_{ma1}}{sC_{a1}R_L + g_{ma1}R_L}v_{OUT}$$

$$\left(i_{FVF1} + g_{ma1}\frac{sC_{a1}}{sC_{a1} + g_{ma1}}v_{OUT}\right)\frac{r_{FVF1}}{1 + sC_2 r_{FVF1}}$$
$$= -\frac{1}{g_{mP}}\frac{s^2 C_{a1}C_L R_L + s(C_L + C_{a1})g_{ma1}R_L + sC_{a1} + g_{ma1}}{sC_{a1}R_L + g_{ma1}R_L}v_{OUT}$$

$$\frac{v_{OUT}}{i_{FVF1}}$$

$$= -\frac{g_{mP}r_{FVF1}R_L\left(1 + s\dfrac{C_{a1}}{g_{ma1}}\right)}{s^3\dfrac{C_{a1}}{g_{ma1}}C_L R_L C_2 r_{FVF1} + s^2\dfrac{C_{a1}}{g_{ma1}}C_2 r_{FVF1}\left[\dfrac{C_L R_L}{C_2 r_{FVF1}} + 1 + \left(\dfrac{C_L}{C_{a1}} + 1\right)R_L g_{ma1}\right] + sC_{a1}r_{FVF1}g_{mP}R_L + sC_{a1} + s(C_L + C_{a1})R_L + 1}$$

$$(4\text{-}16)$$

$$\omega_{don} = -\frac{1}{gm_2 R_2 (C_c + C_m) R_1} \tag{4-17}$$

$$A_{DC} = gm_1 R_1 gm_2 R_2 gm_3 R_3 \tag{4-18}$$

And one low frequency dominant LHP zero are given as:

$$z_1 = -\frac{gm_{a2}}{C_{a2}} \tag{4-19}$$

Two non-dominant high frequency zeros are given as:

$$z_2 = -\frac{1}{(C_c+C_m)R_m} \tag{4-20}$$

$$z_3 = -\frac{gm_{a1}}{C_{a1}+C_B} \tag{4-21}$$

Non-dominant pole and high frequency pole by pole splitting effect from AFFC shown in Figure 7 can be calculated from the derivations of cascode frequency compensation as follows:

$$\omega_{non-don} = -\frac{1}{A_{v3}R_2C_{a1}} = -\frac{1}{gm_3R_3R_2C_{a1}} \tag{4-22}$$

$$\omega_{HF} = -\frac{gm_3C_{a1}}{(C_{a1}+C_L)(C_p)} \text{---------(in GHz range very high frequency pole)} \tag{4-23}$$
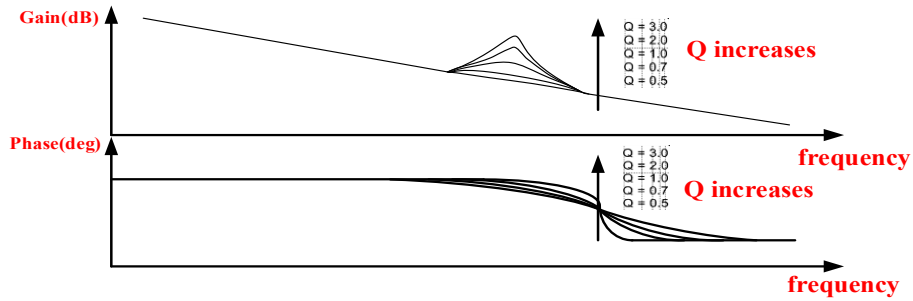
Fig 4.8 Voltage gain and phase shift corresponding to a pair of complex poles with different Q values.

The greatest advantage of the proposed technique compared with conventional simple miller compensation (SMC), cascode frequency compensation (CFC) or nested/ reversed miller (NMC, RNMC) compensation techniques is the proposed DLAFC is using pole-splitting effect in the unconventional way that between the second and third stage only to push the extra pole inevitably generated from the Rm-Cm pair outside the GBW. Thanks to the positive phase shift provided by z_{2-3}, the stability of the DLAFC amplifier can still be achieved even when the GBW is set to be closer to p_{1-2}. Therefore, the GBW of the DACFC amplifier can be improved by using the proposed pole-zero placement strategy shown in Figure 4.6 instead of using the third-order Butterworth response. As it is shown in Figure.4.8, The importance of the locations of the non-dominant complex pole pairs give rise to minor magnitude peaking, However, the effect on phase margin is mitigated by the presence of z_2 and z_3.

The designed complex conjugate poles are given as:

$$p_{1-2} = \sqrt{\frac{gm_2 gm_3 C_{a2}}{C_{a1} C_L}} \tag{4-24}$$

$$\varphi(p_{1-2}) = \sum_{i=1}^{2} arctan(\frac{\frac{\omega_{GBW}}{\omega_{cpi}}}{Q[1-(\frac{\omega_{GBW}}{\omega_{cpi}})^2]}) \tag{4-25}$$

$$p_{1-2} = 3 * GBW, Q = 0.502 \tag{4-26}$$

The reason for designing the Q-value of according to (24)-(26) can be understood using Figure.8 which shows the effect of a pair of non-dominant complex poles with different Q-values on the voltage gain and the phase shift of a generic three-stage amplifier. To avoid gain overshooting and dramatic phase reduction as shown in Figure. 8. Q-value of complex poles must be ensued to be smaller than 1. Therefore, the feature of having an additional positive phase shift due to two LHP zeros z_{2-3} creates an opportunity to achieve stability by using advanced pole-zero placement strategy. Due to the presence of two separate LHP zeros, the positive phase shift generated by z_{2-3} will cancel out the amount of the negative phase shift caused by p_{1-2} the non-dominant complex poles. The stability of the DLAFC amplifier is determined by its phase margin (PM) that is given as (17):

$$PM = 90 - arctan(\frac{\omega_{GBW}}{\omega_{p2}}) - \sum_{i=1}^{2} arctan(\frac{\frac{\omega_{GBW}}{\omega_{cpi}}}{Q[1-(\frac{\omega_{GBW}}{\omega_{cpi}})^2]}) + \sum_{i=1}^{3} arctan(\frac{\omega_{GBW}}{\omega_{zi}}) \tag{4-27}$$

4.3 SIMULATION RESULTS AND DISCUSSIONS

To verify the functionality of the proposed DLAFC based scheme driver amplifier design. The proposed prototype is implemented in 0.18-um DBH 5V technology process. The amplifier is expecting to drive maximum load less than 60pF including the probe capacitance. The first dominant pole is pushed around 5KHz to contain enough loop gain to suppress THD. Figure. 9 shows the frequency responses of the proposed amplifier with the loading of 10 pF and the poles and zeros from the previous analysis are labeled on the plot. It shows that under the propose delicate pole -zero placement, the phase margin of a multi-stage amplifier can be optimized to be approximately equal 90, the nominal GBW is around 250MHz. Fig. 4.10 shows the proposed diver amplifier can achieve very robust operation in all different corners under wide range of load capacitance. The simulated results for the proposed DLAFC amplifier are further verified with different capacitive loads to prove the robustness of the proposed design.

Fig.4.11 and Fig. 4.12 shows the proposed amplifier can achieve slew rate SR+- greater than 250V/us under small voltage swing and large voltage swing, meanwhile SR test can be also a good verification of the robustness of the proposed frequency compensation technique in this work. Fig.4.13 provides the frequency response under process variations, and it is clearly showing the proposed DLAFC is robust under most extreme corners. Fig. 4.14 and Fig. 4.15 shows the proposed amplifier can achieve THD suppression at high frequency operation (@1MHz and 8MHz) under large voltage swing 1 Vpp and 2 Vpp. Figure 4.16 and Figure 4.17 shows the extraordinary performance of input referred noise, PSRR and CMRR, output impedance under all different process corners to demonstrate the proposed circuits can maintain high immunity to power supply noise, common mode noise, and maintain low noise floor under high frequency operation. The ultra-low output impedance (less than 10 ohms) within 100MHz shows the proposed amplifier can have very powerful driving capacity without suffering from signal distortion. Overall, it is clear to show that the proposed design is robust in terms of the circuit's architecture, THD suppression and frequency compensation scheme.
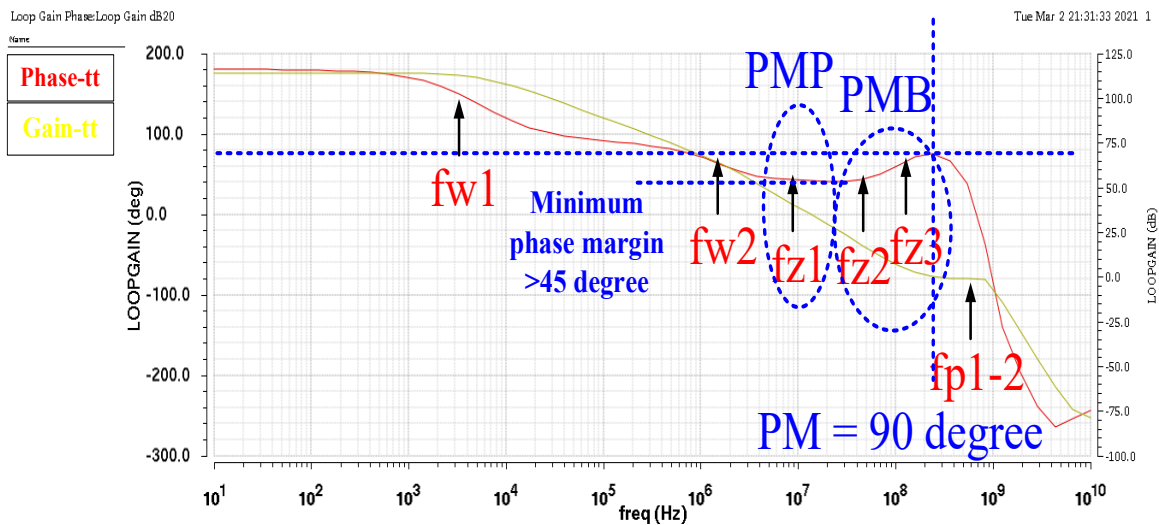
Fig 4.9. Simulated (a) gain and (b) phase responses of the DLAFC configuration.
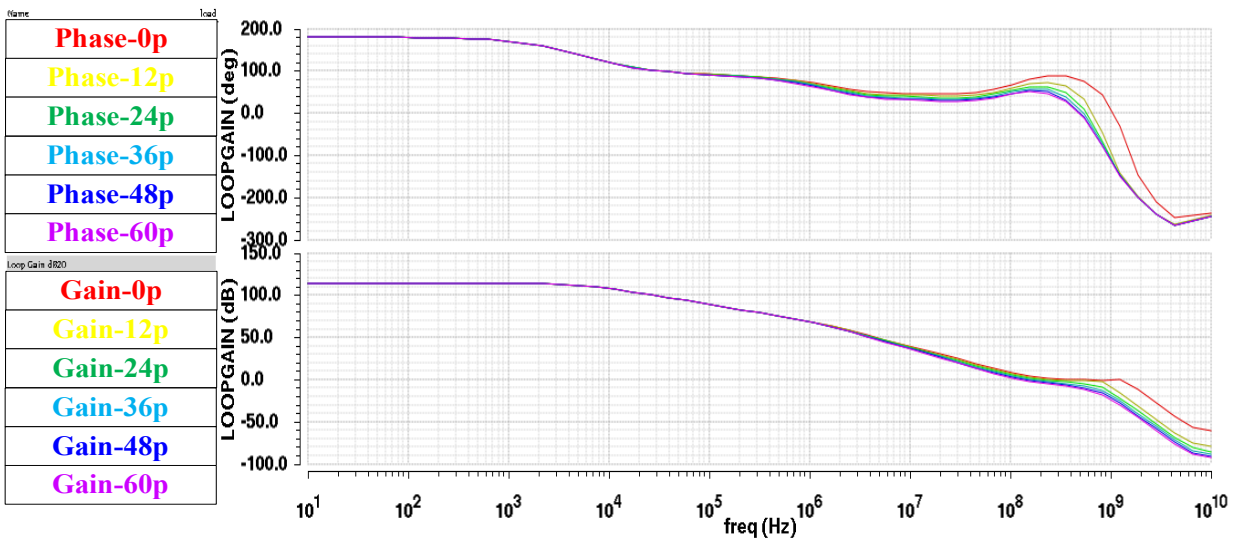
Fig 4.10. gain and phase responses under load variations between 0 - 60PF.
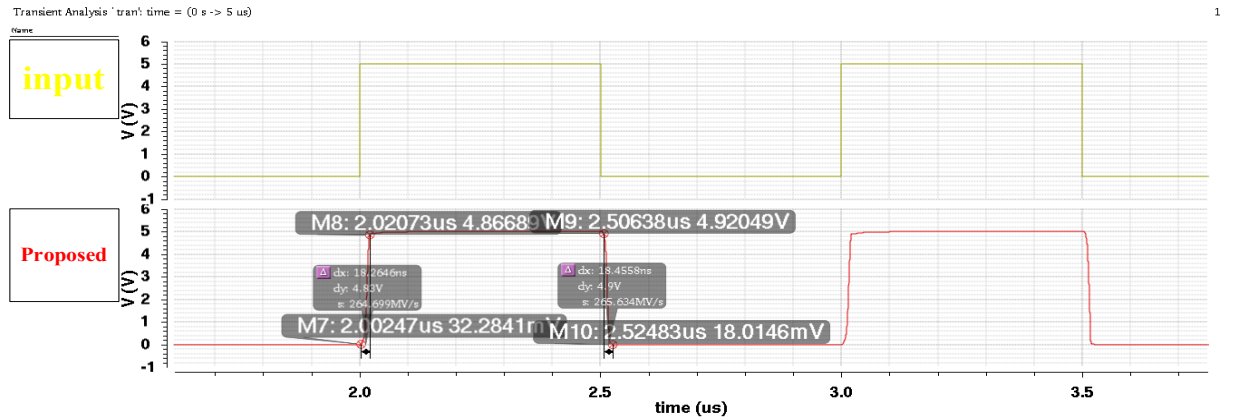
Fig 4.11. slew rate for large output swing of the proposed architecture in closed loop
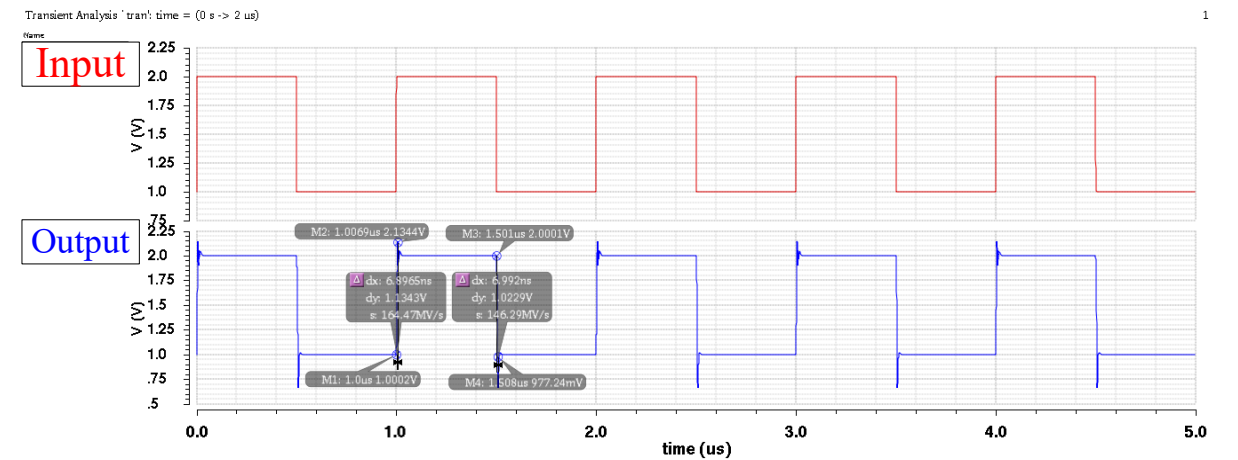
Fig 4.12. slew rate for small output swing of the proposed architecture in closed loop

88
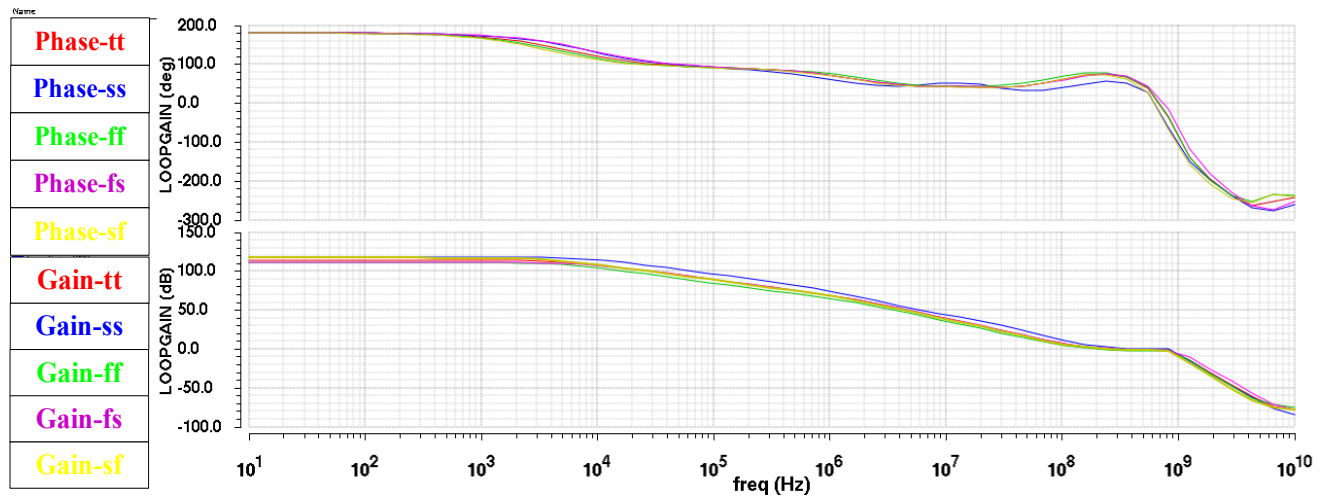
Fig 4.13 proposed OTA AC response under 5 different process corners.
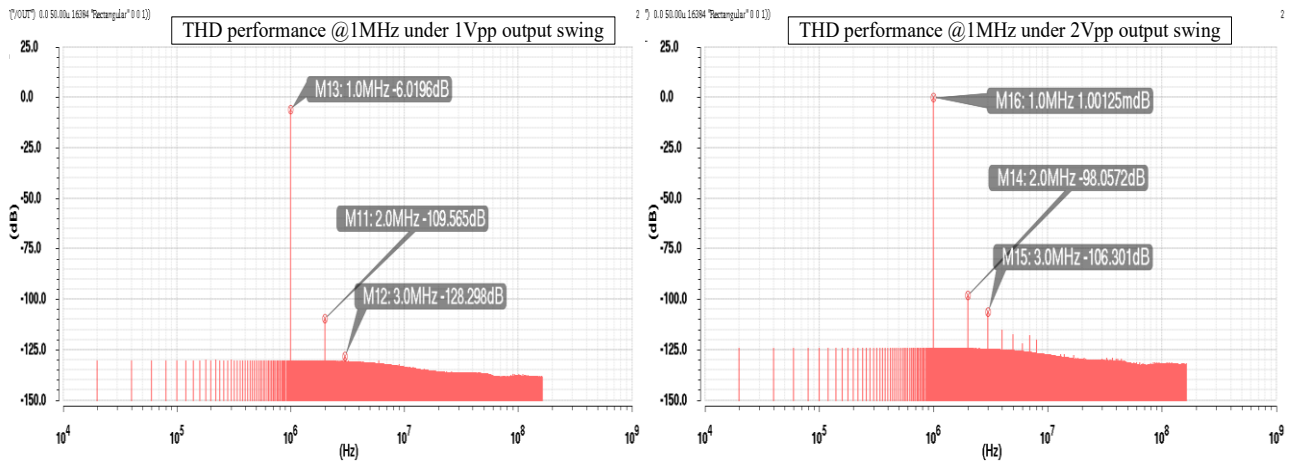
Fig 4.14 total harmonic distortion under 1V and 2V output swing operating at 1MHz.
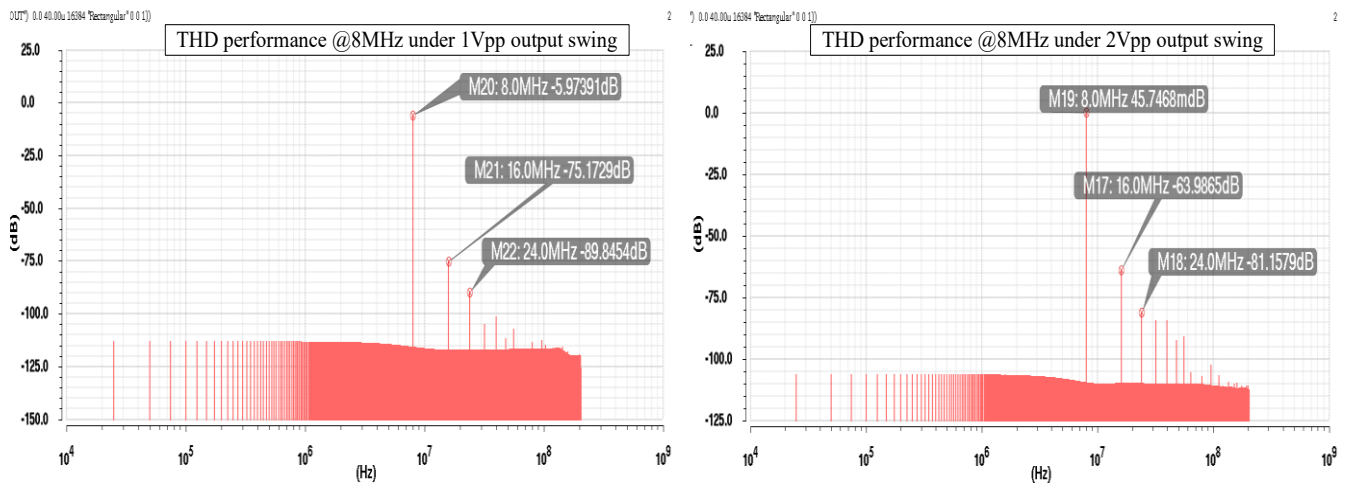
Fig 4.15 total harmonic distortion under 1V and 2V output swing operating at 8MHz.
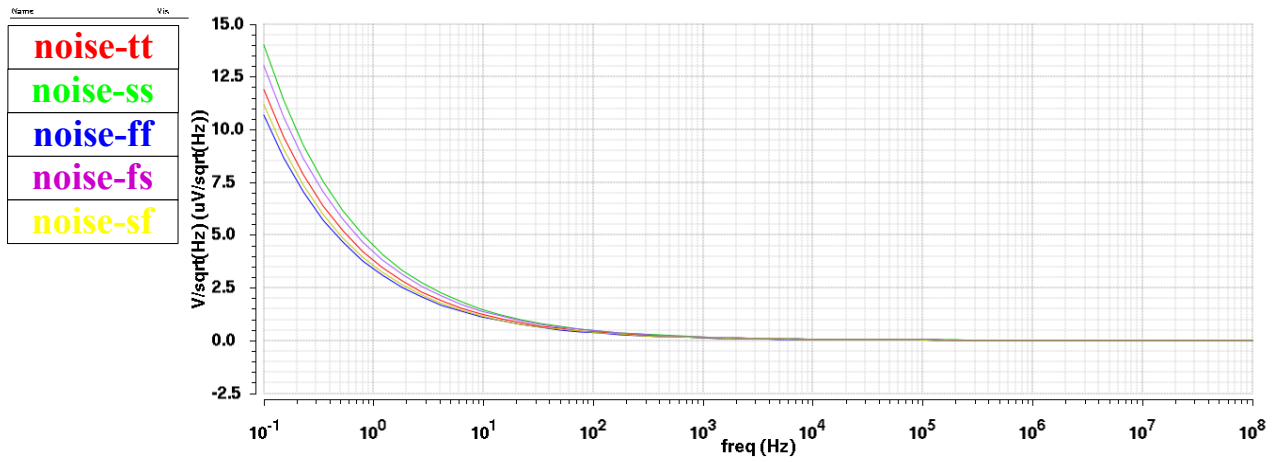
Fig 4.16 proposed OTA noise response under 5 different process corners.
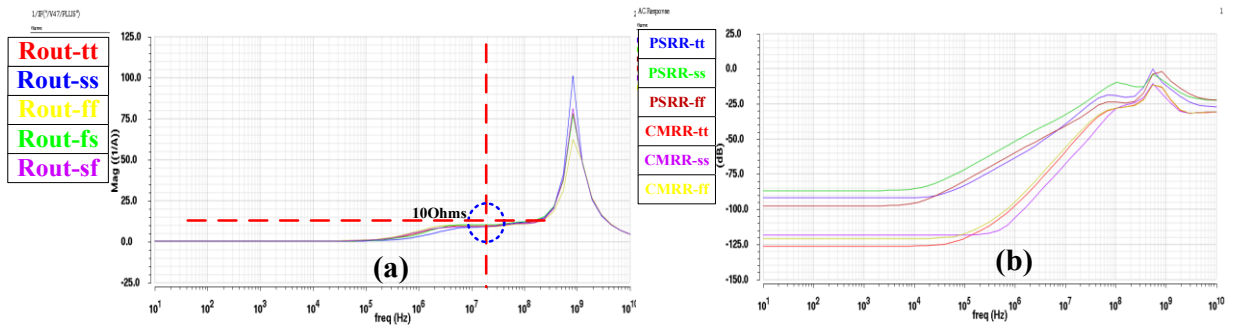
Fig 4.17 (a) Proposed ADC driver amplifier output impedance (b) PSRR & CMRR

Table 4.1. Performance table and comparison to the prior works.

Parameter	[1]This work	**[57]	**[58]	**[59]	**[60]
Technology	DBH-0.18um	Bipolar/BICMOS	Bipolar/BICMOS	Bipolar/BICMOS	0.18-BICMOS
Supply	5	5	5	5	3.3
Power(mW)	12.5mW	5.7mW	5mW	11mW	120.12mW
A0(dB)	115	70	45	33	97
GBW(MHz)	250	50	34	30	2200
SR (V/us)	265	490	45	22	
Input referred noise.	5nV/$\sqrt{Hz}$ @1MHz	5.7nV/$\sqrt{Hz}$ @1MHz	6.4nV/$\sqrt{Hz}$@ 1MHz	5.1nV/$\sqrt{Hz}$ @1MHz	1.67nV/$\sqrt{Hz}$ @1MHz
HD2,3 @ (1MHz output swing (1V, 2V)	16.5-bit 16-bit (-109/128) (-98/106)	HD2,3 at 10 kHz (dB) -133/140	HD2,3 at 10 kHz -106/-103	HD2,3 at 10 kHz (dB) -125/-126	HD2,3 at 10 kHz (dB) -74/-101
HD2,3 @ (8MHz) output swing (1V, 2V)	14-bit 13.5-bit (-75/-89) (-63/-81)				
Input offset(uV)	85	2000	200	360	-----------

1   Simulation results, others are from state-of-art products and publications.

4.4 CONCLUSION

In this paper, a DLAFC based driver amplifier is presented in this paper. The theoretical analysis and simulation results shows good agreement in terms of excellent DC gain, GBW, speed, input referred noise and THD which is suitable for high-speed applications. Moreover, the proposed amplifier is proven stable in most extreme PVT variations to validate the design robustness. The proposed amplifier has competitive performance compared with state-of-the-art amplifiers using as products.

CHAPTER 5 LOW NOISE, HIGH PSRR, HIGH-ORDER PIECEWISE CURVATURE COMPENSATED CMOS BANDGAP REFERENCE

Ximing Fu[1], Dalton Martini Colombo[2], Yadong Yin[3], and Kamal El-Sankary[1] Senior Member, IEEE
[1]Electrical and Computer Engineering, Dalhousie University, Halifax, NS, Canada
[2]Electrical Engineering Department, Federal University of Minas Gerais, Belo Horizonte, Brazil
[3]School of Physics and Information Engineering, Fuzhou University, Fujian, China

Corresponding author: Ximing Fu (e-mail: xm954365@dal.ca).

ABSTRACT

A Bandgap reference (BGR) circuit with a new high-order curvature-compensation technique is proposed in this paper. The curvature method operates by adding up two correction voltages. The first one is proportional to the difference in gate-source voltages of two MOS transistors (ΔV_{GS}) operating in weak inversion mode, while the second one (V_{NL}) is generated using a nonlinear current created by a piecewise-linear circuit. To improve the power supply rejection ratio (PSRR) and the line regulation performance, a low-power pre-regulator isolates the circuit power supply and BGR output. Additionally, the chopping technique reduces the output voltage noise and offset. Consequently, the overall PVT robustness of the proposed circuit is significantly improved. The circuit was implemented using a thick-oxide transistor in a standard 0.18 μm CMOS technology with a 3.3 V power supply voltage. The silicon results exhibit a temperature coefficient of 5-15 ppm/°C in the temperature range of $-10°C$ to $110°C$, whereas the simulated results demonstrate a similar performance within the temperature range of $-40°C$ to $150°C$. The supply current consumption is 150 μA, and the chip area is 0.56 x 0.8 mm^2. The measured peak noise at the output is 1.42 $\mu V/\sqrt{Hz}$ @320 Hz, the measured PSRR @ 1kHz is -80 dB, and the line regulation performance is 10 ppm/V, making the proposed circuit suitable for applications requiring low noise, high-order temperature compensation, and robust PVT performance.

5.1 INTRODUCTION

The voltage reference is essential for many analog and mixed-signal electronic devices. Such devices include data converters, power management controllers (LDOs and DC-DC converters), oscillators, and phase-locked loops that rely on voltage references that have low-temperature coefficient (T.C.) and high-power supply rejection ratio (PSRR). Moreover, high line/load regulation, low noise, and robustness against the impact of fabrication process effects are also highly desired. Most of these applications require high accuracy, resulting in challenging specifications for the voltage reference design.

The first 1st order temperature compensated BGR circuit was proposed by Widlar and Brokaw [70]-[71] in the 1970s. Due to the nonlinearities of voltage V_{BE} temperature compensation is usually limited to 30–100 ppm/°C for first-order temperature compensated references. Several high-order curvature correction compensation techniques have been proposed to overcome the temperature variations limitation of 1st order voltage references [72-78].

Among them are the quadratic temperature compensation [78], exponential temperature compensation [79], piecewise-linear curvature correction [80], [81], [84]-[89] and resistor temperature compensation [82-83]. The continuous-time feedback technique is employed in [84] to reduce noise and offset. The proposed BGR temperature coefficient compensation technique includes five pieces of linear compensation, including a buffer circuit, five V-I converters, and four current subtraction circuits, with an Opamp for each V-I converter. In [86], the adjusted piecewise temperature compensation circuit implements an accurate reference voltage with a good temperature coefficient over a wide temperature range. However, there are no essential techniques for mitigating Opamp noise, offset, and improving PSRR and line regulation performance. In [87], the curvature compensation current has been divided up into multiple parts for fine-tuning. This strategy may be a challenge regarding the stability of the loop. Moreover, the circuit requires multiple clock sequences to operate, resulting in additional (not for the BGR core) circuitry, signals, silicon area, and power consumption – which may be impossible for certain applications.

Besides an excellent temperature coefficient, another critical design specification for voltage references is the output noise at the BGR output. It means that the circuit must be designed to minimize the noise of the internal device (e.g., thermal and flicker noise) and mitigate the noise coming from the supply lines – which is quantified by the PSRR parameter. Furthermore, an excellent line-regulation performance is also demanded to protect the output voltage from DC supply voltage variations. Those mentioned performance parameters are especially important for modern SoC, including high-performance and high-resolution circuits.

One of the main techniques to enhance PSRR and line regulation is the inclusion of cascode or self-cascode structures [79]. Some other approaches have been developed to improve the PSRR of BGR, such as the supply independent current source technique [90]-[91], pseudo floating voltage source technique [92], and voltage follower technique with PMOS as input transistor [93].

To summarize the previous analysis, many previously mentioned techniques focus only on generally 1-2 aspects of design specifications for BGR references. In this work, we proposed a BGR topology that employs a new curvature correction method that employs existing methods in a different and optimized way. The temperature performance is achieved at the same time with other important specifications, such as low noise, PSRR, and line regulation. As a result, the proposed circuit is a good candidate for high-resolution and high-performance applications.

5.2 PROPOSED BGR: AN GENERAL VIEW
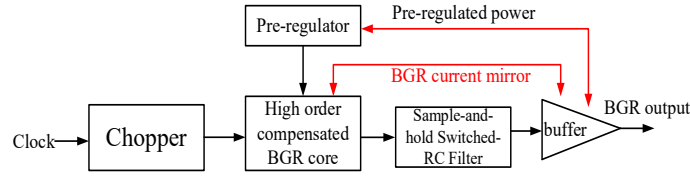
Fig 5.1. Block diagram of the proposed BGR system-level architecture.
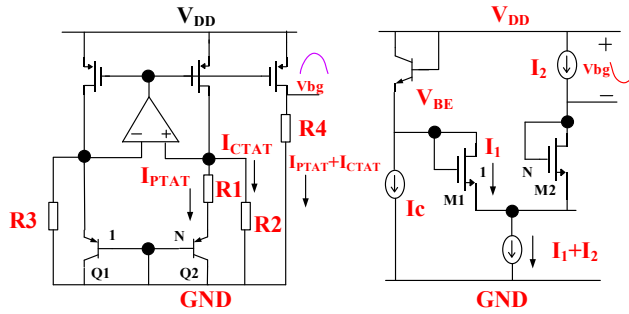
Fig 5.2. (a) 1st order BJT BGR (b) 1st order CMOS BGR [89]

Fig. 5.1 illustrates the system architecture of the proposed BGR. It consists of a non-overlapping clock with the chopper block, a pre-regulator to generate the isolated power supply to the BGR core, and an output buffer with a switched R-C filter. The proposed BGR can cancel high-order nonlinearities of the output voltage by adding two correction voltages at the output node. The first one, named ΔV_{GS} compensation, is generated using the difference of gate-source voltages of two MOS transistors operating in weak inversion mode. The second one, named V_{NL}, is generated using a piecewise nonlinear current compensation unit. These correction voltages have an opposite high-order temperature coefficient to those nonlinear terms generated by the BJT transistor employed in the majority of BGR architectures.

The proposed pre-regulator creates a shielding effect between the main power supply and the BGR output by generating an isolated and process/temperature-insensitive supply voltage for the BGR core. As a result, high PSRR and excellent line regulation are achieved. A low noise unity gain output buffer was included at the output node to drive a load current within 1-2 mA. The buffer is biased by the pre-regulator output voltage and was designed with a large area input transistor to reduce its offset voltage. Consequently, the offset voltage of the output buffer is negligible and does not degrade the temperature

performance of the BGR. Additionally, the chopping technique is employed in the BGR architecture to reduce the flicker (1/f) noise and the input offset of the Opamp, thus generating a precise and low noise output voltage. Finally, a sample-and-hold (S/H) switched-RC notch filter is included before the buffer output node to reduce the residual chopping ripple generated by the chopping technique.

This paper is organized as follows: Section 5.3 presents the operating principles of the proposed BGR, while its circuit topology is shown in Section 5.4. Section 5 focuses on the pre-regulator circuit design with offset and noise reduction by using the chopping technique. Section 5.6 shows the experimental results with the performance table summary and a comparison with the state-of-art works. Section 5.7 concludes the paper.

5.3 PROPOSED BGR: FUNDAMENTAL THEORY

As it is shown in Fig. 5.2(a), a standard 1st order BGR uses a bipolar transistor to generate a voltage that is, in the first order, complementary proportional to the absolute temperature (CTAT). Also, the difference between two base-emitter voltages (ΔV_{BE}) is used to generate a voltage proportional to the absolute temperature (PTAT). In Fig. 5.2(a), ΔV_{BE} and V_{BE} voltages are converted into two currents, I_{PTAT} and I_{CTAT}. In order to determine the reference output voltage, the sum of currents I$_{PTAT}$ and I$_{CTAT}$ is multiplied by the output resistance R4. The mathematical description of the temperature behavior of the output voltage shown in Fig. 5.2(a) is described by:

$$V_{ref} = V_{PTAT} + V_{CTAT} = \left(\frac{kT ln(N)}{qR1} + \frac{V_{EB1}}{R2,3}\right)R_4 \tag{5-1}$$

$$V_{EB}(T) = V_{G0}(T_R) - (V_{G0}(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta - \delta)V_T ln\left(\frac{T}{T_R}\right) \tag{5-2}$$

$$V_G(T) = V_{G0} - bT - cT^2 \tag{5-3}$$

In equation (5-2), $V_{G0}(T_R)$ is the bandgap voltage at the reference temperature T_R, T_R is the reference temperature, η depends on the structure of NPN or PNP and is a constant, which is approximately about 3.54. Parameter δ is the order of the temperature dependence of the collector current. Where V_{G0} is

1.17885 V to 1.20595 V, b is 9.025×10⁻⁵V/K to 2.7325×10⁻⁴ V/K, c is 3.05×10⁻⁷ V/K² to 0 if the temperature is in the range of 150 K (-123 °C) to 400 K (127 °C) [28]. Note that they are positive constants. When the collector's current . of the PNP transistor increases linearly with temperature T, $\delta=1$; but when it is not related to the temperature T, $\delta=0$. In equation (2), $(V_{G0}(T_R) - V_{EB}(T_R))\frac{T}{T_R}$ is the first-order temperature-dependent part, and $(\eta - \delta)V_T ln(\frac{T}{T_R})$ is the high-order nonlinearity. Due to the higher-order nonlinearities from the V_{EB} shown in equations (2)-(3), the temperature compensation is limited for the 1st order BGRs. By grouping the nonlinear terms inserted by V_{EB} (equation 5-2) into equation 5-1, $V_{ref\_nonlinear}$ can be written as:

$$V_{ref\_nonlinear} \approx \frac{R4}{R2}V_{EB1}(T) \approx \frac{R4}{R2}[f(T)] \tag{5-4}$$

$$f(T) = -cT^2 - (\eta - 1)\frac{kT}{q}ln\left(\frac{T}{T_R}\right) \tag{5-5}$$

Equation $f(T)$ details the high order terms of (5-4). Taking the simplified Taylor series expansion of the term ln(T) at T_R Equation (5-5) can be rewritten as (5-6):

$$ln(T) \approx (T - 1) - \frac{(T - 1)^2}{2} + \frac{(T - 1)^3}{3} - \frac{(T - 1)^4}{4}\dots\dots$$

$$f(T) \approx \left[-c - 2(\eta - 1)\frac{k}{qT_R}\right]T^2 + (\eta - 1)\frac{k}{2qT_R^2}T^3 \tag{5-6}$$

Note also that the second-order term $[-c - 2(\eta - 1)\frac{k}{qT_R}]T^2$ has a negative sign, and therefore, it explains the main reason for the limited temperature compensation and the concave down parabola curve of a 1ˢᵗ BJT BGR.

To get a lower temperature coefficient reference voltage for high-resolution applications, a typical 2ⁿᵈ order compensation, namely exponential curvature compensation for $V_{EB}(T)$ is applied as it is shown in Fig. 5.3. The emitter-base voltages V_{EB}(T) of Q1 and Q3 can be written as the following:

$$V_{EB3}(T) = V_G(T) - (V_G(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta)V_T ln(\frac{T}{T_R}) \qquad (5\text{-}7)$$

$$V_{EB1}(T) = V_G(T) - (V_G(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta - 1)V_T ln(\frac{T}{T_R}) \qquad (5\text{-}8)$$

The emitter current flows from Q3 is approximately temperature independent ($\delta = 0$), while the emitter current from Q1 has a positive temperature dependence ($\delta = 1$). Thus, the difference between these voltages, $\Delta V_{EB1,3}$, is nonlinear and can be written as follows:

$$\Delta V_{EB1,3} = V_{EB1}(T) - V_{EB3}(T) = \frac{kT}{q} ln\left(\frac{T}{T_R}\right) = V_{cmp} \qquad (5\text{-}9)$$

As a consequence, the output voltage of the circuit in Fig. 5.3 becomes:

$$V_{bg} = R_6(\frac{\Delta V_{EB1,2}}{R_2} + \frac{V_{EB1}}{R_3} + \frac{\Delta V_{EB1,3}}{R_4}) = \frac{R_6}{R_3} (\frac{R_3}{R_2}\Delta V_{EB1,2} + V_{EB1} + \frac{R_3}{R_4}V_{cmp}) \qquad (5\text{-}10)$$
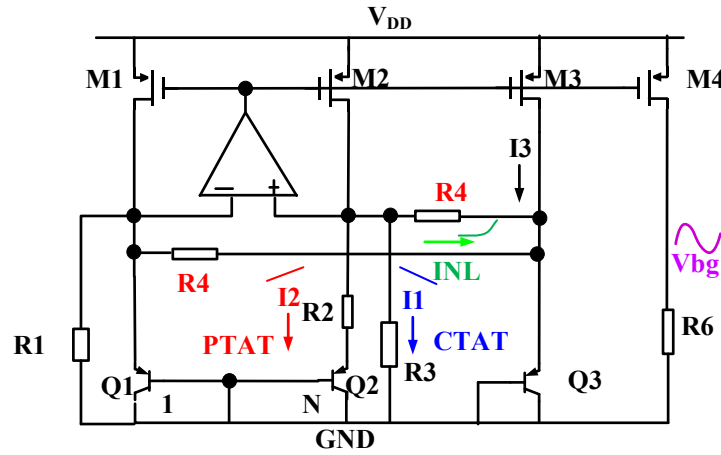
Fig 5.3. Conventional 2nd order exponential compensated BGR [90]

Where, $\Delta V_{EB1,3}$ is a nonlinear voltage with a positive temperature coefficient, and it can be used to compensate for the transistor emitter-base voltage nonlinear temperature-dependent term in V_{EB} described by (6), as long as $\frac{R_3}{R_4} = \eta - 1$. The compensation is done by satisfying the following equation:

$$\frac{R_6}{R_3}\left(\left[-c - 2(\eta - 1)\frac{k}{qT_R}\right]T^2\right) + \frac{R_6}{R_4}V_{cmp} \approx 0 \tag{5-11}$$

However, since V_{cmp} ($\Delta V_{EB1,3}$) is a curvature compensation voltage; it is more susceptible to the effects of the fabrication process. Referring again to the circuit of Fig. 5.3, since a second-order exponential voltage is added to the output voltage equation, the temperature dependency of the output becomes similar to an approximately "sinusoidal" curvature corrected shape instead of a concave down parabola. As a result, a reduced and better TC is achieved. However, the compensation voltage increases dramatically with the temperature increase and may be problematic if not restricted to a specific temperature range. This approach may not be adequate for BGR operating in extended temperature ranges. The proposed BGR architecture also solves this limitation by generating a correction current for a specific range of low temperatures using a piecewise compensation unit. An alternative way to generate the PTAT voltage is by using the difference of gate-source voltage difference (ΔV_{GS}) between two MOSFETs operating in weak inversion mode. Fig. 5.2(b) is an example of architecture that employs this strategy. The output voltage of this circuit is described by (5-12). The only difference between (5-1) and (5-12) is the way to generate the PTAT voltage. The proposed BGR architecture also generates a PTAT voltage using ΔV_{GS} as part of the proposed higher-order temperature compensation, as explained in the following section.

$$V_o = V_{BE} + \Delta V_{GS} = V_{BE} + \frac{nkT}{q}ln\left(\frac{I_{D1}(\frac{W}{L})_2}{I_{D2}(\frac{W}{L})_1}\right) \tag{5-12}$$

5.4 PROPOSED HIGH ORDER COMPENSATION BANDGAP

The proposed high-order temperature-compensated bandgap reference employs two correction voltages: ΔV_{GS} and V_{NL}. The first is used for a high-temperature range, and the last is used for a low-temperature range. Figures 5.4 (a)-(e) demonstrate the simulated step-by-step process to achieve the temperature compensation and its mechanisms. In the sub-sections, it will be explained how these voltages are generated.

5.4.1 GENERATION OF THE CORRECTION VOLTAGE: ΔV_{GS} VOLTAGE

Many studies have been conducted on the weak inversion region for MOSFETs [7] - [9]. Equation (5-13) for the drain current of N-channel MOS (NMOS) operating in a weak inversion region can be written as:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (\frac{nkT}{q})^2 exp^{\frac{q}{nkT}(V_{GS}-V_{th})} (1 - exp^{-\frac{qV_{DS}}{nkT}}) \tag{5-13}$$

Under the condition of $V_{DS} >> \frac{kT}{q}$, equation (13) can be simplified as equation (5-14):

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (\frac{nkT}{q})^2 exp^{\frac{q}{nkT}(V_{GS}-V_{th})} \tag{5-14}$$

Rewritten and isolating V_{GS}:

$$V_{GS} = V_{th} + \frac{nkT}{q} ln \frac{I_D}{\mu_n C_{ox} \frac{W}{L}(\frac{nkT}{q})^2} \tag{5-15}$$

Therefore ΔV_{GS} can be solved as:

$$\Delta V_{GS} = \frac{nkT}{q} ln(\frac{I_{D4}(\frac{W}{L})_5}{I_{D5}(\frac{W}{L})_4}) \approx \frac{nkT}{q} ln(N) \tag{5-16}$$

where V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, V_{DS} is the drain-source voltage, C_{ox} is the oxide capacitance per unit area, μ_n is the effective mobility of carriers in the channel, W is the gate width, and L is the gate length. Equation (5-16) would be ideally linear with temperature without the parameter "n". This parameter is a function of temperature, and it is one of the limitations of the first-order temperature compensation of BGRs that employ MOSFET in weak inversion mode [10]. According to Tsividis and Ulmer [70]-[71], the temperature dependence of "n" can be modeled as $n = E + FT + GT^2$, where E, F, and G are positive constants. Consider Fig. 5.5 and substituting n(T) into (5-16), and assuming $\frac{I_{D4}(\frac{W}{L})_5}{I_{D5}(\frac{W}{L})_4} = a$, for a > 1, the difference ΔV_{GS} can be rewritten as:

(a)

1st order BGR

(b)

M1: 30.11C 1.161329V

1st order BGR with ΔV_{GS} compensation

dx: 81.814C
dy: 1.67716048mV
s: 20.4996759uV/C

M2: 111.924C 1.159652V

(c)

M1: -40.0C 1.15081V

dx: 20.58333C
dy: 1.67913511mV
s: 81.5774142uV/C

Non-linear-current compensation
under different tripping point
temperature

M2: -19.41667C 1.149131V
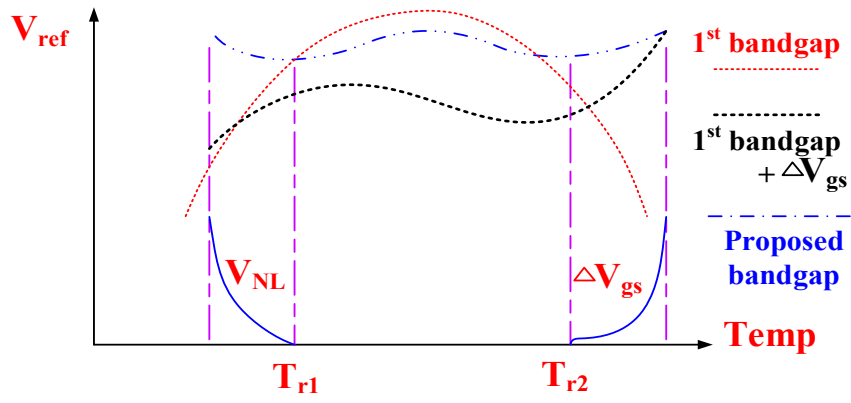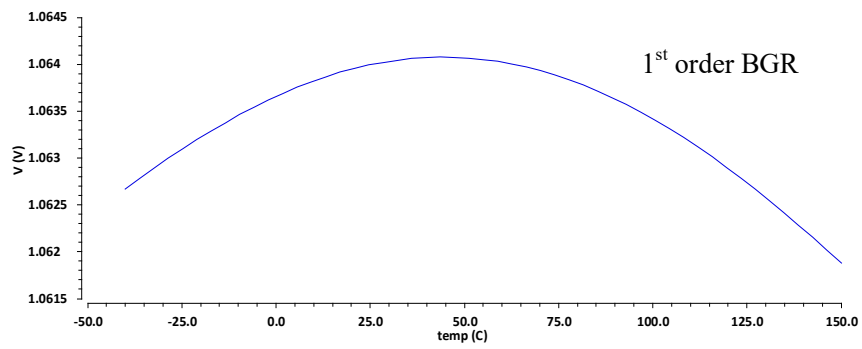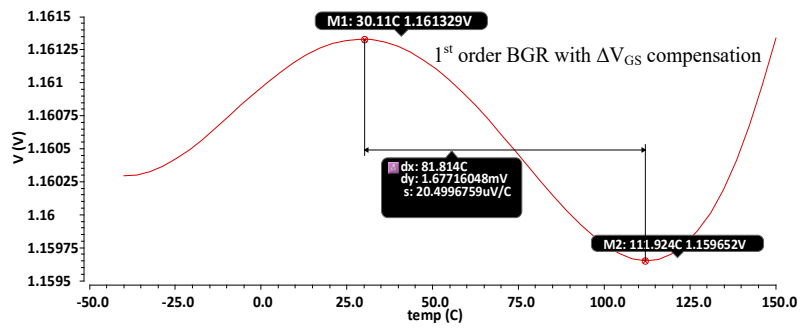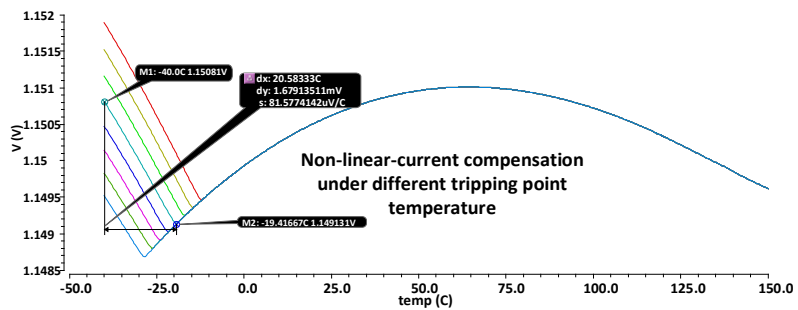
(d)
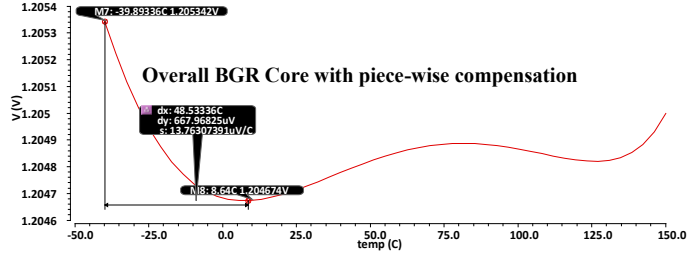
(e)

Fig 5.4. (a). The proposed curvature compensation main principle. (b) conventional 1st order BJT BGR (c) 2nd order temperature compensation with ΔV_{GS} compensation (d) temperature compensation in addition to nonlinear current compensation unit (e) temperature coefficient compensation for overall BGR Core Circuit
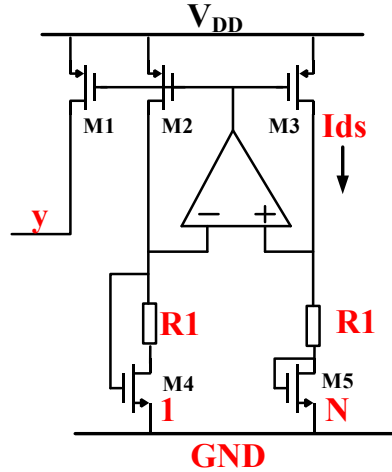
Fig 5.5. ΔV_{GS} compensation unit for the proposed BGR

$$\Delta V_{GS} = \frac{EkT}{q}ln(a) + \frac{FkT^2}{q}ln(a) + \frac{GkT^3}{q}ln(a) \tag{5-17}$$

If ΔV_{GS} is converted to a current and injected on two resistors in series (R4 and R5, shown in Fig.5.7), the correction voltage becomes Equation (5-18):

$$V_{MOS}(T) = \frac{kT}{q}\frac{R4+R5}{R0}k_6ln\,(k_7)(E + FT + GT^2) \tag{5-18}$$

The coefficients of the second-order term of (18) are positive. The previous analysis shows that MOS/BGR and BJT/BGR have inverse second-order temperature coefficients. In summary: (i) ΔV_{EB} voltage has a positive first-order coefficient, (ii) V_{EB} voltage has first-order, second-order, and third-order coefficients, all negative, and (iii) the temperature coefficients of the first, second, and third-order of ΔV_{GS} are all positive. Therefore, if both second-order temperature coefficient terms can be added through appropriate weights, high-order temperature compensation can be performed, and an improved BGR with a reduced temperature coefficient is achieved. Combining the output voltage of a first-order BGR and a voltage generated by ΔV_{GS} current, (5-19) is written.

$$V_{sum} = V_{PTAT} + V_{CTAT} + V_{MOS}(T) \tag{5-19}$$

As mentioned before, the third term of the above equation increases rapidly with the temperature, and thus, it should be restricted to a specific and short temperature range. It can be used, for instance, at high temperatures to compensate for the traditional

output voltage reduction caused by the non-linearities of V_{EB}. For low temperatures and a reduced range, a nonlinear current compensation, named as V_{NL}, generated by a piecewise-linear circuit is employed, as discussed in sub-section B.

5.4.2 GENERATION OF THE CORRECTION VOLTAGE: V_{NL} VOLTAGE

Voltage V_{NL} can be used to mitigate the reduction of the output voltage of the typical BGR. The generation of the nonlinear current compensation for low temperatures, as illustrated in Fig. 5.4, can be performed by the circuit shown in Fig. 5.6. Now consider currents I_{PTAT} and I_{CTAT} as given below:

$$I_{CTAT} = \beta_1 \frac{V_{EB}}{R2} \text{ and } I_{PTAT} = \beta_2 V_T \frac{ln(N)}{R1} \tag{5-20}$$

Where β_1 and β_2 are the gains of current mirrors formed by any 1st order BJT BGR, respectively. From Fig. 5.6 and Fig. 5.7, consider that I_{CTAT} is from M24 and I_{PTAT} is from M25 for both nonlinear current compensation cells 1 and 2. The tripping point temperature $T_{r1}, T_{r2} \in (\sim -20\ ^\circ\text{C} -0\ ^\circ\text{C})$ is designed by simulation optimization, where there is a temperature compensation between I_{CTAT} and I_{PTAT}, such as

$I_{CTAT} = I_{PTAT}$. Therefore, when $T > T_{r1}$, $I_{CTAT} < I_{PTAT}$ and then $I_{NL} = 0$. But for $T < T_{r1}$, $I_{CTAT} > I_{PTAT}$, and $I_{NL} = I_{CTAT} - I_{PTAT}$. The current flowing in M$_{26-27}$ can be written as:

$$I_{M26-27} = \begin{cases} \left(\beta_1 * \dfrac{VEB1}{R2} - \beta_2 * \dfrac{kTln(N)}{qR1}\right), & T < Tr1 \\ 0 & T > Tr1 \end{cases} \tag{5-21}$$

The output voltage Vref can be high-order temperature compensated for by injecting a piecewise-linear compensation current into the node "X," where there is a resistor called R5 connected. The compensation voltage VNL is then given by:

$$VNL1 = \begin{cases} R5 * k3 \left(k1 * \dfrac{VEB1}{R2} - k2 * \dfrac{kTln(N)}{qR1}\right), & T < Tr1 \\ 0 & T > Tr1 \end{cases} \tag{5-22}$$

$$VNL2 = \begin{cases} R5 * k5 \left(k1 * \dfrac{VEB1}{R2} - k4 * \dfrac{kTln(N)}{qR1}\right), & T < Tr2 \\ 0 & T > Tr2 \end{cases} \tag{5-23}$$

To further optimize the temperature coefficient, the nonlinear current unit cell is repeatedly used twice to provide more freedom in terms of optimization.

5.4.3 COMPLETE CIRCUIT

The proposed bandgap reference voltage can be written as follows:

$$V_{ref} = V_{1st\,roder} + \Delta V_{GS} + V_{NL1-2} \tag{5-24}$$

The complete circuit shown in Fig. 5.7 contains the sub-circuits of figures 5 and 6 and implements equation (5-24). Its circuit topology is shown in figure 5.7. The resistor ratio between R3, R4, and R5 was designed to be 1:1:1. Note the node "X" and "Y", where the correction voltages are injected.

5.4.4 MONTE CARLO SIMULATION

The temperature performance of the proposed BGR was simulated over the fabrication process corners and using Monte Carlo Analysis, including process and mismatch variations, for 200 samples. Fig.5.8(a) presents simulated TCs for different MOSFET corners. The maximum variation in this simulation is 1.5 mV over the temperature range of -40 ^{o}C to 150 ^{o}C. The simulated results indicate that the process variation does not severely affect the reference voltage, and the proposed TC compensation robustness is guaranteed.

The Offset voltage Monte Carlo simulation is shown in Fig. 5.8(b). The BGR presents a worst-case scenario with a TC of 5-15 ppm/°C. Its average mean value is 11.83 ppm/°C. Figure 5.8(c) presents the histogram of TC with its average and standard deviation value.
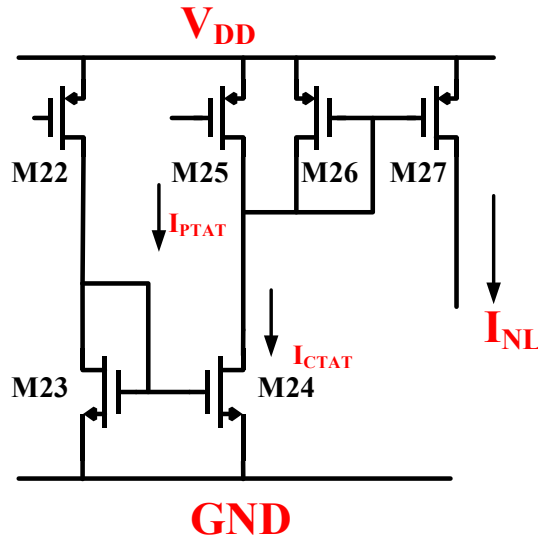
Fig 5.6. nonlinear current compensation unit for the proposed BGR
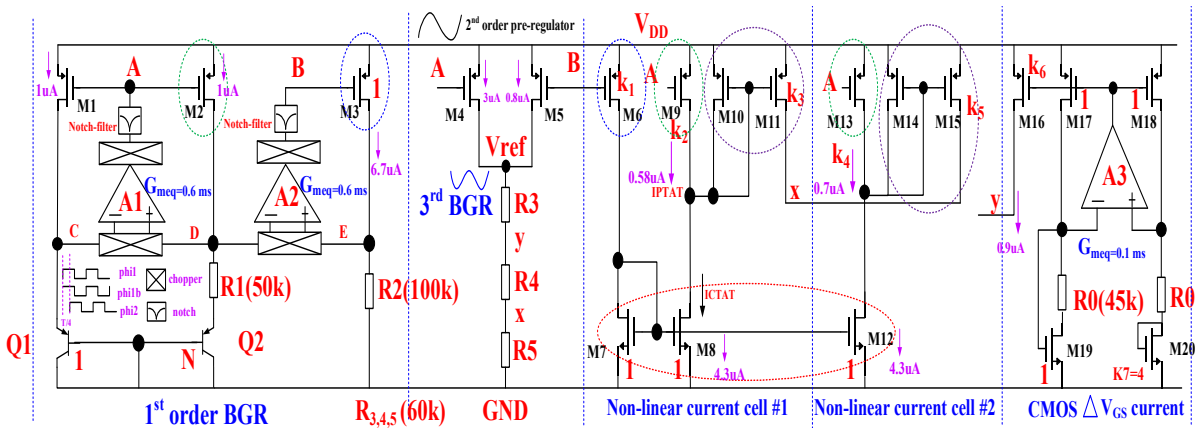
Fig 5.7. Overall BGR Core Circuit implementation

(a)

Simulated curvature compensation BGR under 200-point MC @ TT Corner

(b)

(c)

106
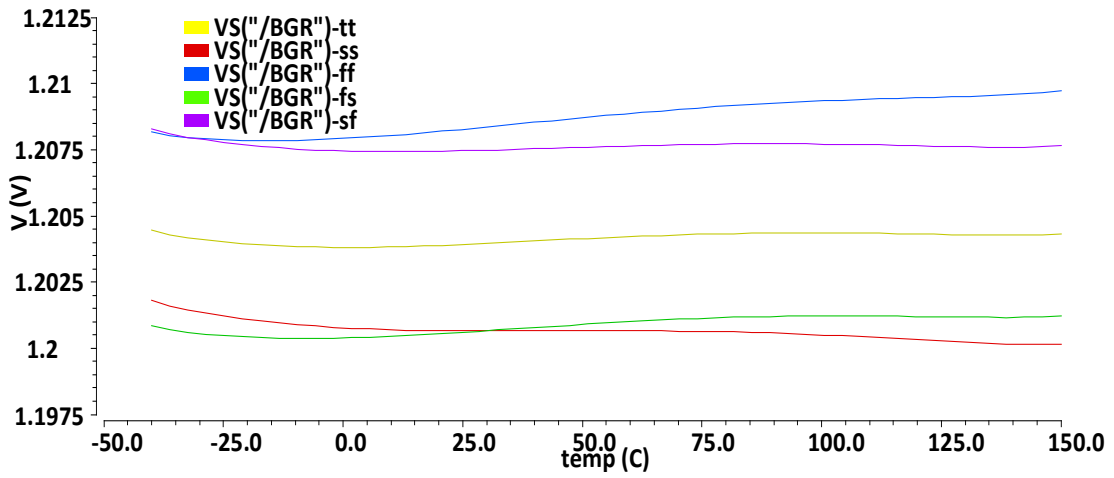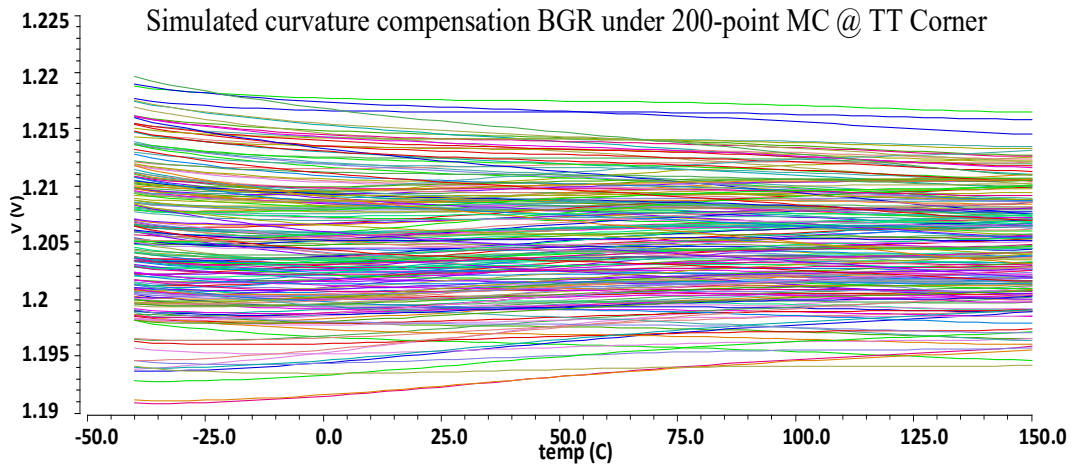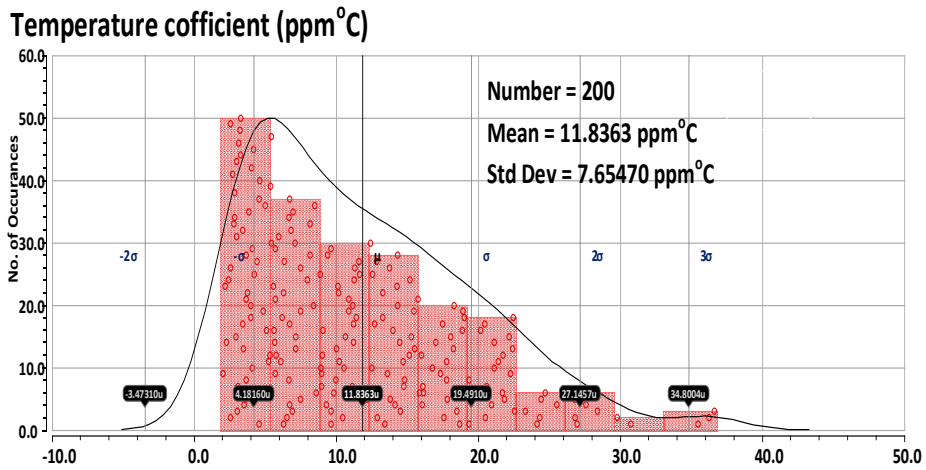
Fig 5.8. (a). The simulated T.C. simulation results in different MOSFET corners (b). Simulated curvature compensation untrimmed BGR under 200-point MC, (c). Simulated curvature compensation BGR histogram statistics

5.5 PRE-REGULATOR CIRCUIT DESIGN AND FLICKER NOISE/OFFSET REDUCTION

The pre-regulator is an essential block that safeguards the BGR from fluctuations in the power supply line, guaranteeing a robust line regulation performance, high PSRR, and the effectiveness of the temperature curvature compensation. The pre-regulator is shown in Fig. 5.9 (a).

The pre-regulator comprises its own BGR reference, a low-dropout regulator (LDO) with low quiescent current consumption, and a feedforward compensation to achieve high loop gain and small compensation capacitor C_{m1-2} silicon area. This solution provides a higher power-bandwidth efficiency when compared to the conventional simple Miller R_m-C_m compensation and successfully generates the power supply (V_{out} in Fig. 5.9 (a)) for the curvature-compensated BGR. The design equation for the current generation for the pre-regulator is given below. First, consider that M5 and M6 are operating in weak inversion mode.

(a)

2nd order TC compensation pre-regulator

(b)

BGR output voltage TC variations & drift without Pre-regulator

M1: 145.6409C 1.21135V

dx: 10.89776mC
dy: 26.629669mV
s: 2.4435912V/C

VDD variations from 2.2V – 2.8V

M2: 145.63C 1.184721V

(c)

M3: -40.0C 1.210266V

dx: 66.51421C
dy: 968.867676uV
s: 14.5663252uV/C

BGR output voltage TC variations & drift protection with Pre-regulator

VDD variations from 3.3V – 2.7V

M4: 26.51421C 1.209298V

(d)

Loop Gain Phase:Loop Gain dB20

96.99101deg

-527.6426mdB

Gain margin = 8.10165 dB at frequency = 20.4592 MHz.
Phase margin = 100.224 Deg at frequency = 4.73743 MHz.

5.58944MHz

(e)

108

Fig 5.9. (a). The proposed pre-regulator. (b) the 2nd order TC compensated pre-regulator output voltage (c) BGR output voltage drift & T.C. variations without pre-regulator assistance (d) BGR output T.C. variations & drift protections with pre-regulator assistance (e) LDO loop stability simulation

Thus, the current flowing into M5 and M6 are described by:

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L} \left(\frac{nkT}{q}\right)^2 exp^{\frac{V_{GS}-V_{th}}{nV_T}} \qquad (5\text{-}25)$$

Considering the loop M5-M6-R1, equation (26) is obtained:

$$V_{GS5} = V_{GS6} + I_s R_1 \qquad (5\text{-}26a)$$

Using the equation (16) to describe the gate-source difference between M_5 and M6, current $I_{S.}$ is obtained:

$$I_s = \frac{\Delta V_{GS}}{R_1} = \frac{(V_{GS5}-V_{GS6})}{R_1} = \frac{nV_T ln(K)}{R_1} \qquad (5\text{-}26b)$$

5.5.1 TEMPERATURE ANALYSIS

Fig. 5.9 (b) shows the output voltage of the voltage regulator. As can be seen, it is temperature compensated. Fig. 5.9 (c) shows the BGR temperature performance as a function of VDD if the temperature-compensated voltage regulator was not employed. It was possible to see that the high-order temperature compensation proposed by this work would not be achieved. This observation is valid for several existing curvature correction techniques in literature and highlights one of the contributions of this work. The authors usually do not show the temperature compensation for different values of VDD.

Finally, Fig. 5.9 (d) shows the output of the proposed BGR when the pre-regulator is included. The circuit can reject the supply voltage variations (2.7 V – 3.3V), making the circuit robust to PVT fluctuations. By introducing LHP zero along with Miller compensation, feedforward compensation improves the power-bandwidth efficiency of the pre-regulator; Fig. 5.9 (e) illustrates the stability of the pre-regulator; the proposed pre-regulator has a small area, a high bandwidth efficiency, and low power consumption when driving small or moderate capacitive loads.

5.5.2 TRANSIENT AND PSRR ANALYSIS

Fig. 5.10 (a) shows the simulated transient response results of the proposed BGR assisted by the pre-regulator. It shows that the regulator improves the line-regulation performance of the BGR by making it robust against large AC variations in the supply line. The output voltage only changes by 1-2% for an input V_{DD} variation of 400 mV.

Fig. 5.10 (b) presents the start-up process of the BGR reference and the proposed regulator. It shows that the pre-regulator's fast start-up process helps speed up the start-up of the BGR core. When considering the worst corner case (i.e., S.S.), the complete initialization takes just 20 μs.

In addition, the frequency domain perspective is shown in Fig.11. The simulated PSRR for the pre-regulator at 1kHz is about −77 dB, and the final BGR can achieve an improved PSRR of more than −100 dB lower than 100 Hz.
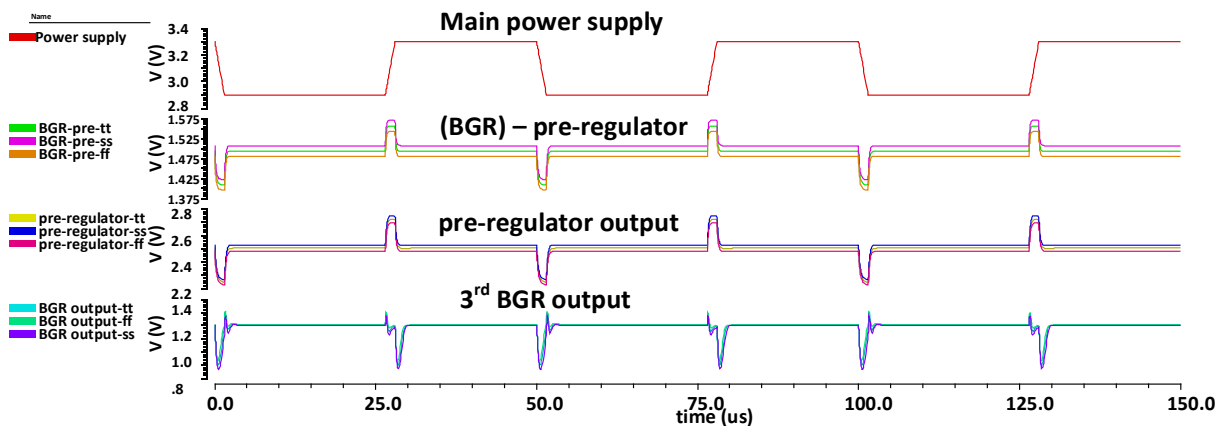
Fig 5.10 (a). Transient simulation of line regulation enhancement of the BGR
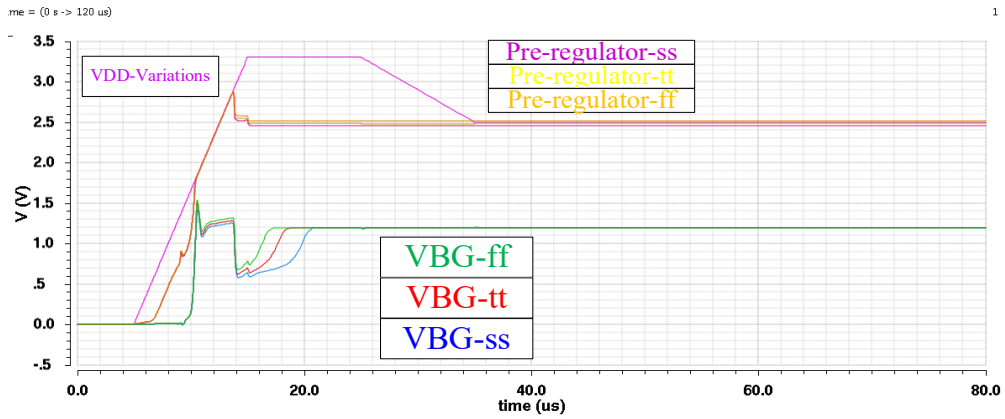
Fig 5.11 (b). Transient simulation of start-up process of the BGR

Simulated PSRR of the proposed BGR & Pre-regulator
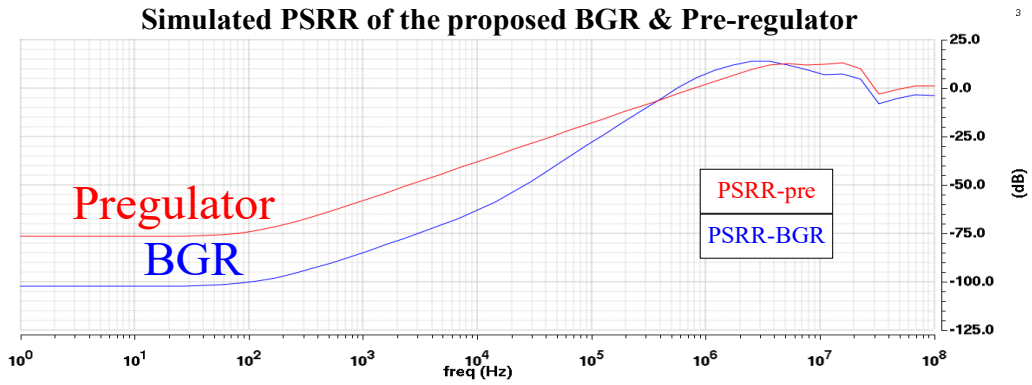
Fig 5.11. Simulated PSRR enhancement of the proposed BGR with pre-regulator protection
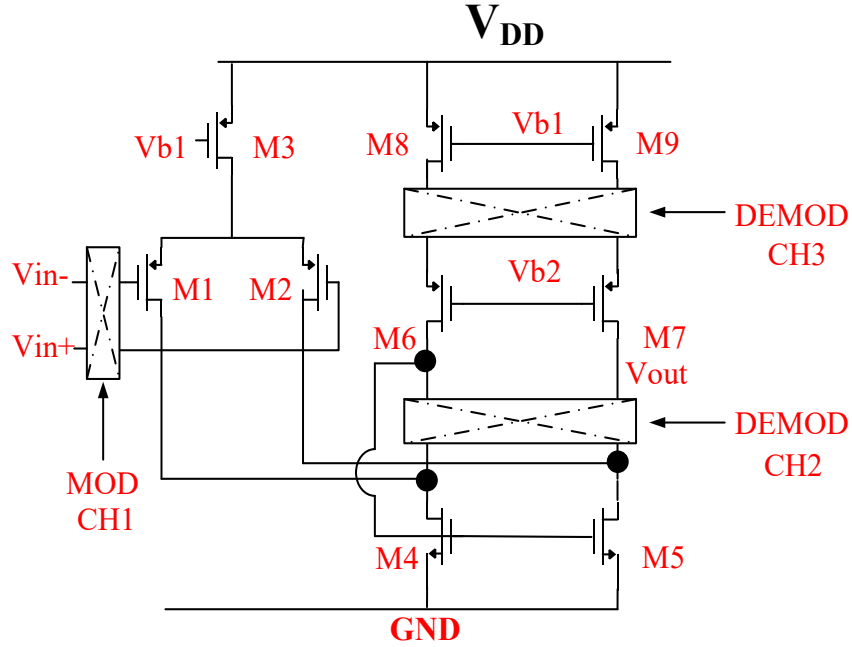
Fig 5.12. The Chopping Error Opamp (A_{1-2}) used in the proposed BGR
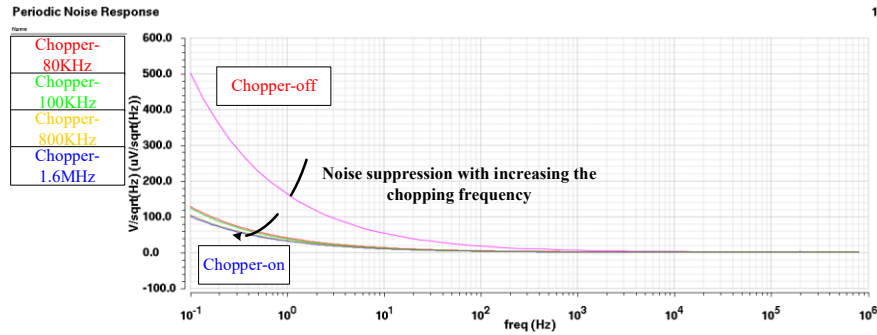
Fig 5.13. Analysis of the noise spectrum of the BGR before and after chopper & notch filters were activated.

5.5.3 CHOPPING ERROR OPAMP USED TO MITIGATE OFFSET AND NOISE

The folded-cascode Opamp, shown in Fig. 5.12, is the error amplifier used in the BGR core. The random input offset of this type of Opamp can be described as:

$$V_{os} = \Delta V_{th1,2} + \Delta V_{th4,5}\frac{g_{m4}}{g_{m2}} + \Delta V_{th8,9}\frac{g_{m8}}{g_{m2}} + \frac{V_{ov1,2}}{2} * [\frac{\Delta\frac{W}{L}_{1,2}}{\frac{W}{L}_{1,2}} + \frac{\Delta\frac{W}{L}_{4,5}}{\frac{W}{L}_{4,5}} + \frac{\Delta\frac{W}{L}_{8,9}}{\frac{W}{L}_{8,9}}] \tag{5-27}$$

112

Where ΔV_{th} and $\Delta \frac{W}{L}$ are the threshold voltage mismatch and the transistor sizes mismatch. From the noise perspective, the error amplifier (A_{1-2} refer to BGR Circuit in Fig. 5.7) is the major dominant contributor according to the noise summary from simulation. The designed folded cascode amplifier reduces the dominant flicker noise (1/f) and the offset voltage by using the chopping technique. The method uses switches at three locations in the schematic: CH1, CH2, and CH3. CH1 switches are at Opamp's input terminal and modulate the input signal to the odd harmonics of the chopping frequency and then amplify it through the input stage. These CH1 switches are designed with small transistor sizes to reduce the impact of charge injection and clock feedthrough. Switches CH2 and CH3 are located at the low-impedance node of the cascode stage, and their sizes were increased to reduce their linear on-resistance and not reduce the voltage swing amplitude. Fig. 5.7 also shows that the notch clock (phi2) is 90° delayed from the chopping clock (phi1) but with the same chopping frequency [27]. The notch filter is employed using the same structure as Fig. 5.14. Initially, the frequency of the noise integration is chosen such that the chopping frequency is two times the noise integration bandwidth, i.e., $F_{CHOP} > 2F_{NBW}$. Flicker noise is reduced by eliminating the need for degeneration resistance, typically used with M8-9 & M4-5 (refer to Fig. 5.12) to reduce flicker noise, providing increased headroom for future technology advances.

Fig. 5.13 presents the results of the Noise Spectrum simulation (e.g., PSS+Pnoise simulation using Cadence tools) to prove that the chopping error amplifier (EA) and the notch filter reduce the noise at the BGR output voltage. This figure shows two cases: chopper amplifier OFF and ON. As can be seen, the low-frequency noise is dramatically reduced when the chopper of the EA is ON for different values of chopping frequencies. Regarding the variability of the output voltage, the complete expression for it considering offset voltages of A_{1-2} is given by equation (28):

$$V_{ref} = V_{1st\ roder} + \Delta V_{GS} + V_{NL1-2} + V_{os1}\frac{R_3+R_4+R_5}{R_1} + V_{os2}\frac{R_3+R_4+R_5}{R_2} \qquad (5\text{-}28)$$

Where V_{os1-2} are the offset voltage of A_{1-2} described by (27). Voltages V_{os1-2} are amplified by the resistor ratio, thus increasing the changes at the output voltage. Besides applying the chopping technique,

a high DC gain and large input transistors have been employed to minimize random offset voltages. While a very symmetrical and compact layout can reduce the systematic offset.

5.5.4 CHOPPING RIPPLE REDUCTION USING SWITCHED R.C. FILTER & OUTPUT BUFFER

To reduce the ripple at the output voltage caused by the chopping technique, a switched capacitor (S.C.) notch filter was included at the input node of the output buffer. The notch filter is shown in Fig. 14 (c) and comprises a switched capacitor resistor shown in Fig. 5.14 (a).
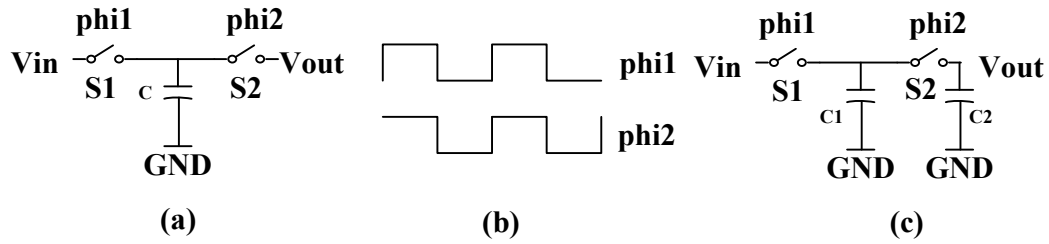
Fig 5.14 (a) Switched capacitor resistor; (b) non-overlapping clock; (c) low-pass notch filter

The two transmission gates (S1 and S2) are controlled by non-overlapping clock signals, $\Phi 1$ and $\Phi 2$ (Fig. 5.14(b)). During phase $\Phi 1$, the input voltage is sampled onto C1, while during phase $\Phi 2$, this ripple-free sampled voltage is transferred to C2. The advantage of the S.C. filter compared with the R.C. filter is that the frequency domain response of the first will introduce distinct notches at f_{chop}. Moreover, the harmonics of the S.C. filter can also improve the order of the LPF, saving a significant amount of area and achieving higher-order filtering and process-independent cut-off frequency. For an input x(t), the time-domain response y(t) for S.C. low-pass filter can be described as:

$$y(t) = \sum_{k=0}^{\infty} x(kT) * [u(t - kT) - u(t - (k + 1)T)] \tag{5-29}$$

where $T = \dfrac{1}{f_{ch}}$ In the frequency (s) domain, (29) becomes:

$$Y(s) = \sum_{k=0}^{\infty} x(kT) * \left[\frac{exp^{-skT} - exp^{-s(k+1)T}}{s}\right] =$$

$$\frac{1 - exp^{-sT}}{s} [\sum_{k=0}^{\infty} x(kT) exp^{-skT}] \tag{5-30}$$

Thus, rewriting for the transfer function of the filter $H(s)$ from (30), we get:

$$H(s) = \frac{1 - exp^{-sT}}{s} \tag{5-31}$$

The filter loop bandwidth can also be calculated as the following:

$$\omega_{eq} = \frac{1}{R_{ch}C} = f_{ch}\frac{C_1}{C_2} \tag{5-32}$$

The transient response of the BGR output voltage before and after activating the SC filter is shown in Fig. 5.15. We can see that a considerable portion of ripples due to the chopper technique is reduced, showing the importance of the output SC-filter without much area penalty. Fig. 5.16 shows the PSRR simulation results of the proposed BGR. The high-frequency PSRR performance is improved by applying an output S.C. low pass filter, while the pre-regulator mainly protects the low-frequency PSRR.
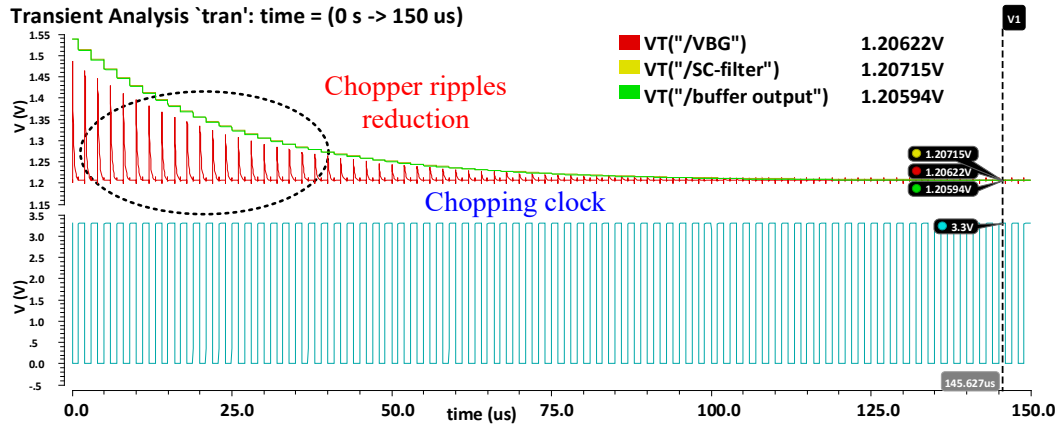
Fig 5.15. Sample and hold SC-filter for BGR output voltage ripples reduction
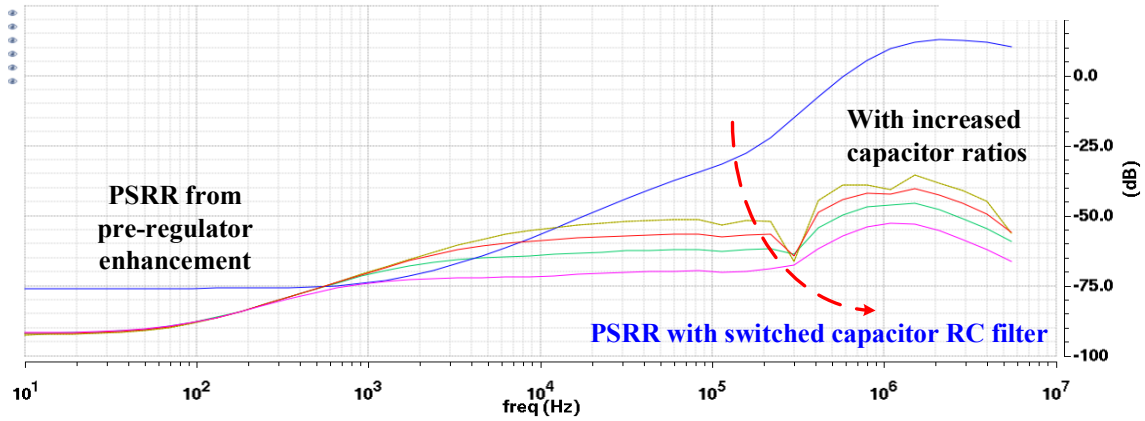
Fig 5.16. PSRR enhancement by adding output SC-low pass filtering

5.5.5 FABRICATED CHIP AND SILICON AREA
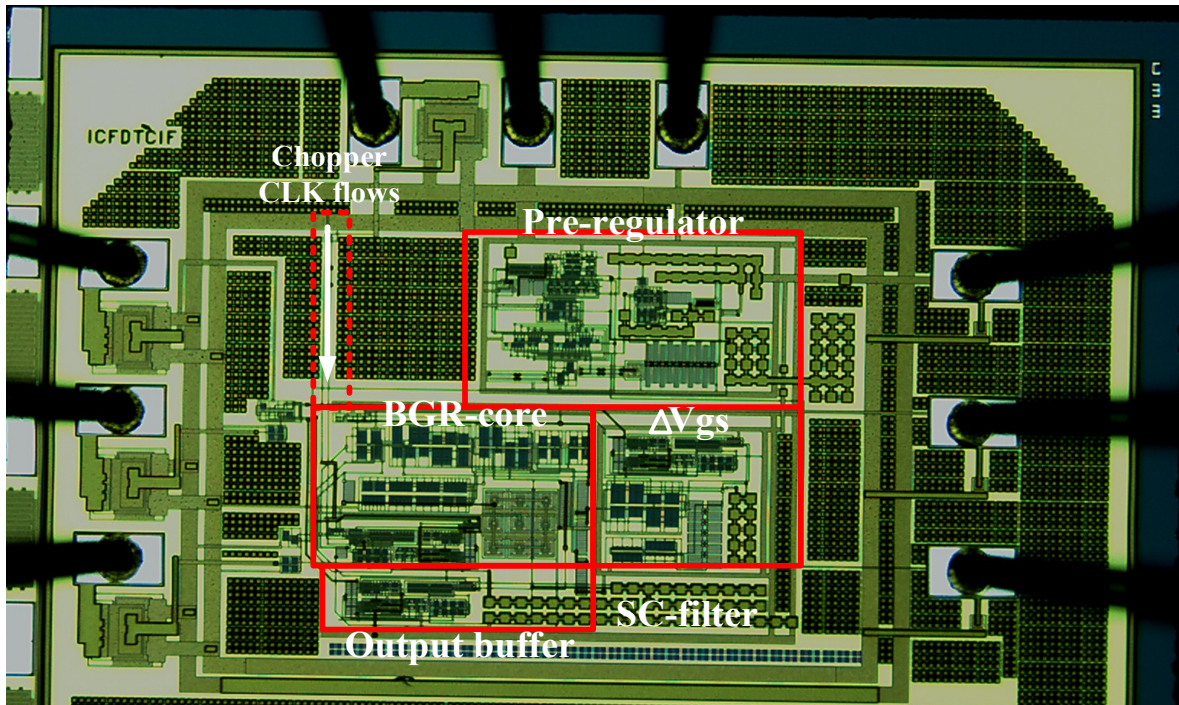
Fig 5.17. The microchip of the proposed bandgap.

Fig. 5.17 depicts a microphotograph of the proposed BGR implemented in 0.18 μm standard CMOS technology. The entire chip area is 0.56*0.8 mm^2.

5.6 EXPERIMENTAL RESULTS

5.6.1 OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE
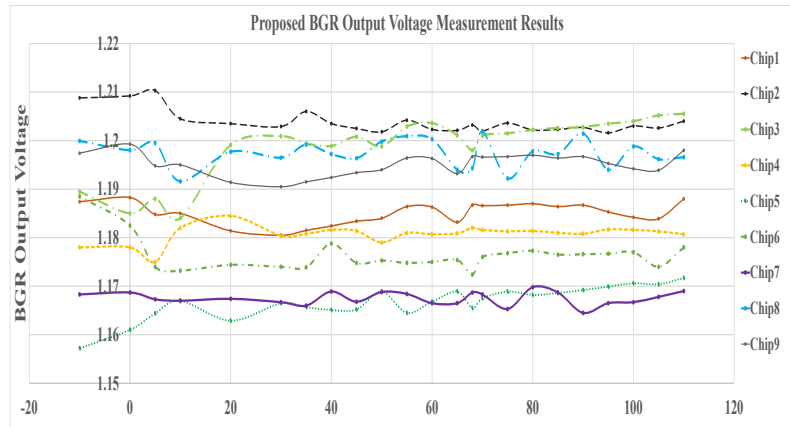
Fig 5.18 The proposed bandgap reference output voltage with temperature variations.

For assessments of proposed BGRs, several specific non-ideal effects, such as thermal electromotive forces (EMFs), need to be considered. Therefore, it is essential to consider the equipment's errors as well. By alternating probes during each measurement at a given temperature point, each measurement is repeated ten times in order to reduce systematic error, including several sources of systematic error, such as random offsets, mismatched BJTs, mismatched current mirrors, and mismatched resistors. Wires leading from the temperature chamber to V_{BG} are twisted together as differential wires in order to reduce spur and other common mode noise. (EMFs) can be reduced by using wires that are made from the same material and of the same length. The average value is then calculated from these ten measurements. Fig. 5.18 illustrates the temperature behavior of the output voltage of the proposed BGR for nine samples extracted from varying in temperature from -10 ºC to 110 ºC without trimming. The measured temperature coefficient is 5-15 ppm/ºC, which is more precise than conventional 1st order BJT-BGR with concave-down parabola T.C. (e.g., usually 50-80 ppm).

Note that although the circuit presents some sample-to-sample variation, high-order temperature compensation is guaranteed without any trimming technique, which is the most important. The voltage variations are caused by the mismatch of the output resistor. If a very accurate output voltage is desirable,

a simple trimming circuit can be added. However, two-point temperature calibration is not needed, and as a consequence, the trimming procedure is significantly simplified.

5.6.2 OUTPUT VOLTAGE AS A FUNCTION OF VDD VARIATIONS

The output response as a function of supply voltage variations was also measured and shown in Fig. 5.19-5.20. The power supply voltage was configured to operate as a periodical signal with 500 Hz and 50 kHz frequencies with amplitude variation of 2.7 V to 3.3V. The output variation under these conditions is less than 1%.
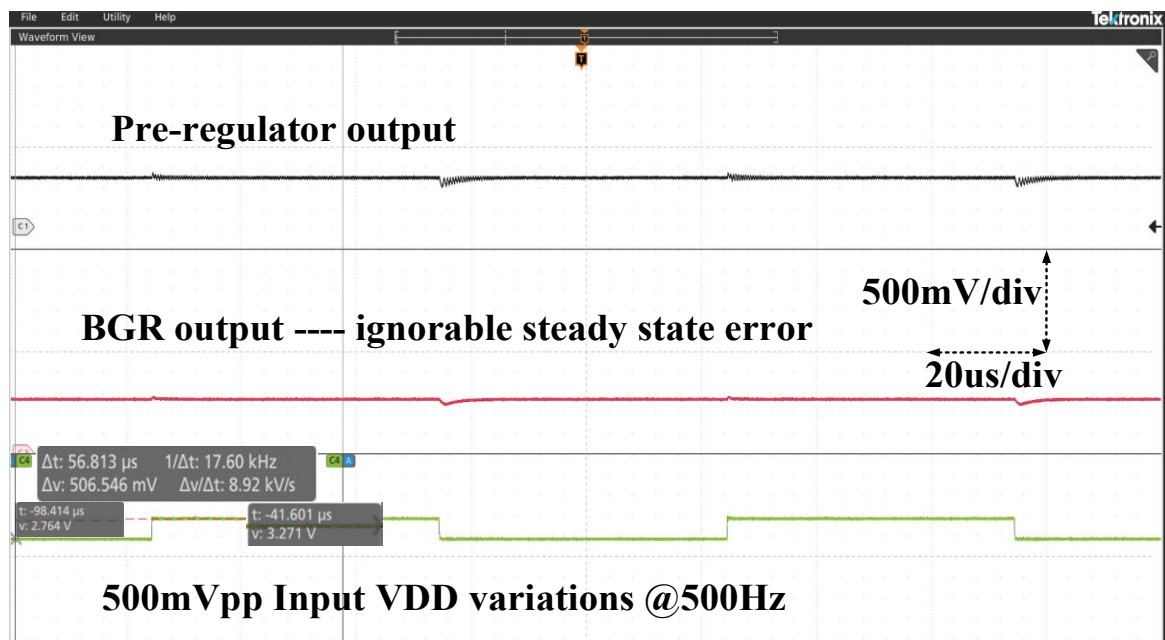
Fig 5.19 (a). 500mVpp VDD voltage under with clock variations @ 500Hz
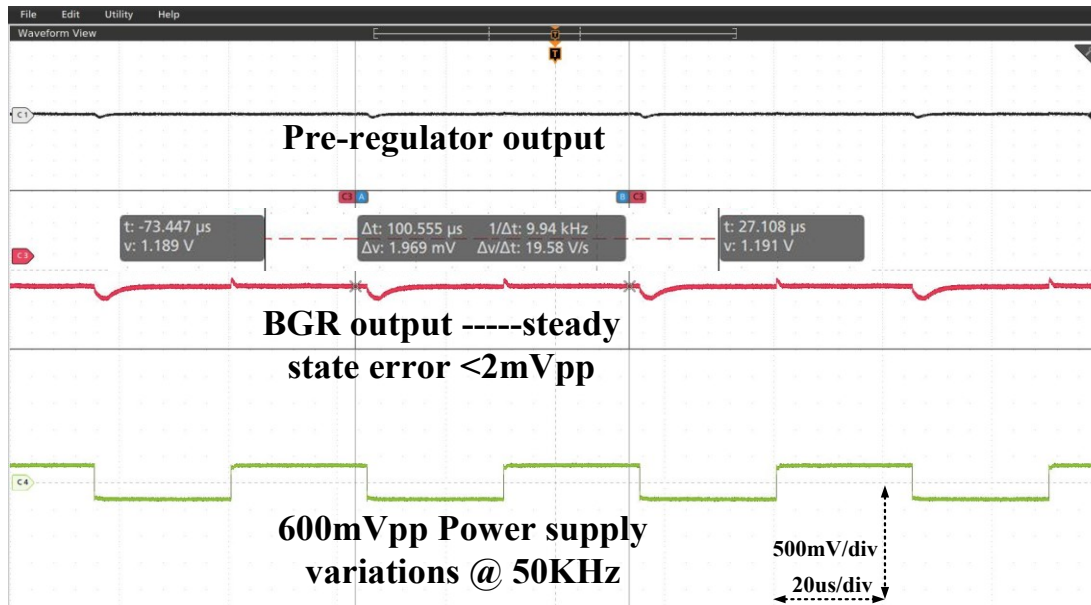
Fig 5.19 (b). 600mVpp VDD voltage under with clock variations @ 50KHz
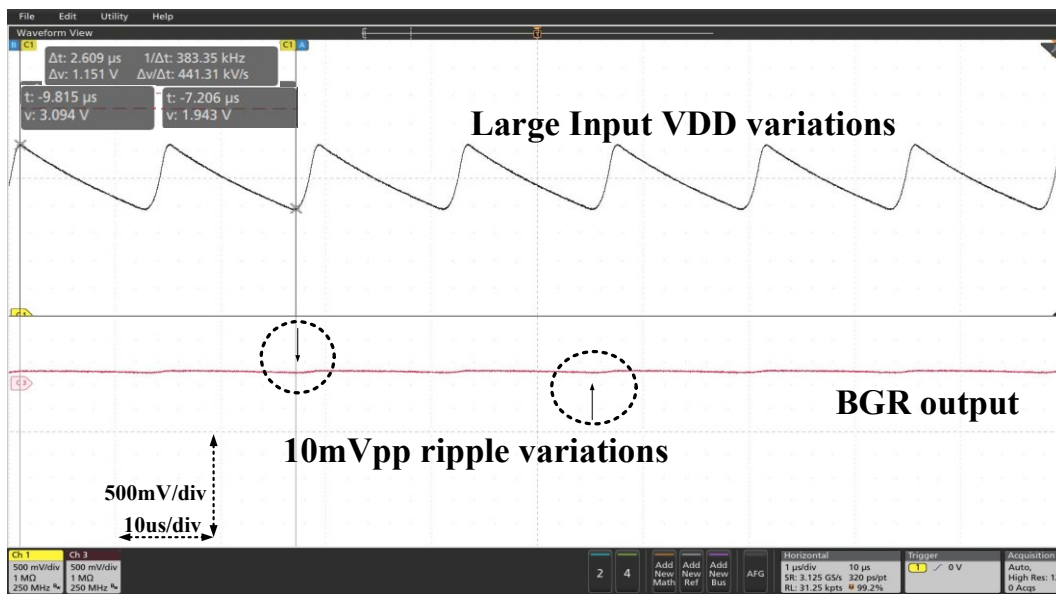
Fig 5.20. Transient VDD voltage variations with ramp variations
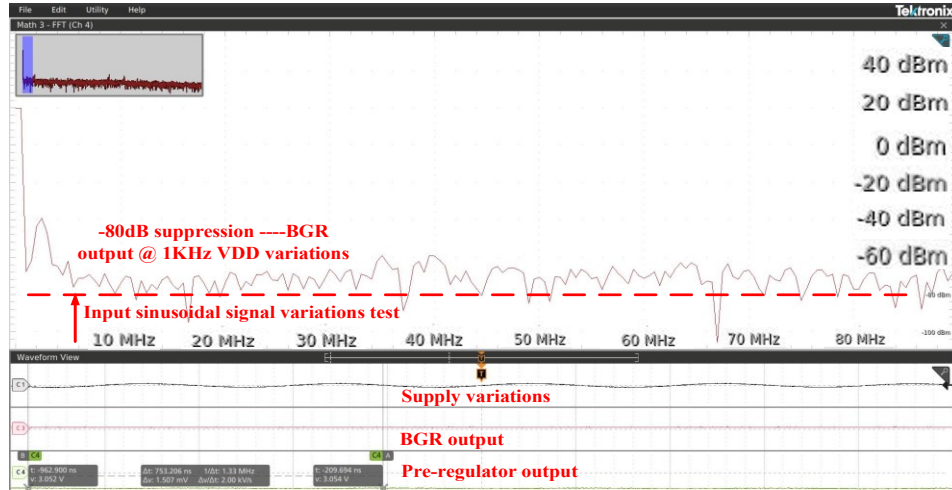
Fig 5.21. BGR output spectrum and its power supply noise rejection capability
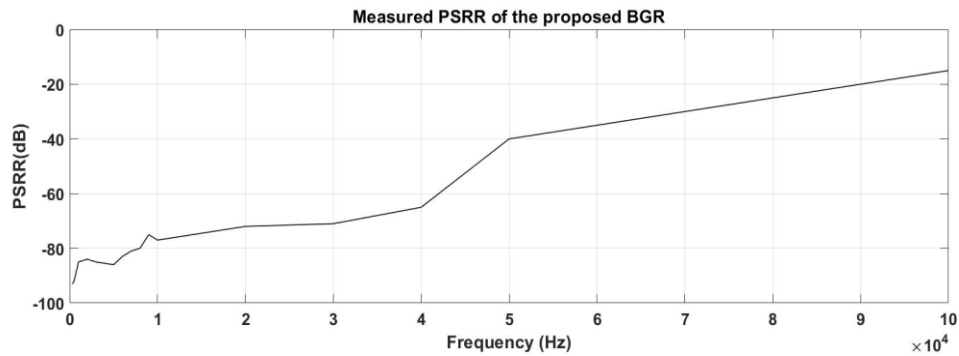
Fig 5.22. (a). Measured low-frequency PSRR of the proposed BGR without output filter
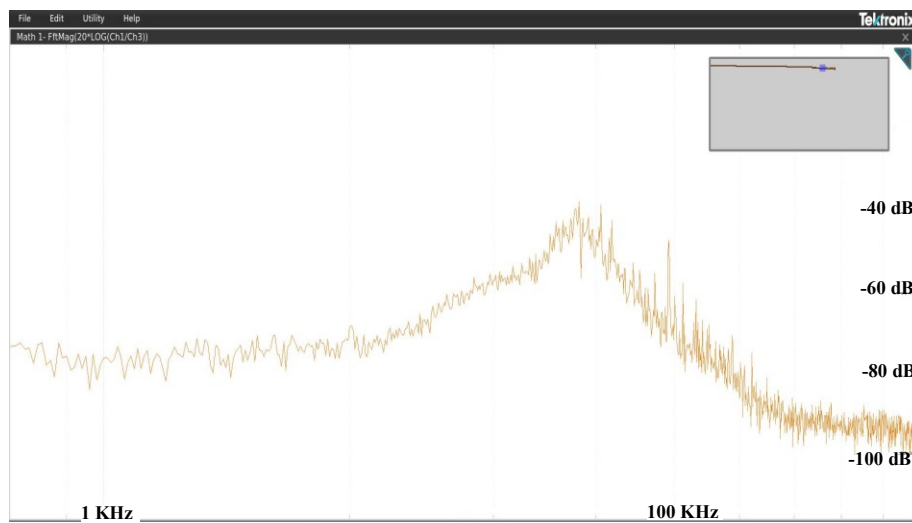
Fig 5.22 (b). Measured PSRR of the proposed BGR final output with the output filter

Fig. 5.20 shows a considerable V_{DD} variation (sawtooth variation), and its effect on the BGR output is still minimal. Therefore, the proposed BGR circuits can have strong immunity to power supply variations.

5.6.3 OUTPUT SPECTRUM AND PSRR PERFORMANCE

The measured BGR output spectrum and the PSRR performance are shown in Fig.5.21 and Fig.5.22, respectively. The V_{DD} voltage was measured at 3.3 V, and the PSRR value at DC and 1kHz frequency is −80 dB. The worst PSRR is −40.5 dB at 90 kHz.

5.6.4 OUTPUT NOISE AND POWER/AREA BREAKDOWN

Fig. 5.23 shows the measured noise PSD of the BGR for different chopping frequencies ($fchop$ = 10KHz, $fchop$ = 10MHz) at room temperature (27°C) with all noise sources considered. As can be seen, the chopping technique significantly mitigates the error amplifier's 1/f noise, which is dominant from 10 Hz to about 100kHz. The high chopping frequency (f_{chop} = 10MHz) shows a very effective chopping ripple reduction in the frequency domain. The ripple at 1st and 3rd harmonics is also reduced from −40dB to below −60dB, respectively.

Fig. 5.24 shows the breakdown of power and area for the proposed BGR. The pre-regulator, SC filter, and output buffer will significantly improve circuit performance at the cost of increased power consumption and area consumption.

Table I compares this proposed bandgap voltage reference with other prior-art curvature-compensation bandgap voltage references.
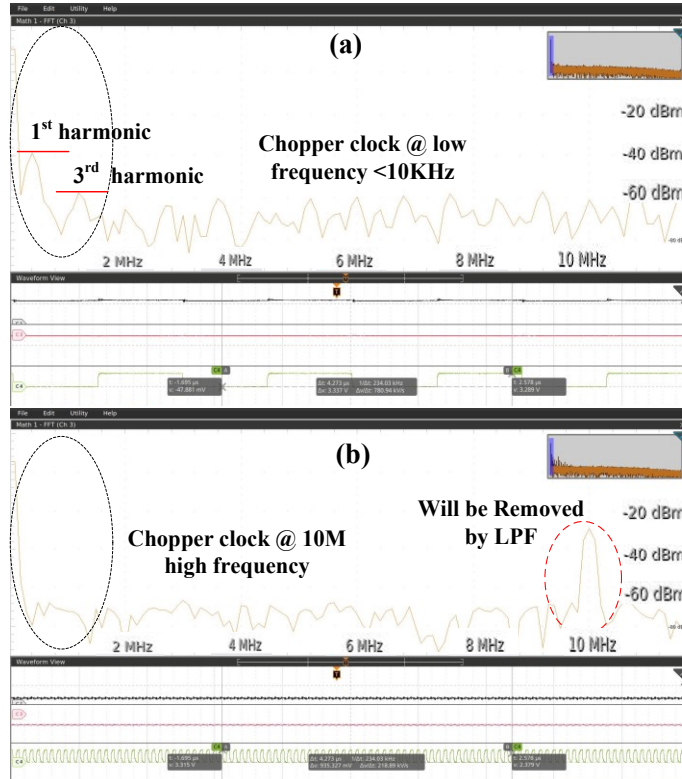
Fig 5.23 Measured functionality of chopper technique for flicker & D.C. offset the reduction.
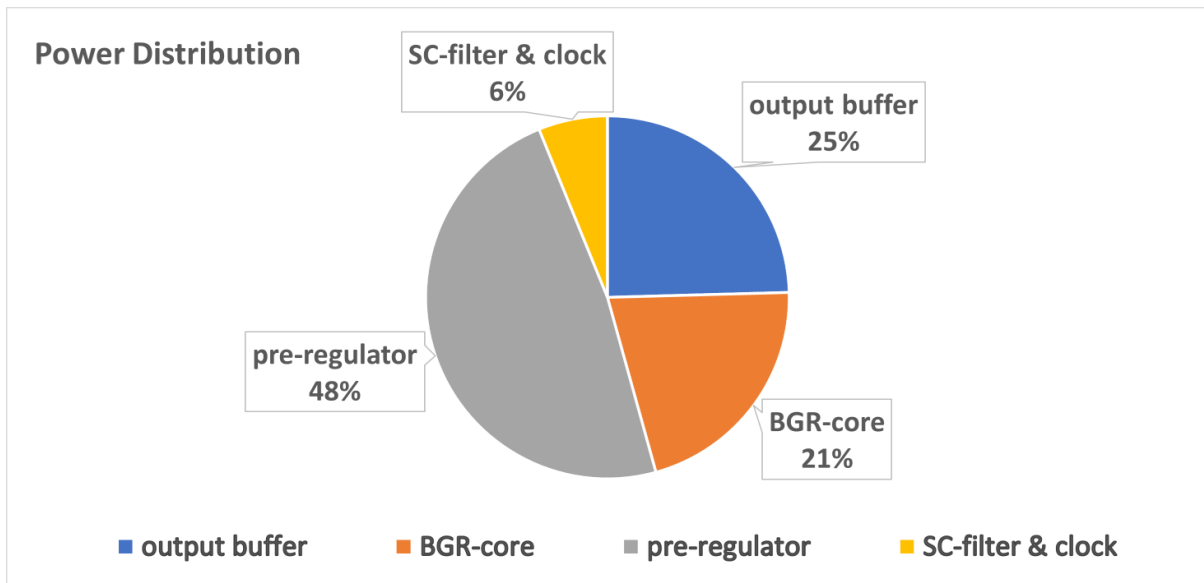
(a)
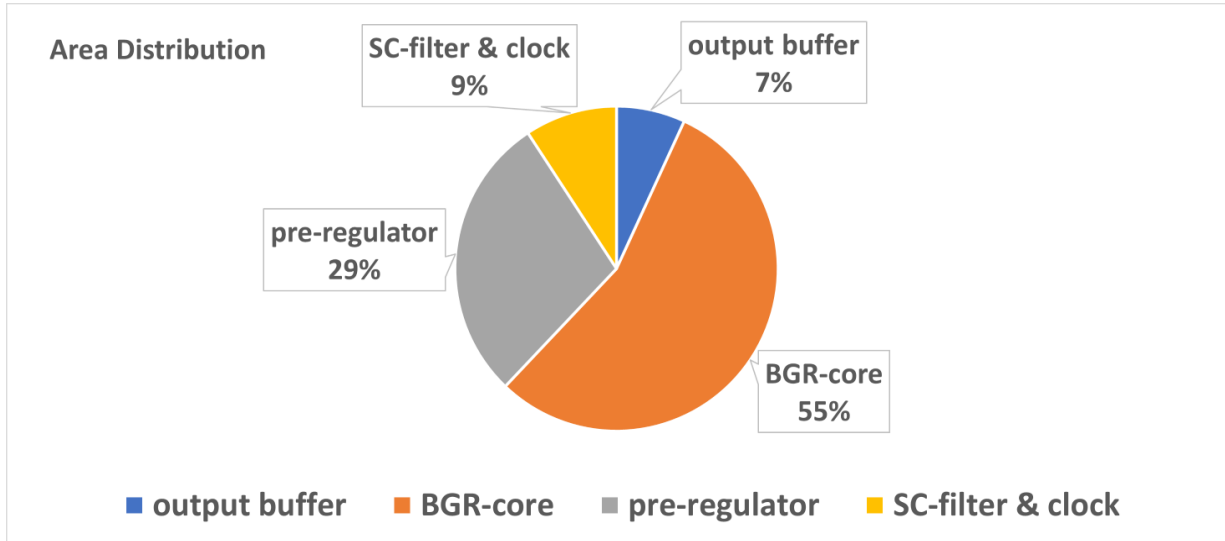
(b)

Fig 5.24 (a). The proposed BGR power distribution, (b). The proposed BGR area distribution

5.7. CONCLUSION

This paper presents a novel high PSRR, low noise, and high-order curvature-compensated bandgap voltage reference with a measured temperature coefficient of 5-15 ppm/$^{\circ}$C, and supply current consumption of 150 μA under a 3.3V power supply. The output buffer with a switched RC LPF is used to reduce the BGR noise further, save area and increase BGR PSRR. The chopping technique is applied in the error amplifier to significantly reduce the BGR output noise and input offset to allow the proposed BGR to work in low-noise applications. Finally, several silicon tests have been conducted to demonstrate the feasibility of the proposed curvature-compensated bandgap voltage reference.

TABLE 5.1 Performance summary and comparison

Parameter	This work	[87]	[86]	[74]	[73]
Year	**2022**	2021	2017	2015	2014
Technology	**0.18um CMOS**	0.13um CMOS	0.18um CMOS	0.13um CMOS	0.18um CMOS
Temperature range (°C)	**Meas: -10-110**	-40-150	-40-140	-40-120	-40-120
TC(ppm/ºC)	**5-15**	5.8-13.5	1.67	9.3	3.4-6.9
Supply (V)	**3.3-2.7**	3.3	1.3-1.8	1.2	1.2
Reference votlage (V)	**1.2**	1.16	0.547	0.735	0.767
Power (µW)	**<150**	396	50	144	45
Line regulation(%/V)	**0.005**	0.03	0.08	----	0.054
Noise	**1. 42 µV @320 Hz 112 µV (average noise)**	175 µV (average noise)	0.35 µV @700 Hz	200µV (average noise)	5.402µV @320 Hz
PSRR(dB @ DC)	**-80**	-82	------	-30 @100KHz	-80
Silicon Area mm^2	**0.448**	0.08	0.0094	0.063	0.036

CHAPTER 6 AN ULTRA-HIGH-SPEED, WIDE DYNAMIC RANGE LDO USING PIECEWISE SPEED ENHANCEMENT

Ximing Fu[1], Yushi Zhou[2], Pierre Leduc[2], and Kamal El-Sankary[1]

[1]Electrical and Computer Engineering, Dalhousie University, Halifax, NS, Canada

[2]Electrical and Computer Engineering, Lakehead University, Thunder Bay, ON, Canada

ABSTRACT

This paper presents an ultra-high-speed, wide dynamic range, low dropout (LDO) regulator that is used in applications for high-speed digital System on Chips (SoCs). The piecewise speed improvement is employed in the proposed LDO to ensure ultra-high-speed operation, which divides the LDO loop dynamics into three phases. Namely, phase one: an initial charge error reduction operation using the proposed current regulation circuits (CRC), phase two: derivative paths control with an auxiliary predictive differential path for large-signal slew enhancement; and phase three: a hybrid passive-active frequency compensation (PAFC) for small signal settling time enhancement by improving the power-bandwidth efficiency to achieve higher bandwidth and phase margin under large load current and capacitance variations. To further optimize the performance of the proposed LDO, essential building blocks are selected and designed. That includes a transconductance with a slew rate enhanced recycling folded-cascode error amplifier (EA) based on the local common-mode feedback is applied. A super-source follower (predictive path1) with class-AB output buffer and slew rate enhancement circuits (SRE) (predictive path2) is employed to enhance the slew rate of the LDO simultaneously. Also, a passive-active frequency compensation (PAFC) technique is derived from the main building blocks to speed up transient response by increasing the closed-loop bandwidth of the circuits. The proposed LDO is designed and fabricated in a 0.18-μm TSMC CMOS technology with 1.2V output voltage while the input voltage ranges from 1.8V to 1.3V. The design has been subjected to a step-change current change of 0-100mA at a large capacitive load of 0-10nF, whose rise/fall time is 50 ns. Having an average static error of less than 10 mV, the output of this regulator is stabilized in less than 2.6-9.8μs ranging from 0-100mA.

6.1 INTRODUCTION

The low-dropout regulator is an essential on-chip power management solutions for mobile and battery-operated devices requiring a clean supply voltage and a small CMOS area. Various types of LDO regulators have been developed [98-107]. One of the main challenges encountered with the high-speed digital system on chip (SoC) applications is optimizing the quiescent current (I_Q) for Low Dropout Regulators (LDOs) while maintaining good load current regulation, rapid response, and high driving capability from pF-nF capacitive loads. Fig. 6.1 shows a typical example of a capacitor-less (CAP-less)

126

conventional LDO regulator, in which the load capacitor (C_{load}) at the output serves as the system's non-dominant pole, and the dominant pole is located at the EA's output. The on-chip output capacitor (C_{filter}) serves as a charge buffer during the transient loading operation, absorbing (providing) any
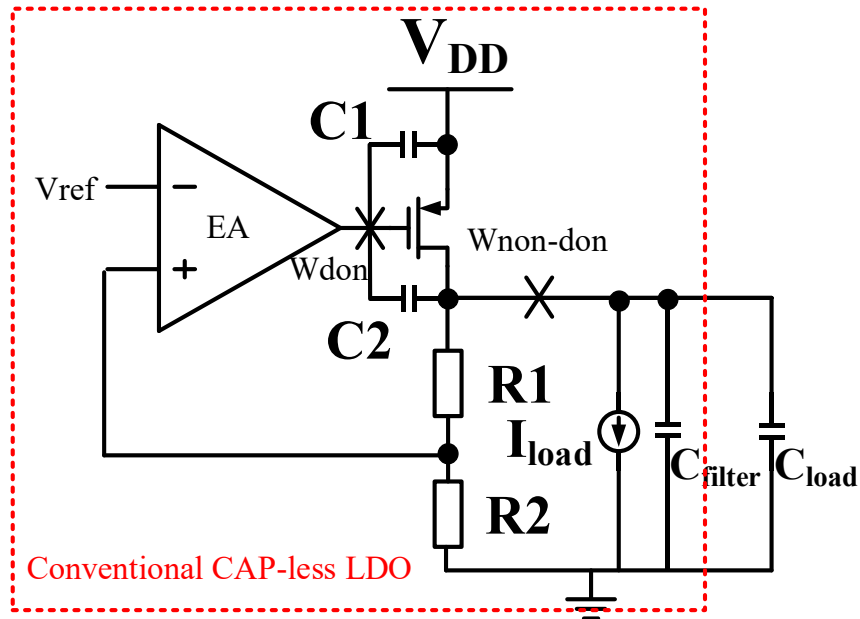
Fig. 6.1 Structure of a conventional output capacitor-less LDO (W_{don} is the dominant pole, and $W_{non-don}$ is the non-dominant pole).

(a) High bandwidth, high slew rate, initial charge compensation
(b) High bandwidth, high slew rate
(c) high bandwidth, low slew rate
(d) low bandwidth, low slew rate
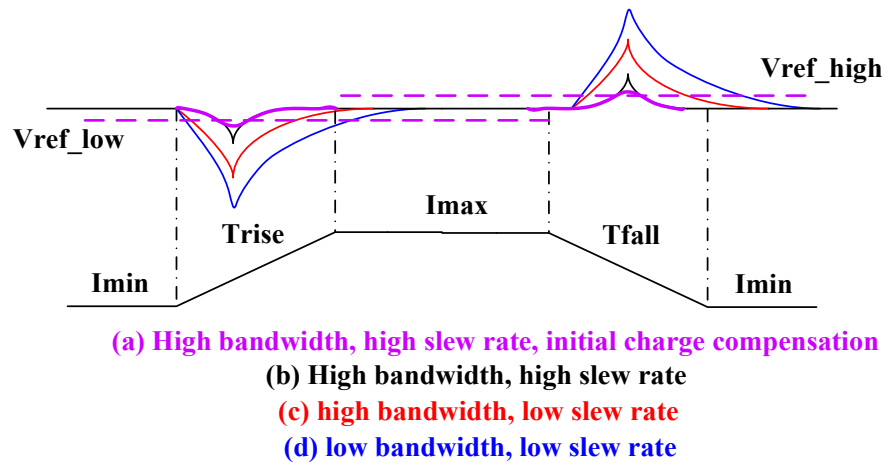
Fig. 6.2. Load transient responses of LDO with (a) high GBW and high SR, initial charge error compensation, (b) high GBW and high SR, (c) high GBW and low SR, (d) low GBW and low SR.
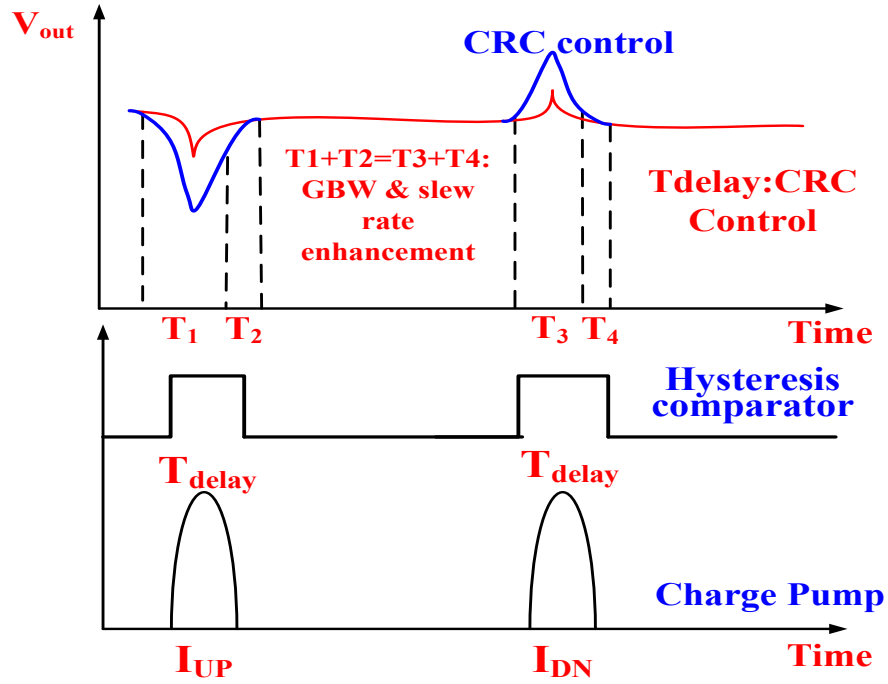
Fig. 6.3 Proposed LDO CRC transient enhancement operating principle.
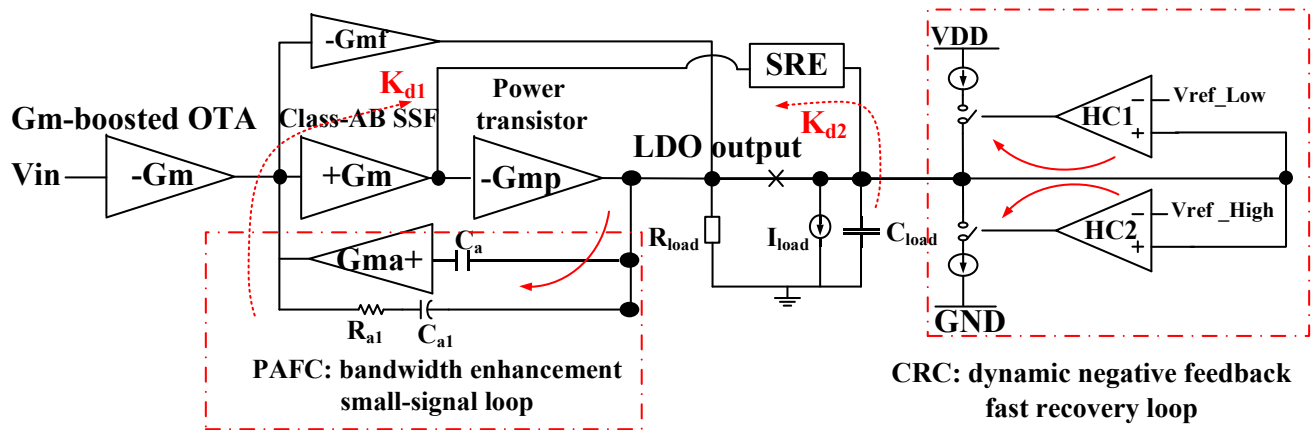
Fig. 6.4 Proposed LDO system architecture, including all treatments on small-signal bandwidth, large-signal slew rate, and initial charge error reduction
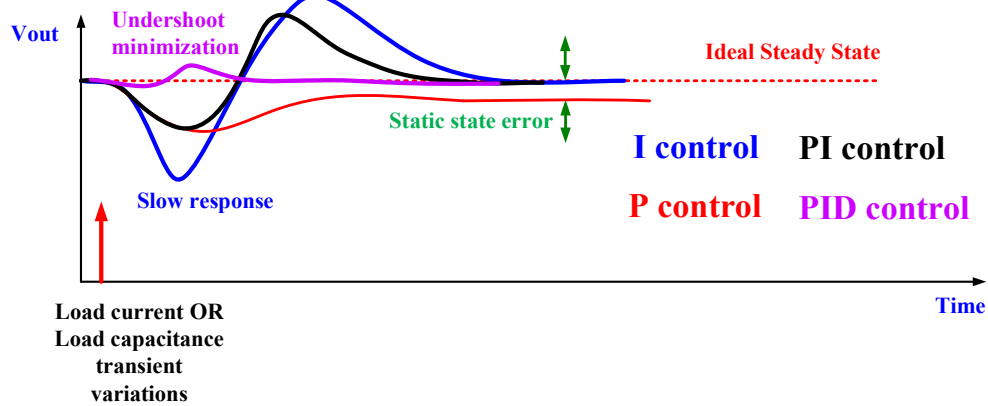
Fig. 6.5. Output voltage transient response under I-only, P-only, PI, and PID control.

transient current differences between the load and power transistors. Fast load current transient requirements will result in CAP-less LDO output voltage being markedly impacted by reduced output filtering capacitors, leading to significant ripple changes in output voltage, which is not acceptable for digital SoC devices supplied by power-line susceptible to LDO regulators. In addition, time-varying large parasitic capacitance, e.g., 10 pF to 5 nF, is inevitably generated from the digital building blocks in SoCs. Fig. 6.2 illustrates the dynamics of LDO loops based on four different scenarios, including the effects of large-signal, small-signal, and initial charge conditions. Wide GBW is essential for a fast-response LDO regulator, while it does not necessarily guarantee a fast response because the response will be slew-rate-limited at the gate of the power transistor. This will be more problematic in the event of a large load current and a small quiescent current.

A wide bandwidth can be achieved using several techniques, including load-current dependent boost currents [108], dynamically biased buffer impedance attenuation (BIA) [109], adaptively biased super current mirrors [110], and multiple small-gain stages [111]. In recent years, fully integrated CAP-less LDO designs have received considerable attention due to their small footprint and low cost. Since a large filtering capacitor is not presented, fully integrated LDOs exhibit significantly reduced transient responses. According to [112], an active-capacitor frequency compensation strategy with push-pull charging capabilities makes for a small, space-saving, and fast-transient capless low-dropout regulator (LDO). [113] reports that CAP-less LDOs can provide a fast transient response for a wide range of load current using the flipped voltage follower (FVF) topology. The design, however, was susceptible to

variations in process, voltage, and temperature (PVT) and was not fast enough to accommodate load current variations in the rise and fall time of less than 50 ns. [116] and [117] demonstrate that FVFs with folded-cascode gain stages can provide improved regulation. However, it may prove difficult to maintain loop stability when driving large capacitive loads. [120] incorporated a non-inverting gain stage for a higher loop gain and Miller compensation for maximum stability but did not provide experimental results for transients faster than 100 ns rise and fall time. A comparator-based ultra-fast response regulator based on a 45 nm SOI process was also proposed in [127] that consumed 12 mA of quiescent current and required a 1.46 nF deep-trench capacitor. It should be noted that the intrinsic ripple of this regulator is 10 mV and not compatible with the power line-sensitive SoC systems.

To overcome the challenge of fast transient loop dynamics while maintaining a wide range of capacitive load, this work uses piecewise speed enhancement to achieve ultra-high-speed and wide stability range simultaneously. As shown in Fig.6.3, when the LDO output triggers a hysteresis comparator, the charge pump will provide the corresponding compensation charge. In a large-signal slewing period, large-signal slewing rate enhancement has been achieved by using differential path control with dual predictive paths from the super source follower (SSF) with class-AB output and SRE. PID controllers [114] combining proportional (P), integral (I), and derivative (D) control methods to improve the loop's ability to respond to transient changes are utilized.
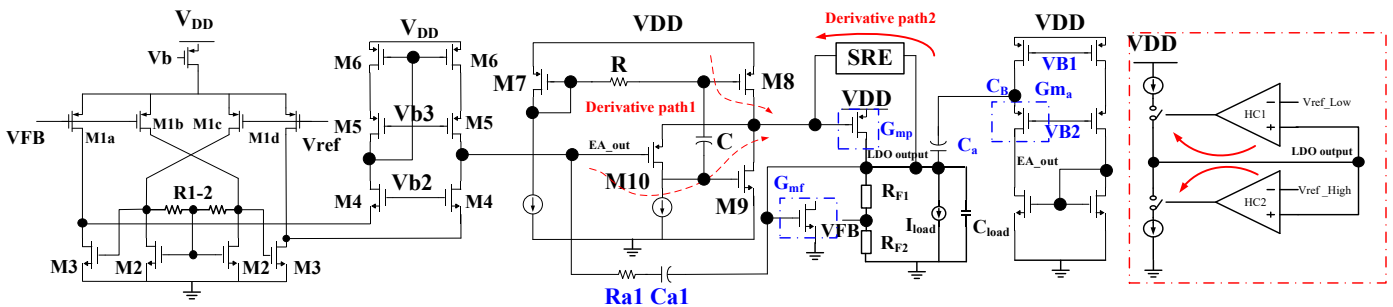
Fig. 6.6 Proposed LDO circuits level implementation based on the system architecture

When LDO enters a small-signal operation, the non-dominant pole generated from the output is dynamically influenced by the output capacitance ranging from the pF-nF range and load current change. As a result, conventional frequency compensation methods, such as Miller compensation, nested or reversed nested Miller compensation, will not maintain good driving capabilities without compromising

stability since the dominant pole for Cap-less LDO designs would no longer be located at the output node. Over the past decades, various compensation schemes for three-stage amplifiers have been reported [98-105]. Nested Miller Compensation (NMC) using pole-splitting techniques is widely recognized in three-stage amplifiers. It involves capacitively nesting several gain stages to achieve pole-splitting [105]. However, this technique is unsuitable for high-speed applications due to the bandwidth loss caused by miller capacitors' pole splitting.

The proposed hybrid passive-active frequency compensation (PAFC) technique is introduced to tackle the previously mentioned problem. The main characteristics of the proposed PAFC technique can be concluded as follows: (i) there is much less power consumption than a multi-feedback active frequency compensation network. Therefore, the additional static power consumption can be ignored. (ii) The current feedback (CBs) loop hybrid with a passive network facilitates the accurate placement of the LHP zeros. (iii) Using the practical design equations for loop gain, pole-zero locations, and phase margin (PM), it is possible to accurately predict the stability condition of the proposed LDO. Unlike other compensation schemes, the proposed scheme does not rely on the absolute accuracy of the components, which improves the robustness of the design. The main concept of the proposed frequency compensation is to remove the internal Miller capacitor with more advanced compensation techniques to extend more tolerance on the phase margin. In addition, most of the works [98-105] failed to address the problem of gain peaking due to a large Q-factor of complex-pole when the load capacitance changes significantly. The proposed technique also improves settling time by effectively improving power-bandwidth efficiency.

This paper is organized as follows: Section 6.2 presents an overview of the proposed LDO architecture with a fundamental theory analysis. Section 6.3 introduces the proposed LDO building blocks, including the hybrid passive-active frequency compensation architecture, EA, class-AB SSF, SRE, and CRC circuits. Section 6.4 presents the measurement results, and Section 6.5 concludes the paper.

6.2 PROPOSED LDO STRUCTURE TRANSIENT SPEED APPROXIMATION

Fig. 6.4 shows the simplified architecture of the proposed LDO, and Fig. 6.5 illustrates loop dynamics under different control mechanisms, e.g., P-control, I-control, PI-control, and PID- control. The I-control integrates the *old* information in the loop, while the P-control offers proportional output based on the *current* error information. Notice that the integration is nothing but a low-pass filter, which exhibits a long transient response time. On the other hand, P-control provides relatively constant gain across a wide frequency range, which is beneficial in reducing overshoots and undershoots. In conjunction with P-control and I-control, it becomes evident that a stable steady-state output can be obtained in a shorter period without sacrificing performance. The undershoot/overshoot voltage $\Delta V_{out}(t)$ can be approximated as:

$$\Delta V_{out}(t) = \max(\int \frac{I_p(t) - I_{load}(t)}{C_L}, \frac{I_{load}(t)}{A_p g_{mp}}) \qquad (6\text{-}1\text{-}a)$$

where $I_p(t)$ and $I_{load}(t)$ are the power transistor current and the load current step, respectively. C_L represents the load capacitance. g_{mp} is the transconductance of the power transistor, and A_p is loop gain of P-control. The $\int \frac{I_p(t) - I_{load}(t)}{C_L}$ term is the voltage drop caused by the loop integration, while the $\frac{I_{load}(t)}{A_p g_{mp}}$ term represents the $\Delta V_{out}(t)$ drop for loop gain of P-control to compensate $I_{load}(t)$. A D-control can be inserted to improve further the transient response's performance, which is utilized to predict the *new* information through the loop. In the presence of the prediction path, a classic proportional-integral-derivative (PID) system can be formed, significantly improving the transient response of the output voltage, shown in Fig.6.5. Eq. (1-b) denotes the output voltage under the PID control:

$$V_{out}(t) = k_p e(t) + k_i \int_0^\tau e(t)dt + k_D de(t)/dt \qquad (6\text{-}1\text{-}b)$$

Where $V_{out}(t)$ is the final output, k_p, k_i, k_D are the main factors of the P, I, and D paths. k_p, k_i are mainly provided from the LDO open-loop transfer function. Fig.6.6 shows two derivative paths, e.g., $k_D = k_{D1} + k_{D2}$, consisting of two parts: (i) The high-pass RC filter within the SSF behaves as a derivative path k_{D1} to significantly increase the slew rate and current efficiency. A class-AB super source follower (SSF) is introduced as a buffer stage. Class-AB operation is achieved without consuming

great static power. (ii) The second derivative path, k_{D2}, is formed by a pair of capacitors in SRE circuits to perform a derivative function. Using these capacitors, the rate of change for the load current is then fed back to the inner loop to perform a large-signal enhancement.

Table I. Influence of PID Control parameters on LDO Loop Characteristics

Parameters	Under/overshoot	Settling time	Steady-state error	Stability
Increase K_p	increase	decrease	decrease	improve
Increase Ki	decrease	increase	decrease	degrade
Increase K_d	decrease	decrease	No effect	improve

From the circuit implementation point of view, the analysis can be given that Fig.6.6 also illustrates that the proposed three-stage LDO regulator is composed of an error amplifier (EA), a buffer (BUF), a power transistor, and a PAFC loop. The dominant pole is located within the feedback loop rather than the output node in the proposed CAP-less LDO structure. To supply a fast transient output current, it is important to improve both the gain-bandwidth $GBW = \frac{\beta_{FB} g_{mEA}}{C_1 + (1+A_p)C_2}$ and the slew rate $SR = \frac{I_{SR}}{C_{gate}}$. C_1 and C_2 in the GBW expression are the output capacitance of the error amplifier (EA) and LDO output, respectively. β_{FB} is the feedback factor determined by $\frac{R_{F2}}{R_{F1} + R_{F2}}$. g_{mEA} is the transconductance of the EA. A_p is $g_{mp} R_{out}$. C_{gate} is the parasitic capacitor at the gate of the power transistor ranging from tens to hundreds of picofarads; therefore, the capacitance C_{gate} would inevitably limit the slew rate of the loop dynamics.

The step response represented by $T_{1,2}+T_{3,4}$ in Fig.6.3 is a function of the closed-loop bandwidth (BW) and I_{SR} given by:

$$T_1 + T_2 \approx T_3 + T_4 \approx \frac{1}{GBW} + C_{gate} \frac{\Delta V}{I_{sr}} \qquad (6\text{-}2)$$

Where GBW is the closed-loop bandwidth. ΔV is the voltage variation at the gate of the power transistor. To minimize $T_{1,2}+T_{3,4}$, the LDO requires a wide closed-loop bandwidth and a high slew rate. Furthermore, the settling time can be minimized by using the proposed CRC circuits. The improved settling time is

$$T_1 + T_2 \approx T_3 + T_4 = \frac{1}{GBW} + C_{gate}\frac{\Delta V - \alpha V_{comp}}{I_{SSF}+I_{SRE}} \tag{6-3}$$
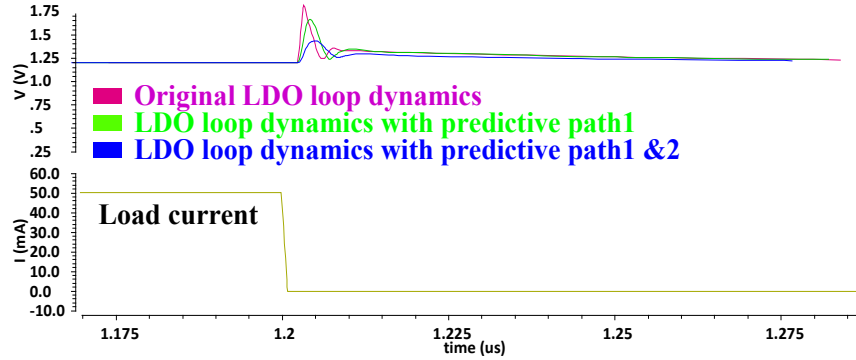
(a)
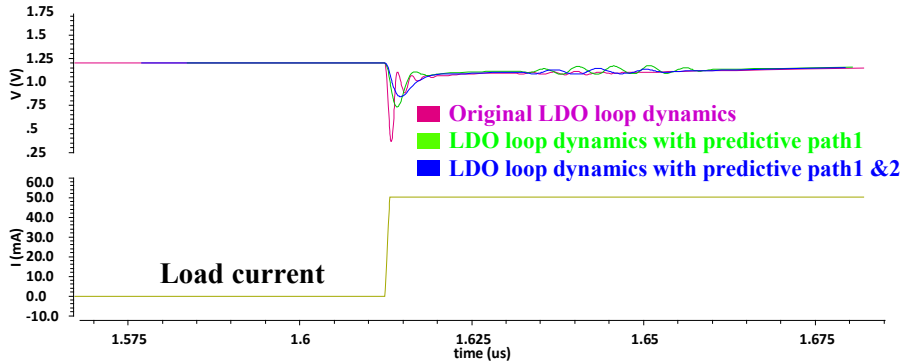
(b)
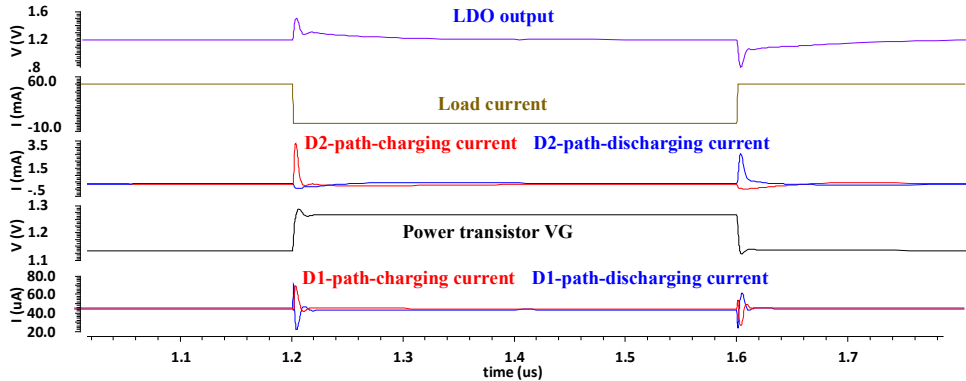
(c)

Fig. 6.7 Simulated load transient responses. (a)Overshoot comparison, (b) Undershoot comparison, and (c) Derivative paths transient charging and discharging current.

$$V_{comp} = \frac{I_{UP,DN} * T_{delay}}{C_L} \qquad (6\text{-}4)$$

I_{SSF} and I_{SRE} are the class-AB SSF buffer driving current and slew rate enhancement driving current, respectively. V_{comp} is compensation voltage factor taken effect on the gate of the power transistor. and α is the CRC feedback error caused by proportional control through integration. (iii) differential control K_d predicts the output signal variation and improves the system stability. As a result, improved overall performance is attained. The effects of the individual controls relative to the LDO loop characteristics are summarized in Table I.

Fig. 6.7 shows the simulation results of undershoot and overshoot with/without SSF using class-AB operation and SRE circuits. Due to the dynamic charge and discharge current generated by differentiating the LDO and error amplifier output variations, the undershoot and overshoot are substantially reduced.

6.3 THE ANALYSIS OF PROPOSED CIRCUITS

6.3.1 SPEED-ENHANCED RECYCLING FOLDED-CASCODE OTA
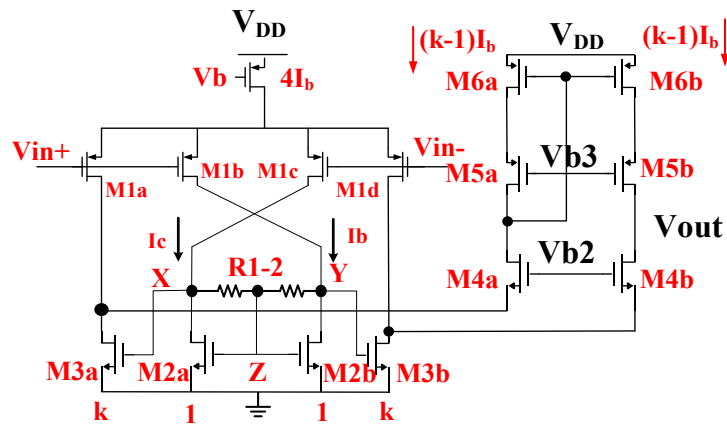
Fig. 6.8 Proposed Gm-enhanced recycling folded-cascode amplifier

[118], [119] presents the conventional recycling folded cascade amplifier (RFC) with all transistors operating in the saturation region. The equivalent transconductance of RFC, e.g., G_{m-RFC}, can be expressed as (6-5). GBW is given as (6-6):

$$G_{m-RFC} = (k+1)\, g_{m1a} \tag{6-5}$$

$$GBW = \frac{G_{m-RFC}}{C_L} \tag{6-6}$$

Where K is the ratio factor of the current mirror of the load pairs. g_{m1a} is the transconductance of input pairs M_{1a}. C_L is the load capacitance. Fig. 6.8 shows the proposed recycling folded-cascode amplifier with G_m enhancement, in which the OTA is based on the local common-mode feedback structure. The active load in [118-119] has been replaced by local feedback loops containing matched resistors R_{1-2}. The resistors do not carry any DC current when the OTA is in a quiescent state. The input AC signal circulates through nodes R_{1-2}, and node Z will serve as the virtual ground. As a result, the equivalent transconductance ($G_{m-enhanced}$) and the GBW are:

$$G_{m-enhanced} = (1 + g_{m3}(R1-2\ //\ ro1_{b,c}\ //\ ro2_{a,b}))\, g_{m1a} \tag{6-7}$$

$$GBW \approx \frac{(1+g_{m3}R)\, g_{m1a}}{C_L} \tag{6-8}$$

Note that if a large value of $R1\text{-}2$ is chosen, $G_{m-enhanced}$ would be much larger than K in RFC. As a result, the G_m has been enhanced compared to RFC at the same power. This results in an increase in GBW as well.

To analyze the large signal response, we assume that a large negative step signal ΔV is applied to V_{in+}, if a large positive Vid is applied to the input ports, a differential current $I_d = I_c - I_b$ is created, and the currents through resistors will be $I_R = 0.5 * (I_c - I_b)$. The drain current of transistors M_{2a} and M_{2b} will be a common-mode current $I_{cm} = 0.5 * (I_c + I_b)$. Thus, the gate and drain voltages of M_{2a} and M_{2b} will change accordingly. Considering the second-order relation between I_d and V_{id}, the transfer characteristic of the proposed amplifier (I_{out} versus V_{id}) is a 4th order function of V_{id}, shown in (6-9). Therefore, the circuit can enhance the slew rate by generating a considerable current.

$$V_{dM2a} = V_{gM2a} + \frac{RI_d}{2}, V_{dM2b} = V_{gM2b} - \frac{RI_d}{2}, \text{R1} = \text{R2} = \text{R}$$

$$V_{gM2a,b} = V_{thn} + \sqrt{\frac{2I_{cm}}{\beta_{2a,b}}}$$

$$I_{3a} = \frac{\beta_{3a}}{2}(V_{gM2a,b} + \frac{RI_d}{2} - V_{thn})^2 = \frac{\beta_{3a}}{2}(\sqrt{\frac{2I_{cm}}{\beta_{2a,b}}} + \frac{RI_d}{2})^2$$

$$I_{3b} = \frac{\beta_{3b}}{2}(V_{gM2a,b} - \frac{RI_d}{2} - V_{thn})^2 = \frac{\beta_{3b}}{2}(\sqrt{\frac{2I_{cm}}{\beta_{2a,b}}} - \frac{RI_d}{2})^2$$

A large voltage swing occurs at node X/Y due to the effect of local common-mode feedback circuits, causing the output current I_{out} through M_{3b} is,

$$I_{out} \approx \frac{(k-1)}{k}\frac{\beta_{3a,b}}{2}(\sqrt{\frac{\beta_{1b,c}}{\beta_{2a,b}}}V_{id} \pm \frac{R\beta_{1b,c}}{4}V_{id}^2)^2 \tag{6-9}$$

The common-mode feedback structure produces the following results: the maximum output current of the OTA increases with V_{id}^4 , leading to a boost in the slew rate when compared to RFC. Therefore, the slew rate enhancement is achieved by generating a considerable current.

6.3.2 CLASS-AB SUPER SOURCE FOLLOWER, SRE, AND CRC CIRCUITS
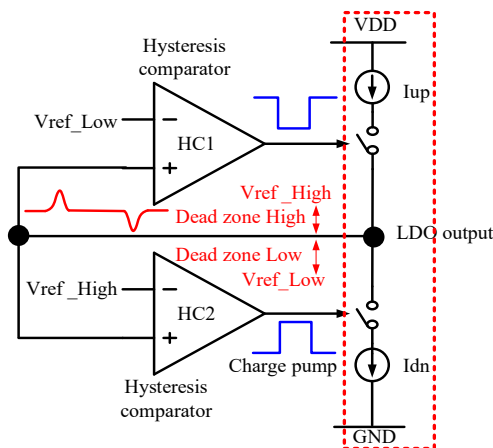
Fig. 6.9. The current regulation circuits (CRC) for transient time improvement
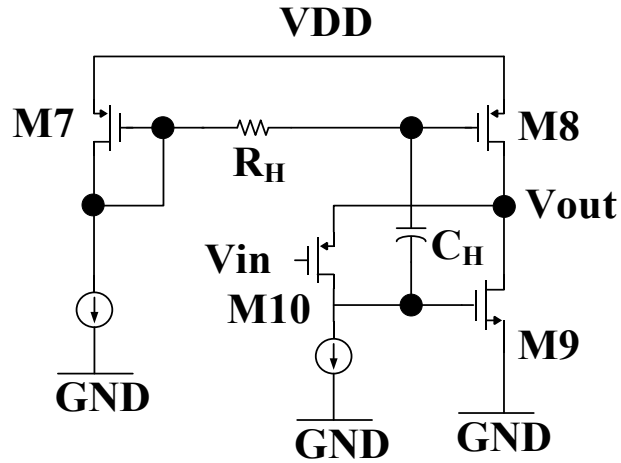
Fig. 6.10. The SSF with the class-AB performs as derivative path1

To provide stable and accurate voltage under the transient load change, the proposed CRC circuits shown in Fig.6-9 are applied to pre-reduce the settling time to overcome the transient speed
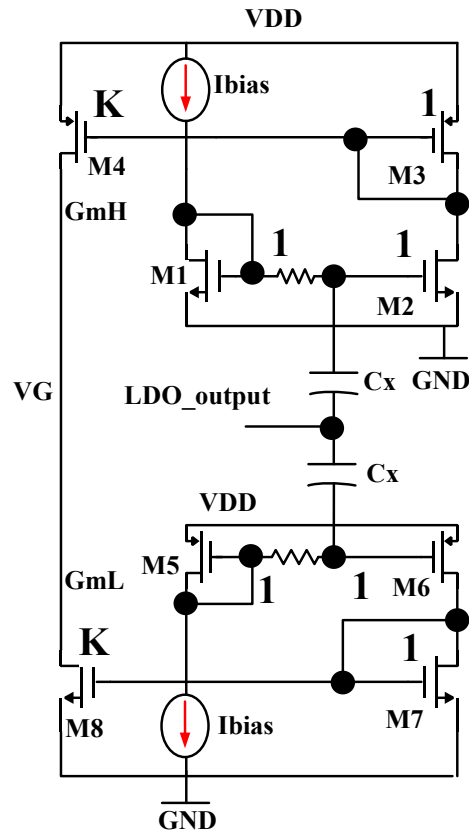
Fig. 6.11. The SRE performs as derivative path2
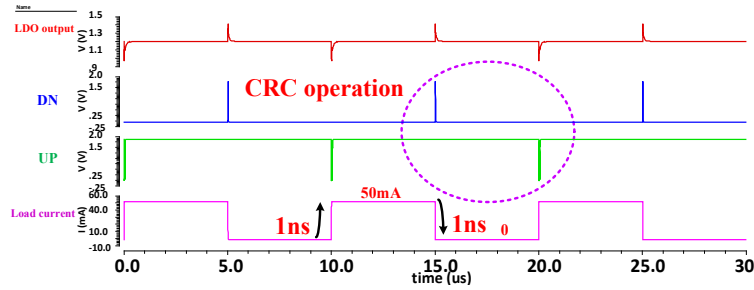
Fig. 6.12. The proposed LDO with ultra-fast dynamic response under load current rise/fall 1ns. C_{load} is 500 pF.
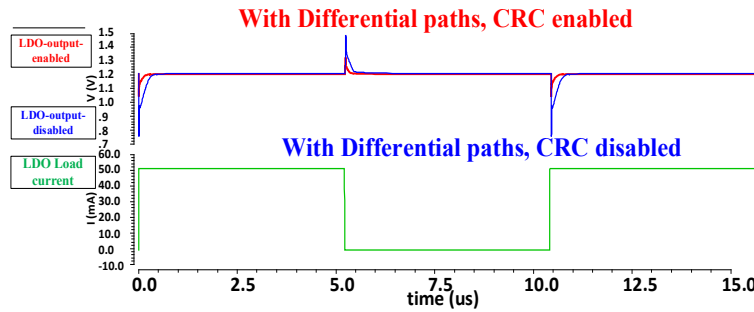
Fig. 6.13. Performance of proposed LDO with/without all techniques enabled under 500pF load capacitor

limitations governed by large-signal slew rate and small-signal closed-loop bandwidth. The CRC circuits incorporate assisted hysteresis comparators (HC1 and HC2) and a charge pump to perform fast initial dynamic loop recovery. Hysteresis comparators (HC1 and HC2) are added to the LDO as a fast auxiliary loop for transient output recovery when the load current has step changes. Moreover, to reduce power consumption, the CRC circuits are in a low standby quiescent current under small-signal operation, which will only wake up under initial transient load current change. In the event of an upward step change in the load current, an undershoot spike will be observed at the LDO output. When the undershoot spike triggers the comparator, the
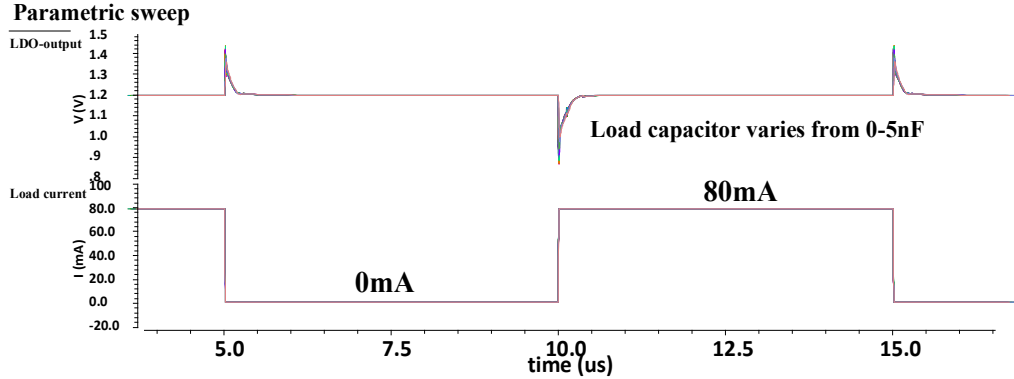
Fig. 6.14. Performance of the proposed LDO with load capacitor varies from 0-5nF under dynamic load currents ranging from 0-80mA

charge pump UP current will be switched on; An additional current I_{up} will flow into the load, thereby regulating the output voltage of the LDO to achieve rapid recovery from undershooting. Similarly, if the load current decreases and the LDO output displays an overshoot spike, the hysteresis comparators will turn on the Down current I_{dn}. The discharge current will flow from the load, resulting in the output of the LDO rapidly recovering from its overshoot. During the LDO settling process after the CRC operation is completed, loop dynamics behavior is always much slower than the load transient rising/falling change, and the power transistor behaves as a constant current source before entering the small-signal operation.

The maximum peaking occurs when the gate voltage of the power transistor is just entering its steady state. When the load current suddenly changes, two fast auxiliary loops (PID control operation), namely the super-source follower with the class-AB output stage and the proposed SRE circuits implementation, shown in Fig.6-10 and Fig. 6-11, compensate for the large-signal slew rate and constitute the essential part of the proposed LDO regulator. The differentiator forms the backbone of the slewing period providing both a fast transient detection path. The proposed design implements a coupling network (RC high pass filter), which senses the EA, and LDO output voltage simultaneously changes and transfers back in the form of a sinking/sourcing current. Fig. 6-10 shows a large resistor R_H connecting the gate of M_8 weakly to the gate of M_7, and a capacitor C_H connecting the gate of M_8 with the gate of M_9. DC characteristic indicates no current flows across R_H; hence, M_7 and M_8 have the same gate voltages. In terms of AC characteristics, a high-pass filter is formed with a cut-off frequency of $\frac{1}{2\pi R_H C_H}$. SSF Buffer can greatly enhance load regulation and transient performance. Upon propagating the AC signal from

the gate of M9 to the gate of M8, it becomes possible to achieve a class-AB transient response without introducing any additional static current consumption. The output impedance can be written as follows:

$$R_{out} = \frac{1}{g_{m10}(g_{m9}+g_{m8})(r_{o9}//(r_{o8}))} \tag{6-10}$$

where g_{m8-10} are the transconductances of M8-10 and r_{o8-9} are the output resistances of M8-9 in Fig.6.10. The LDO is fundamentally a PI controller with low-pass characteristics, while the SSF exhibits a high-pass characteristic. The proposed circuits extend the loop bandwidth while providing large-signal enhancement. The overall slew rate is analyzed as follows: If load current step ΔI_{load} is applied to the LDO, and the output ripple ΔV_{out} is inevitably generated; Δt_{settle} refers to the large-signal loop settling time. The current flowing through the SSF is supplied from C_{gate} until the LDO power transistor, Mp's drain current can compensate for I$_{load}$ and enable V$_{out}$ to return to a steady state. The SR of a transistor is dependent on the rate of gate variation of the pass transistor, which consists of two components:

$$\Delta V_{out} \approx \frac{\Delta I_{Load}\Delta t_{settle}}{C_L} \tag{6-11}$$

$$SR_{SSF} \approx + \frac{\Delta I_{SSF}}{C_{gate}} \tag{6-12}$$

The second derivative path2: SRE enables this critical advantage. In Fig.6.11, $G_{mH,L}$ is defined as the rate of change of ΔI_L or ΔI_H concerning ΔV_{out} as mentioned earlier, i.e.

$$I_{SRE} + \Delta I_{SRE} = K\frac{\beta_{1,5}}{2}[(V_{gs1-2} - V_{th1-2})^2 + 2(V_{gs1-2} - V_{th1-2})\Delta V_{out} + \Delta V_{out}^2]$$

$$G_{mH,L} = K\beta_{1,5}\Delta V_{out}$$

The magnitude of the derivative path term ΔI_{SRE} is extracted and is given by:

$$\Delta I_{SRE} = K\frac{\beta_{1,5}}{2}\Delta V_{out}[2(V_{gs1-2} - V_{th1}) + \Delta V_{out}] = K\beta_{1,5}\Delta V_{out}[(V_{gs1-2} - V_{th1}) + \frac{\Delta V_{out}}{2}]$$

$$SR_{tot} \approx + \frac{\Delta I_{SSF}}{C_{gate}} + \frac{\Delta I_{SRE}}{C_{gate}} \tag{6-13}$$

The auxiliary proposed differential paths are based on the capacitive coupling principle. This circuit works by temporarily taking advantage of the sudden voltage build-up at the LDO and the EA outputs to increase the bias current during the detection process. The LDO's transient response can be significantly improved with LDO's SR improvement. Fig.6.12 shows the simulated transient response. The load current changes with a rising/falling time of 1ns, and the output voltage recovers from the step changes within a short period. In this simulation, the load capacitance is 500pF, and the regulator is subject to a 0 ~ 100 mA load current change. Fig.6.13 shows the difference between enabling and disabling the proposed techniques under the same transient current. Compared with conventional LDO, the recovery time is significantly improved with the proposed techniques. The proposed CRC+ class-AB SSF + SRE and PAFC compensation approach make the output ring 4-5 times less. Fig.6-14 shows that the proposed LDO can drive a wide range of load capacitances from 0 to 5nF without sacrificing transient response.

6.3.3 HYBRID PASSIVE-ACTIVE FREQUENCY COMPENSATION

(a)- SMCNR-(Simple Miller Compensation with Nulling Resistor)

The RHP zero can be determined from the conventional Miller compensation by considering the feedforward small-signal current. One method, the SMCNR, for reducing the feedforward current to eliminate the RHP zero is shown in Fig. 6.15(a). Many publications focus exclusively on the effect of the nulling resistor on the zero position rather than the position of the poles. When the nulling resistor increases substantially, the compensation network is open-circuit, and pole splitting cannot be achieved. Thus, this compensation technique aims to increase the impedance of the capacitive path by inserting a nulling resistor in series with the compensation capacitor. However, the most severe drawbacks will occur when the amplifier drives large capacitive loads. To investigate the nulling resistor's value limit, the transfer function of the SMCNR is given by (6-14).
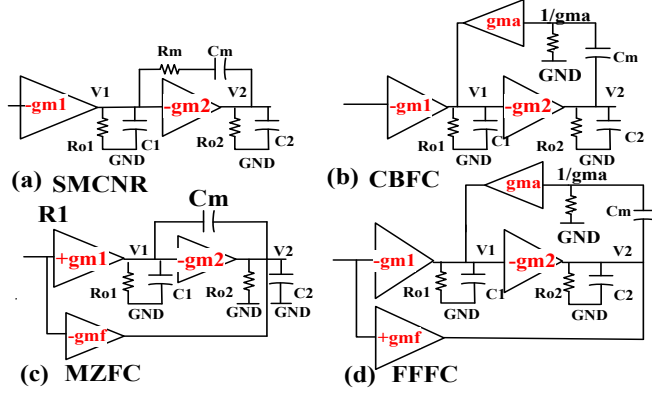
Fig. 6.15. Typical four different fundamental architectures for creating LHP zeros.

$$A_{vSMCNR}(s) \approx \frac{g_{m1}g_{m2}R_{o1}R_{o2}(1+sC_m(R_m-\frac{1}{g_{m2}}))}{(1+sC_m(R_m+g_{m2}R_{o1}R_{o2}))(1+s\frac{C_L(R_{o1}+R_m)R_{o2}}{R_m+g_{m2}R_{o1}R_{o2}})(1+sR_mC_1)} \qquad (6\text{-}14)$$

The previous equation shows that as R_m [Fig.6.15(a)] is increased, the poles will be shifted to lower frequencies, and their positions will be adjusted accordingly. The pole-splitting effect is diminished if R_m is too large. It is unsatisfactory from the conventional OTA or LDOs design point of view. However, in the proposed LDO design, we are taking advantage of this "non-pole splitting effect" to purposely choose a larger resistor value to introduce a passive zero $z_2 \approx -\frac{1}{C_mR_m}$ in the low-frequency within the loop bandwidth.

(b)-CBFC (Current Buffer Frequency Compensation)

Fig.6.15(b) shows that CBs obviate the feedforward path by introducing LHP zeros, thus improving phase margin (PM), stability, and gain bandwidth. Current buffer compensation with g_{ma} and capacitor C_m. Introducing an LHP zero at g_{ma}/C_m. The current mirror forms a non-inverting CB, which is referred to as a cascode compensation. The transfer function of the compensation circuit with the specific LHP zero is shown in (15).

$$A_{vCBFC}(s) \approx$$

$$\frac{g_{m1}g_{m2}R_{o1}R_{o2}(1 + \frac{sC_m}{g_{ma}})}{1 + s(g_{m2}C_mR_{o1}R_{o2}) + (R_{o1}R_{o2}C_1C_2 + R_{o1}R_{o2}C_mC_1)s^2}$$

$$z_1 = -\frac{gm_a}{C_a} \qquad \text{(Active-zero injection)} \tag{6-15}$$

Non-dominant pole and dominant pole by pole splitting effect can be calculated from the derivations of cascode frequency compensation as follows:

$$\omega_{p1(don)} \approx -\frac{1}{gm_2R_2C_mR_1} \tag{6-16}$$

$$\omega_{p2(non-don)} \approx -\frac{gm_2C_m}{C_1(C_2+C_m)} \tag{6-17}$$

Compared with SMCNR, the power bandwidth efficiency of CBFC is much higher; this is because the non-dominant pole under the same power consumption has been pushed to a higher frequency compared with SMCNR. Therefore, the proposed PAFC design adopts the CBFC architecture as part of the solution used as "pole-splitting" to secure the pole locations.

(c)- MZFC (Multipath Zero Frequency Compensation)

High-performance amplifiers or LDO circuits often require resistive load-driving capabilities. A Class-AB output stage reasonably controls the ratio between quiescent and maximum output current. Since the output current changes during the operation, gm_L, the transconductance of the last stage is not a constant, and the exact cancellation of the RHP zero by a fixed Rm is impossible when using SMCNR. The LDO may not be stable at a particular output current level. By utilizing MZFC, the RHP zero can be eliminated effectively while keeping the pole locations unchanged, reducing the design effort. The additional circuitry does not affect the poles' positions, which is the most crucial advantage of this approach. The transfer function derived from Fig.6.15(c) is

$$A_{vMZFC}(s) = -\frac{g_{m1}g_{m2}R_{o1}R_{o2}(1+sC_m(\frac{g_{mf}-g_{m1}}{g_{m1}g_{m2}}))}{(1+sC_mg_{m2}R_{o1}R_{o2})(1+s\frac{C_L}{g_{m2}})} \tag{6-18}$$

In this technique, the zero can be counteracted by adjusting g_{mf}. For canceling pole-zero ($Z_1 = P_2$) with each other, the value of g_{mf} can be obtained by:

$$g_{mf} = g_{m1}(1 + \frac{C_L}{C_c}) \tag{6-19}$$

Controlling g_{mf} and g_{m1} allows the zero to move to the LHP, according to (18). If $g_{mf} > g_{m1}$, the zero will be located at the LHP. From (19), The MZFC is power-effective when applied to small or medium load capacitances as well as large compensation capacitances. Two great advantages can be revealed from(18) and (19): (i) There is no change in the position of the poles by introducing MZFC. The locations of the poles are the same with SMC without nulling resistor; (ii) g_{m2} increases with an increase in output current. Consequently, the non-dominant pole and active zero will simultaneously move to a higher frequency and maintain a larger PM. Therefore, this compensation scheme allows for the stabilization over a much wider range of loading currents.

(d)-FFFC (Feedforward Feedback Frequency Compensation)

The FFFC has shown in Fig.6.15(d) combined all the previously mentioned advantages, including MZFC and CBFC. The transfer function can be written as:

$$A_{vFFFC}(s) \approx$$

$$\frac{g_{m1}g_{m2}R_{o1}R_{o2}(1+\frac{sC_m}{g_{ma}})(1+\frac{sg_{mf}R_{o1}C_1}{g_{mf}+g_{m1}g_{m2}R_{o1}})}{1+s(g_{m2}C_mR_{o1}R_{o2})+(R_{o1}R_{o2}C_1C_2+R_{o1}R_{o2}C_mC_1)s^2} \tag{6-20}$$

Two LHP zeros are:

$$z_1 = -\frac{gm_a}{C_m} \quad \text{(Active-zero1 injection)} \tag{6-21}$$

145

$$z_2 = -\frac{g_{mf}+g_{m1}g_{m2}R_{o1}}{g_{mf}R_{o1}C_1} \quad \text{(Active-zero2 injection)} \tag{6-22}$$

Since it is efficient in terms of GBW, a CBFC with the compensation capacitor can be used in the frequency compensation. The input resistance of the CBFC is ($\frac{1}{g_{m3}}$), and the compensation capacitor C_m can also introduce an LHP zero to increase the phase margin. However, this structure alone does not provide a sufficient slew rate and cannot directly control the non-dominant complex poles in multistage amplifiers or complex LDO designs, which might cause instability. On the other hand, FFFC architecture hybrid by CBFC and MZFC structure guarantees the loop stability within a wide dynamic range by introducing an extra LHP zero, providing a sufficient slew rate, and adequately controlling the Q value of the non-dominant complex poles.

(e)-Feedforward Stage Selection Considerations in Multistage Small-Signal Designs

(a)

(b)

(c)
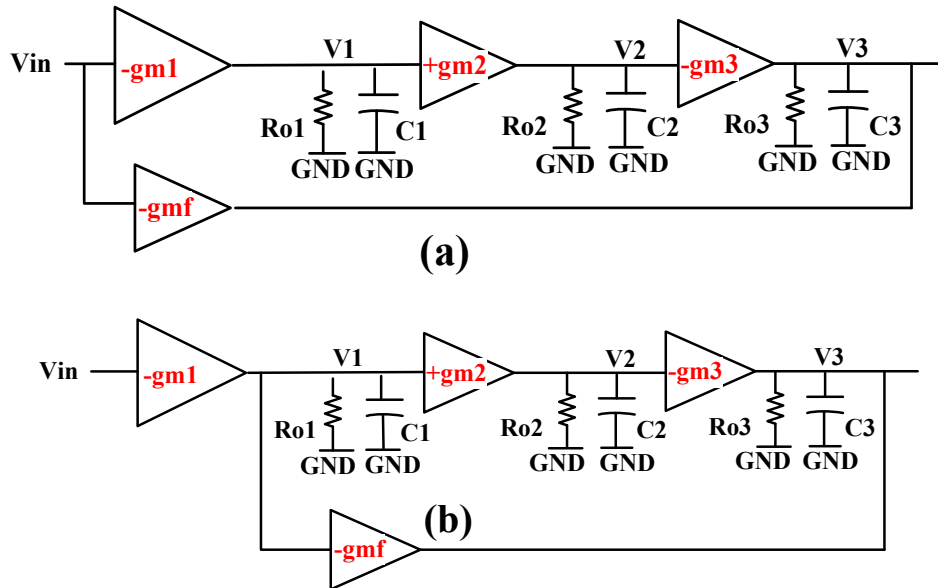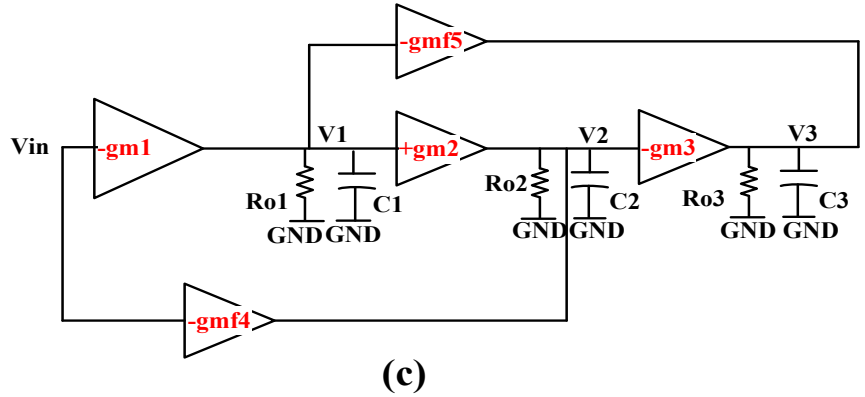
Fig. 6.16 Typical three feedforward topologies

(a)

(b)
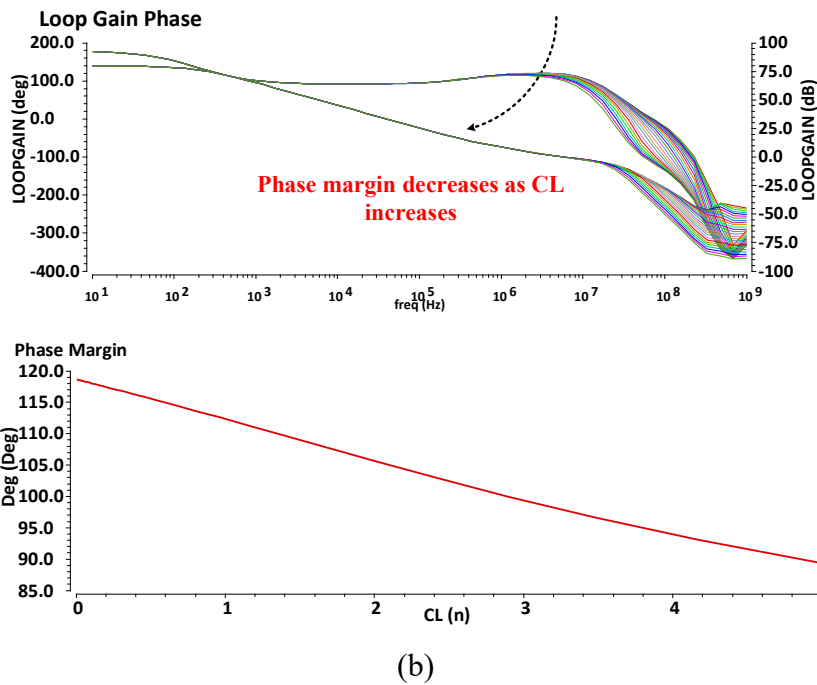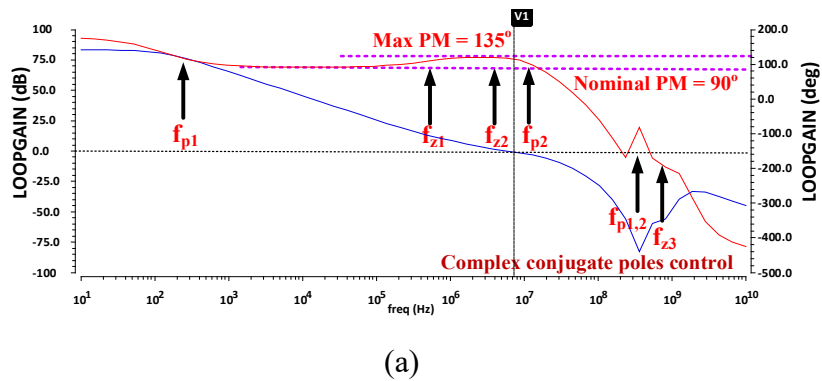
Fig. 6.17. (a) The proposed LDO AC response with pole-zero locations for 500pF load. (b)The proposed LDO with ultra-large dynamic range under load variations.

As previously mentioned, one of the most significant advantages of MZFC is that MZFC techniques do not change the positions of the poles. Fig.6.16 illustrates three typical scenarios that might be potentially applied to designs with the same transfer function denominator. Hence the stability will not be considered in MZFC techniques. The input stage active feedforward compensation structure is shown in Fig.6.16 (a). This structure supplies g_{mf} to the last stage output through the first stage input, resulting in two different real zeros. This type of MZFC might accidentally bring one or two zeros to the right-half plane (RHP) and reduce the circuit's phase margin. In Fig. 6.16(b), where the feedforward stage is inserted at the output of the first Gm stage, MZFC behaves very differently. The stability is improved because the feedforward gain stage gmf can adequately control the non-dominant complex poles to ensure stability. Therefore, the proposed LDO uses the second situation (b) as the feedforward stage. In addition, the feedforward stage creates a push-pull output to increase the slew rate of the LDO. Another commonly used structure shown in Fig. 6.16(c) can also solve the issues in the active-feedback current buffer frequency compensation [17-20] with high power consumption. Without feedforward paths, we have seen that the CBFC technique would place the LHP zeros at a high frequency, which does not benefit from the phase margin attributed to the non-dominant real pole and complex poles. Thus, these zeros cannot remove the significant negative phase shift due to the real pole and non-dominant complex poles. In addition, multi-feedforward paths used in this structure provide two features. g_{mf5} is used to suppress the Q value of the complex poles at the expense of extra quiescent current draining from the power transistor to the ground. The dynamic feedforward path formed by g_{mf4} enhances the transient response of the last stage g_{m3}. In summary, the structure in Fig. 6.16(b) was used due the following reasons: (i) g_{m2} is designed to be a Super-Source Follower (SSF) with the built-in class-AB operation to increase the slew rate., (ii) The feedforward path control the LHP zero at the high frequency, which can adjust the Q-factor of the complex poles, stabilizing the loop. (iii) Low power consumption can be achieved as compared to Fig.16(c) as fewer components are used. The transfer functions of all the discussed compensations techniques are listed in Appendix. A.

The actual implementation is shown in Fig.6.4. The circuit is presented as an open-loop small-signal model consisting of a first-stage amplifier (-G_{m1}), a second-stage buffer (+G_{m2}), and an output transistor (-G_{mp}). Active-passive feedback for phase margin boosting, feedforward gmf stage for complex conjugate poles control (Q-control). One low-frequency dominant LHP zero is given as

$$z_1 = -\frac{gm_a}{C_a + C_B}(\text{Active-zero injection}) \qquad (6\text{-}23)$$

Two non-dominant high-frequency zeros are given as:

$$z_2 = -\frac{1}{C_{a1}R_{a1}}(\text{Passive-zero injection}) \qquad (6\text{-}24)$$

$$z_3 = -\frac{g_{m2}g_{m3}}{g_{mf}C_2} \ (\text{feedforward zero Q-control}) \qquad (6\text{-}25)$$

Non-dominant pole and dominant pole within the small-signal bandwidth by pole splitting effect can be calculated from the derivations of cascode frequency compensation as follows:

$$\omega_{p1(don)} = -\frac{1}{gm_3R_3(C_{a1}+C_a)R_1} \qquad (6\text{-}26)$$

$$\omega_{p2(non-don)} = -\frac{gm_3C_a}{C_{EAout}(C_L+C_a)} \qquad (6\text{-}27)$$

The PM is

$$PM = 90 - arctan(\frac{\omega_{GBW}}{\omega_{p2}}) + \sum_{i=1}^{3} arctan(\frac{\omega_{GBW}}{\omega_{zi}}) - \sum_{i=1}^{2} arctan(\frac{\frac{\omega_{GBW}}{\omega_{cpi}}}{Q[1-(\frac{\omega_{GBW}}{\omega_{cpi}})^2]}) \qquad (6\text{-}28)$$

Figure 6.17(a) shows the proposed LDO small-signal transfer function, referred to as the open-loop AC response. Comparisons were made between the AC responses, the theoretical pole, and zero locations. A plot of PM is shown in Fig. 6.17(b) concerning the output load capacitance, the entire range of output load capacitance, PM remains between 125° and 85°. The small variation in PM with load capacitance over 0-5nF confirms the effectiveness of the proposed compensation scheme for PAFC.

6.4 EXPERIMENTAL RESULTS AND CONCLUSIONS
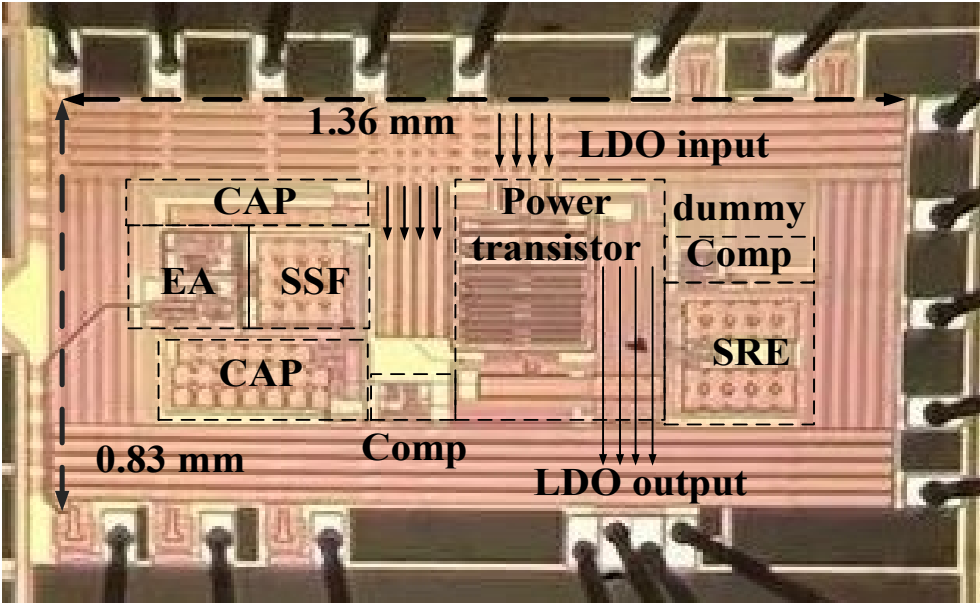
Fig. 6.18. The layout of the chip die for the proposed LDO.
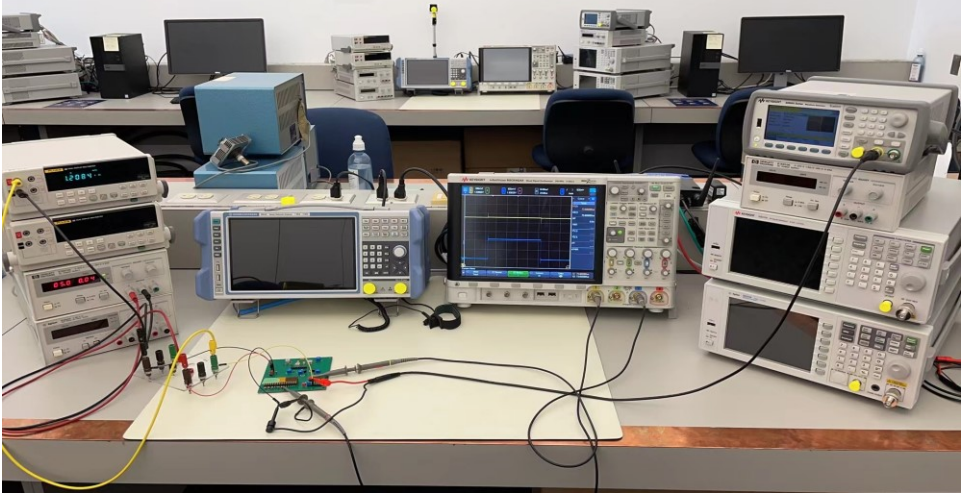
Fig. 6.19. Experimental setup of proposed LDO.
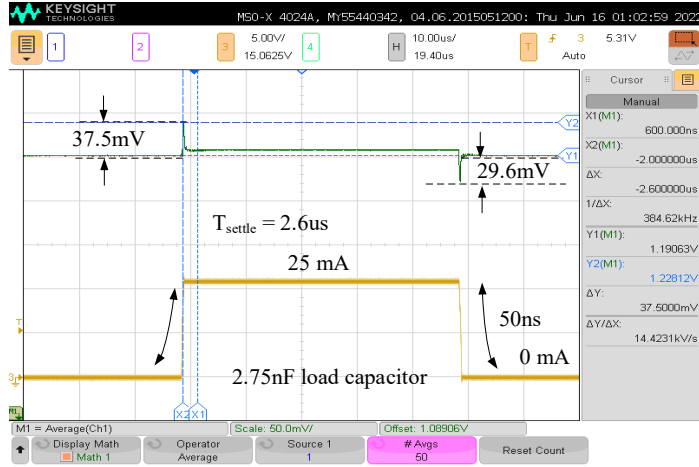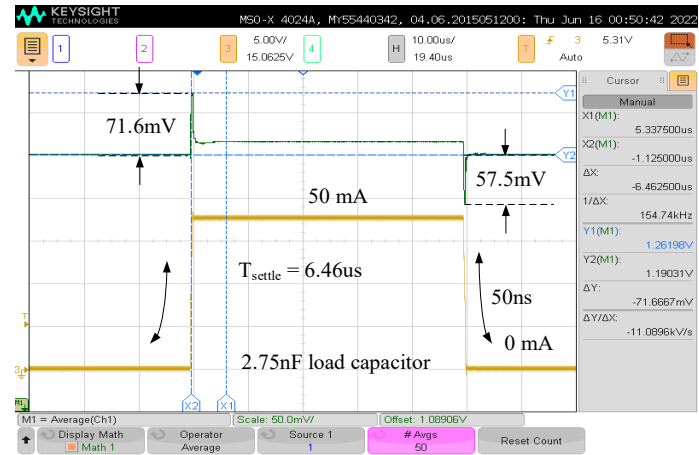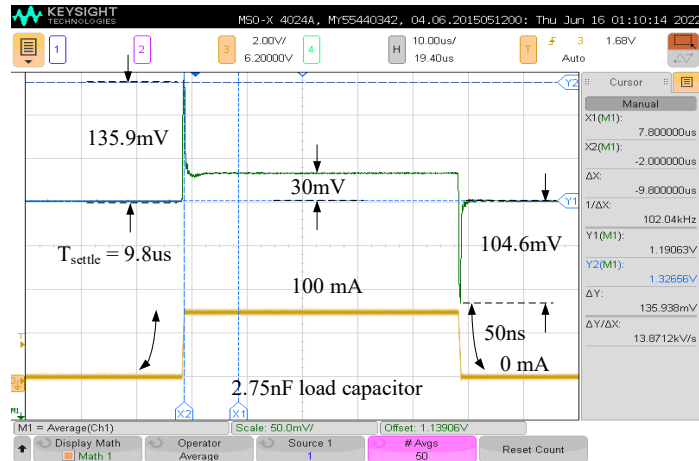
Fig. 6.20. Measured waveforms of load transient response with load step rise/fall time 50ns (a) between 0 and 25 mA. (b) between 0 and 50 mA. (c) between 0 and 100 mA.

The proposed ultra-high-speed LDO with a piecewise speed enhancement was implemented in TSMC 0.18-μm 1.2 V CMOS technology. Fig.6.18 shows the micrograph of the fabricated chip with bonding wire connecting to a DIP40 package. The area of the chip is 1.12 mm^2, excluding the test pads. The quiescent current is 380 μA at no-load. A DC power supply, PCB evaluation board, Keysight oscilloscope, and function generator have been adopted to extract the measurement results shown in Fig.6.19. The measured transient response is shown in Fig. 6.20 with a 2.75nF load under three load currents, 25mA, 50mA, and 100mA, having a rising/falling transition of 50 ns, the desired output is 1.2 V. It can be observed that the transient overshoot, undershoot measured transient response is shown in Fig. 6. 20 with a 2.75nF load under three load currents, 25mA, 50mA, and 100mA, having a rising/falling transition of 50 ns, the desired output is 1.2 V. It can be observed that the transient overshoot, undershoot were obtained with 50mA step change, shown in Fig. 6.20(b). 135.9mV, 104.6mV, and 9.8us were the results of 100mA step change, shown in Fig. 6.20(c).
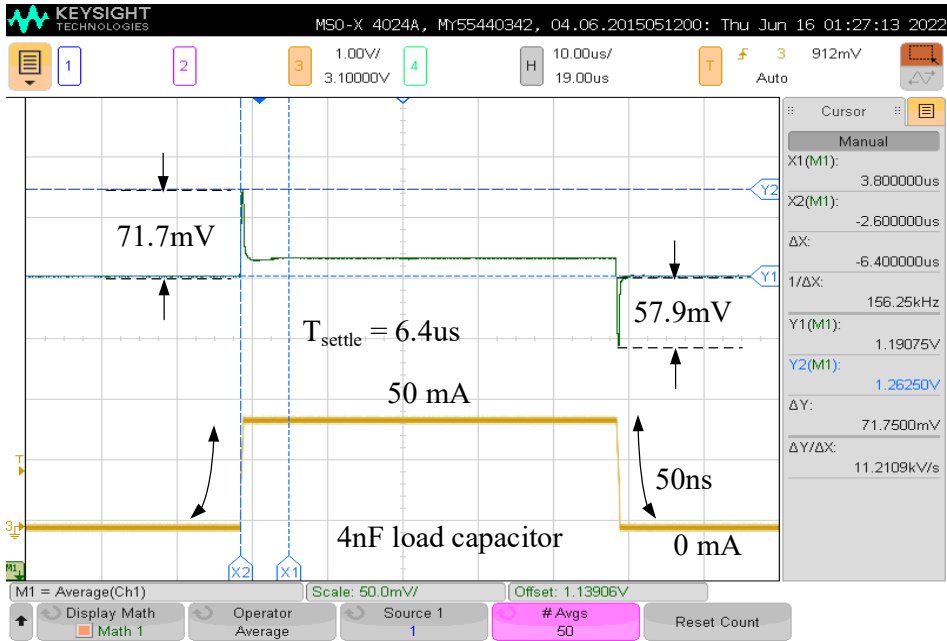
(a)
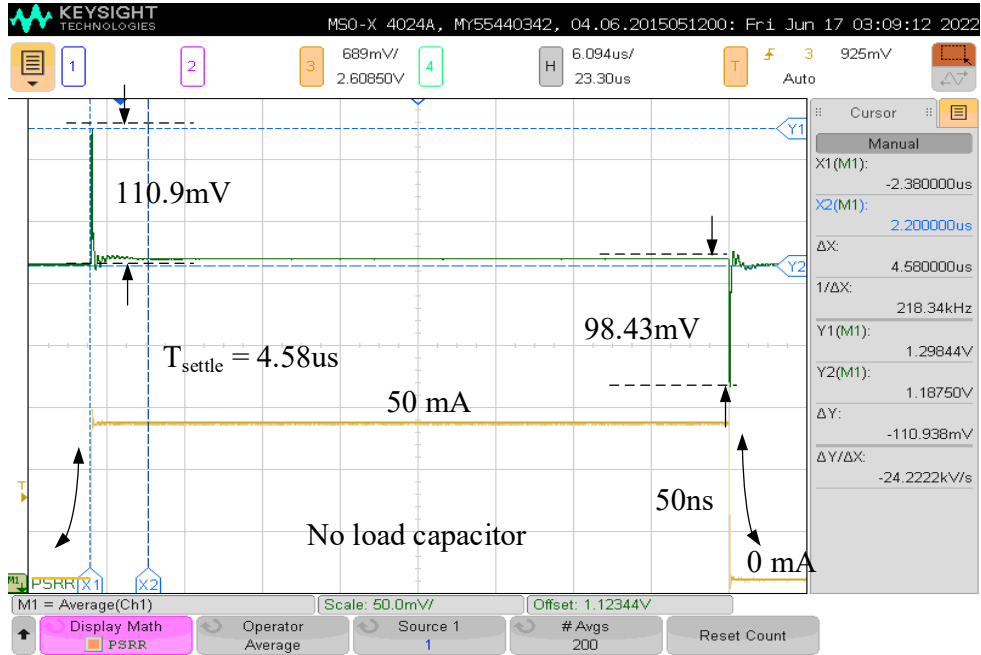
(b)

Fig 6.21. Time-domain transient response under different load capacitors (a) load capacitor 4nF. (b) no-load capacitor.
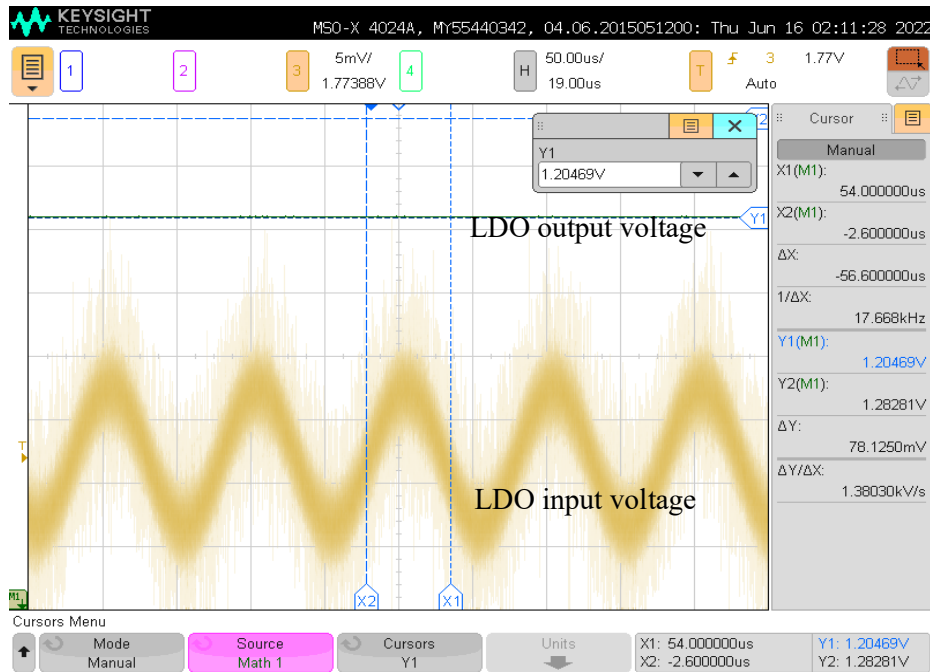
(a)

(b)

Fig. 6.22. LDO's PSRR measurement results under the same load capacitance (a) time-domain noise rejection (b) frequency performance measured with a small signal injection sweep method with the no-load current.
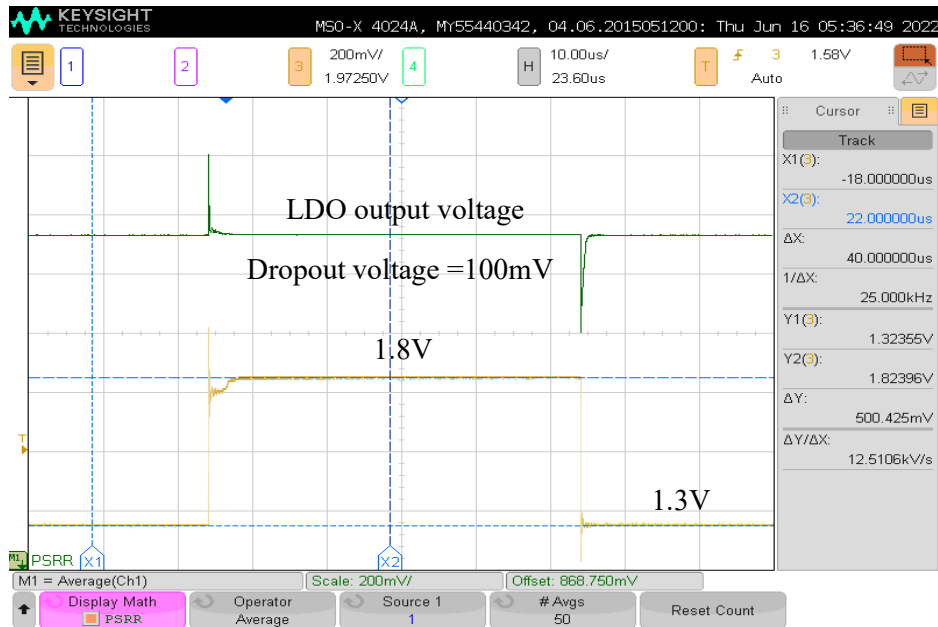
Fig.6.23 Line regulation transient response when input voltage changes from 1.8 V to 1.3 V at 10mA constant load current.
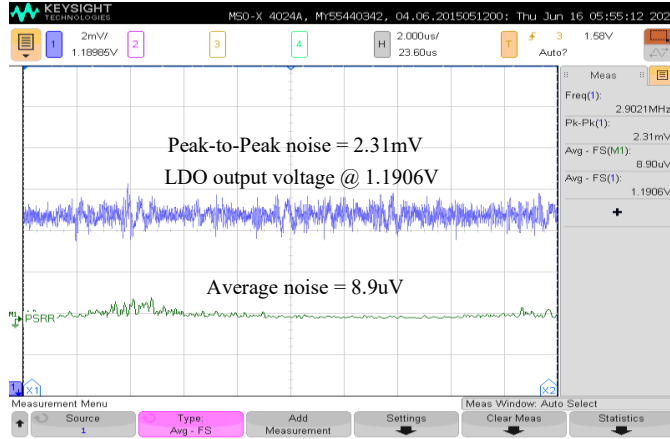
Fig.6.24 measured LDO output transient noise and average time-integrated noise.

The observed undershoot, the overshoot, and the recovery time of the proposed LDO proportionally increase, respectively, from 2.6 μs, 6.46 μs, and 9.8 μs. Fig. 6.21(a)-(b) shows two cases with different load capacitors: 4nF and no-load large capacitive load. The undershoot, overshoot and recovery times for no-load cases are 6.4 μs and 4.58 μs (Fig. 6.21(a)-(b)). Notice that the proposed piecewise speed enhancement with a hybrid passive-active frequency compensation technique can provide a constant 1.2V output voltage with a well-behaved settling characteristic under large load variations.

As a result of the proposed piecewise speed enhancement, undershoot and overshoot were very small when Vout was at 1.2V. Figures 6.20 and 6.21 show the small transient settling time variations and ultra-wide stability conditions obtained under significant load capacitor variations. As a result, it is demonstrated that the hybrid passive-active frequency compensation procedure can provide a well-behaved settling characteristic to an LDO. Fig. 6.22 shows the measurement of the PSRR of the proposed LDO. The DC bias voltage and AC small-signal periodic sinusoidal waves are summed together and applied at the input of the LDO. V_{DC} is the operating point bias voltage, and V_{sin} is the noise source used in the test. To improve measurement accuracy, a high bandwidth amplifier is recommended to be used as a summing node to inject the signals and provide isolation between V_{sin} and V_{DC}. To minimize the effects of setup impedance on V_{in} and V_{out} of the LDO, high-impedance probes should be used. The measured PSRR time-domain and frequency-domain described in Fig. 6.22 show the PSRR at 100Hz low frequency is -45dB and -27dB at 1MHz high frequency. Fig. 6.23 illustrates the line transient response, according to which the implication of an input voltage varying up to the output voltage limit is outside the stability margin. When the change in the input voltage was from 1.8V to 1.3V, the

approximated dropout voltage of the proposed LDO is 100mV. Fig. 6.24 shows the noise performance of the LDO; The total integrated LDO output noise is more practical since all the noise will be folded in frequency and integrated by the system. Table 6.2 summarised the performance with other recent works.

TABLE 6.2 Results and Comparison with Other Works

Parameters	This work	[6]	[23]	[9]	[18]	[31]
Year	**2022**	2011	2014	2016	2018	2019
Dropout (V)	**0.1**	0.1	0.2	0.4	0.2	> 0.2
Settling time	**< 4us**	0.1s	1.65us	5us	< 1us	> 1s
Capacitor range	**0-10nF**	NA	10pF-10nF	600pF	100pF	NA
Technology	**180nm**	130nm	65nm	180nm	130nm	250nm
Supply (V)	**1.8-1.3**	0.9	1.2	1.6-2	2.5-1.4	3.9-10
Vout (V)	**1.2**	0.8	1	1.2	1.2	2.5
Imax (mA)	**100**	50	50	10	50	500
IQ (µA)	**380**	1.3	25	300	65.8	450
Output capacitor (µF)	**Cap-free**	Cap-free	On-chip 20pF	Cap-free	On-chip 2.6pF	22
Load regulation (mV/mA)	**0.005**	NA	0.034	4	0.048	0.03

6.5 CONCLUSION

The analysis and design of an ultra-high-speed LDO were presented. The proposed design applies to high-speed digital SoCs. A detailed investigation of the principles of the frequency compensation techniques was compared, proving the effectiveness of the proposed circuit in the slew rate loop-bandwidth enhancement. The mathematical treatment of circuit topologies was provided. We showed that in the presence of a PID-control mechanism formed by EA, SSF with the class-AB operation, PAFC, and the CRC circuit, the proposed LDO significantly improves the time of reaching steady-state under large load variations. The measurement results showed that the output would reach 1.2V in less than 10us under 100mA load current change and 2.75nF load capacitor, while the settling time could be reduced to 2.6µs when the load current was 25mA.

CHAPTER 7 CONCLUSION

This chapter summarizes the contributions in this thesis. Additionally, suggestions for future work are presented.

7.1 CONCLUSIONS

This dissertation aims to design and implement highly integrated analog front-end sensors for use in applications such as smart sensor arrays within wireless sensor networks (WSNs) as well as in chemistry, biology, and biomedicine. Low-power and high-sensitivity LIA was implemented in a 180-nm CMOS technology that can easily be interfaced with or integrated with digital signal processors. The complete integrated circuit design of the sensor node included noise-shaping SAR-ADCs with DLAFC-based driver amplifier input buffers. Also, high PSRR, low noise, and high-order curvature-compensated bandgap voltage reference are implemented as the reference voltage as well. Finally, we implemented an ultra-high-speed LDO with slew rate loop bandwidth enhancement to offer clean power supply voltage with strong capacitive driving capability. The proposed LIA, BGR, and LDO designs in this thesis are supported by experimental results.

Chapter 2 proposes a fully integrated single-channel, analog LIA to reduce power consumption and the size of passive components by taking advantage of a new signal power detection scheme based on 2nd order harmonic extraction and automatic phase alignment technique. The proposed LIA utilizes $2\omega_c$ harmonic instead of DC signal to improve the transient response of the LIA and overcome the 1/f flicker noise limitation with a built-in chopping technique to improve the SNR of the entire system. The automatic phase tuning mechanism for phase alignment between the reference and input signals is also proposed.

Chapter 3 proposes a novel high-speed SAR-ADC with 2nd-order noise shaping. The noise shaping technique is designed as a passive-active arrangement, utilizing a low-gain, open-loop amplifier with positive feedback. This implementation reduces the area required for passive integrator noise shaping

and compensates for passive implementation's gain and phase errors. A common-mode stabilization technique is proposed along with the monotonic switching technique, which prevents the common-mode level shift during SAR conversion and helps to improve the circuit's performance. The circuit's simulation results in 180nm achieving an SNDR of 89.4 dB, an SFDR of 98.6 dB, and a THD of 0.0003%. The power consumed is 880 uW at a supply voltage of 1.8V.

Chapter 4 proposes a DLAFC-based driver amplifier is presented. The theoretical analysis and simulation results show good agreement regarding excellent DC gain, GBW, speed, input-referred noise and THD, which is suitable for high-speed applications. Moreover, the proposed amplifier is proven stable in most extreme PVT variations to validate the design robustness. The proposed amplifier has competitive performance compared with state-of-art amplifiers used as products.

Chapter 5 proposes a novel high PSRR, low noise, and high-order curvature-compensated bandgap voltage reference with a measured temperature coefficient of 5-15 ppm/^{o}C, and supply current consumption of 150 μA under a 3.3V power supply. The output buffer with a switched RC LPF is used to reduce the BGR noise further, save area and increase BGR PSRR. The chopping technique is applied in the error amplifier to significantly reduce the BGR output noise and input offset to allow the proposed BGR to work in low-noise applications. Finally, several silicon tests have been conducted to demonstrate the feasibility of the proposed curvature-compensated bandgap voltage reference.

Chapter 6 proposes an ultra-high-speed LDO were presented. The proposed design applies to high-speed digital SoCs. A detailed investigation of the principles of the frequency compensation techniques was compared, proving the effectiveness of the proposed circuit in the slew rate loop bandwidth enhancement. The mathematical treatment of circuit topologies was provided. We showed that in the presence of a PID-control mechanism formed by EA, SSF with the class-AB operation, PAFC, and the CRC circuit, the proposed LDO significantly improves the time of reaching steady-state under large load variations. The measurement results showed that the output would reach 1.2V in less than 10us under 100mA load current change and 2.75nF load capacitor, while the settling time could be reduced to 2.6μs when the load current was 25mA.

7.2 FUTURE WORK

In light of this study's theoretical and measurement results, future investigations are recommended to enhance the performance of the proposed analog front-end sensor system presented in this thesis as follows.

Sensor interface (a fully integrated single-channel, analog LIA):

➤ The proposed LIA requires a highly selective BPF design, which considers flicker noise and THD[3] as the major design challenge. Future work can focus on how to design low-power, high Q, and low crossover distortion fully differential bandpass filters for very low-frequency applications.

➤ The design of the Envelop detector may be optimized to reduce power while still guaranteeing PVT insensitive, highly linear, and low-distortion performance.

➤ An automatic gain calibration (AGC) may be considered included in the signal channel, allowing the gain of such channel to be variable according to the input signal power, thus reducing total power consumption.

➤ The mixer circuit may be optimized to reduce power but still guarantee a large dynamic range, small offset drift, adjustable time constant, and good linearity, which may be a challenge.

Back-end ADC (novel high-speed SAR-ADC with 2nd-order noise shaping):

➤ The passive implementation of the resonator degrades the filter performance due to the charge redistribution among C_{s1}, C_{s1r}, and the CDAC. This can be further improved by a more advanced noise-shaping loop filter scheme.

➤ A dynamic amplifier that may be more power-efficient to replace the Gm-R open-loop amplifier is employed in the current NS filter in this work.

ADC Driver amplifier (DLAFC-based driver amplifier) :

➢ The proposed amplifier is also required to be stable in most extreme PVT variations under low voltage applications to reduce power consumption and has competitive performance compared with state-of-art amplifiers used as products.

The reference voltage (a novel high PSRR, low noise, and high-order curvature-compensated bandgap voltage reference):

➢ The sample-to-sample variation is quite large (~50mV). As part of the future BGR design, offset trimming circuits will be included to precisely trim the BGR output voltage.

➢ The proposed BGR occupies a large area. The proposed pre-regulator and SC filter will be further refined to reduce power and area.

➢ On-chip high-precision RC oscillator will be added, and the optimized chopping frequency can be further investigated and proved by mathematical equations.

CAP-less on-chip LDO (ultra-high-speed LDO with slew rate loop bandwidth enhancement):

➢ Analog circuits cannot benefit from the scaling CMOS process and are incompatible with the standard digital design flow. Great design efforts are still required as the fabrication process continues to update, and the transistors' descending supply voltage and intrinsic gain have made the design of analog circuits even harder. In order to overcome the disadvantages of conventional analog LDOs, digital LDOs have been proposed. Digital LDOs, unlike their analog counterparts, are highly scalable and can work in the near-threshold or subthreshold regions. Digital LDOs can be synthesized as other digital functional blocks inside the SoC and, consequently, can be easily integrated. In order to combine the advantages of both analog and digital architectures, a digitally assisted dual-loop (DADL) LDO will be used in future LDO designs.

BIBLIOGRAPHY

[1] Principles of coherent communication, A. J. Viterbi, McGraw- Hill, 1966 - 321 pages.

[2] Blair, D.P.: 'Phase sensitive detection as a means to recover signals buried in noise', J. Phys. E, Sci. Instrum., 1975.

[3] Lock-in amplifiers and preamplifiers, Princeton Appl. Res. Corp., data sheets, 1971

[4] J. Aguirre, D. García-Romeo, N. Medrano, B. Calvo and S. Celma, "Square-Signal-Based Algorithm for Analog Lock-In Amplifiers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5590-5598, 2014.

[5] A. De Marcellis, G. Ferri and A. D'Amico, "One-Decade Frequency Range, In-Phase Auto-Aligned 1.8 V 2 mW Fully Analog CMOS Integrated Lock-In Amplifier for Small/Noisy Signal Detection," IEEE Sensors Journal, vol. 16, no. 14, pp. 5690-5701, July 2016.

[6] P. Maya, et al., "Low-Cost Autonomous Lock-in Amplifier for Resistance/Capacitance Sensor Measurements.", *Electronics*, vo. 8, no. 12, pp. 1413, Nov. 2019.

[7] D. Amico, A., De Marcellis, A., Di Carlo, C., et al.: 'Low-voltage low power integrated analog lock in amplifier for gas sensor applications', *Sens. Actuators B, Chem.*, 2010, 144, (2), pp. 400–406.

[8] A. Hu and V. P. Chodavarapu, "CMOS Optoelectronic Lock-In Amplifier With Integrated Phototransistor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 274-280, Oct. 2010

[9] De Marcellis, A., Ferri, G., Mantenuto, P., and D'Amico, A.: 'A new single-chip analog lock-in amplifier with automatic phase and frequency tuning for physical/chemical noisy phenomen detection'. Proc. IEEE 5th Int. Workshop on Advances in Sensors and Interfaces (IWASI), Bari, Italy, June 2013, pp. 121–124

[10] H. H. Alamdari, K. El-Sankary, and G. N. Maksym, "Time-Varying Respiratory Mechanics as a Novel Mechanism Behind Frequency Dependence of Impedance: A Modeling Approach," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 66, no. 9, pp. 2433-2446, Sept. 2019.

[11] G. Begin. K. M. AL-Tamimi, H. H. Alamdari, D. Roach, M. Schmidt, and K. El-Sankary, "Respiratory Bidirectional Ultrasonic TOF Flow Sensor Resilience to Ambient Temperature Fluctuations," *IEEE Sensors Journal*, vol. 12, no. 17, pp. 18920 - 18931, Sept. 2021.

[12] G. Krause, et al.: "1/f noise analysis of a 75 nm twin-flash™ technology nonvolatile memory cell," 7th Annu. Non-Volatile Mem. Technol. Symp. NVMTS (2006) 12.

[13] L. S. Levitov and G. B. Lesovik: "Charge distribution in quantum shot noise," Jetp Lett. C/C Pis'Ma V Zhurnal Eksp. Teor. Fiz. 58 (1993) 230.

[14] A. Van Der Ziel: "Thermal noise in field-effect transistors," Proc. IRE 50(1962) 1808.

[15] Stanford Research Systems: "About lock-in amplifiers," Appl. Note. (2011) 1.

[16] G. Giusi, et al.: "Ultra-low-noise large-bandwidth transimpedance amplifier," Int. J. Circuit Theory Appl. 43 (2015) 1455 (DOI: 10.1002/cta.2015).

[17] E. Kamrani, et al.: "Low-noise, high-gain transimpedance amplifier integrated with SiAPD for low-intensity near-infrared light detection," *IEEE Sensors Journal*, vol. 14, no. 1, pp. 258-269, Jan. 2014.

[18] G. Ferri, et al.: "A low-voltage integrated CMOS analog lock-in amplifier prototype for LAPS applications," *Sens. Actuators A Phys.* 92 (2001) 263.

[19] M. L. Meade: "Lock-in amplifiers: principles and applications," Peter Peregrinus Ltd on behalf of the Institution of Electrical Engineers.

[20] F. N. Hooge, et al.: "Experimental studies on 1/f noise," Rep. Prog. Phys. 44 (1981) 479 (DOI: 10.1088/0034-4885/44/5/001).

[21] H.-H. Son, et al.: "Signal detection technique utilising 'lock-in' architecture using 2ωc harmonic frequency for portable sensors," *Electronics Letters* 46 (2010) 891.

[22] W. Oh, B. Bakkaloglu, C. Wang and S.K. Hoon, "A CMOS low noise, chopper stabilized low-dropout regulator with current-mode feedback error amplifier," *IEEE Trans. Circuits and Syst. I: Reg. Papers,* vol.55, no.10, pp.3006-3015, Nov. 2008.

[23] H.-K. Chiou and H.-Y. Chung: "2.5–7 GHz single balanced mixer with integrated Ruthroff-type balun in 0.18μm CMOS technology," *Electronics Letters* 49 (2013) 474.

[24] S.-G. Mao, et al., "Design and modeling of uniplanar double-balanced mixer," *IEEE Microwave Guided Wave Letters* 8 (1988) 354

[25] J. Wang, et al., "A 5-bit 500 MS/s flash ADC with temperature-compensated inverter-based comparators," Solid State Electronic Letters, vol. 2, pp.1-9, 2020.

[26] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS Threshold- Compensated RF Energy Harvester," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011.

[27] Z. Hameed and K. Moez, "Fully-integrated Passive Threshold Compensated PMOS Rectifier for RF Energy Harvesting," in *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2013, pp. 129–132.

[28] Cheung Fai Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC- DC converter with on-chip current-sensing technique," in IEEE Journal of Solid-State Circuits, vol. 39, no. 1, pp. 3-14, Jan. 2004, doi: 10.1109/JSSC.2003.820870.

[29] Fredenburg, J. A., & Flynn, M. P. (2012). A 90-Ms/s 11-MHz bandwidth 62-dB sndr noise-shaping sar adc. IEEE Journal of Solid-State Circuits, 47, 2898–2904.

[30] Chen, Z., Miyahara, M., & Matsuzawa, A. (2016). A second-order fully-passive noise-shaping SAR ADC with embedded passive gain. In 2016 IEEE Asian Solid-State Circuits Conference (ASSCC) (pp. 309–312).

[31] Chen, Z., Miyahara, M., & Matsuzawa, A. (2016). A 9.35-ENOB, 14.8 fJ/conv.-step fully passive noise-shaping SAR ADC. IEICE Transactions on Electronics, 99, 963–973.

[32] Guo, W.n, Zhuang, H., & Sun, N. (2017). A 13b-ENOB 173dBFoM 2 nd-order NS SAR ADC with passive integrators. In 2017 Symposium on VLSI Circuits (pp. C236–C237).

[33] Payandehnia, P., Mirzaie, H., Maghami, H., Muhlestein, J., & Temes, G. (2017). Fully passive third-order noise shaping SAR ADC. Electronics Letters, 53, 528–530.

[34] Yi, P., Zhu, Z., Li, D. *et al.* An opamp-free second-order noise-shaping SAR ADC with 4× passive gain using capacitive charge pump. *Analog Integr Circ Sig Process* **105,** 125–133 (2020).

[35] Shikata A, Sekimoto R, Kuroda T, et al. A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS. IEEE J Solid-State Circuits, 2012, 47(4): 1022

[36] Y. Song, C. Chan, Y. Zhu, L. Geng, S. U. and R. P. Martins, "Passive Noise Shaping in SAR ADC With Improved Efficiency," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 2, pp. 416-420, Feb. 2018, doi: 10.1109/TVLSI.2017.2764742.

[37] Z. Chen, M. Miyahara and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," 2016 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2016, pp. 309-312, doi: 10.1109/ASSCC.2016.7844197.

[38] Ginsburg B P, Chandrakasan A P. "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC". IEEE Int Symp Circuits and Systems (ISCAS), 2005

[39] Liu CC, et al. "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 _m CMOS process". Symposium on VLSI Circuits Digest of Technical Papers, 2009.

[40] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill, Inc, 2000

[41] Schinkel D, et al. "A double-tail latch-type voltage sense amplifier with 18 ps Setup+Hold time", IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2007

[42] Chen M, Brodersen W. A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-_m CMOS. IEEE J Solid-State Circuits, 2006, 41(12): 2669

[43] Promitzer G. "12-bit low-power fully differential non calibrating successive approximation ADC with 1 MS/s". IEEE J Solid-State Circuits, 2001, 36(7): 1138

[44] Agnes A et al. « A 9.4-ENOB 1 V 3.8 W 100 kS/s SAR ADC with time-domain comparator". IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2008

[45] A. Hussain, S. Sin, C. Chan, S. Ben U, F. Maloberti and R. P. Martins, "Active-Passive $\Delta \Sigma$ Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364-374, Jan. 2017, doi: 10.1109/TVLSI.2016.2580712.

[46] A. Hussain, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "NTF zero compensation technique for passive sigma-delta modulator," in *Proc. IEEE PRIMEASIA*, Oct. 2011, pp. 82–85.

[47] JM de la Rosa. Sigma-Delta Converters: Practical Design GuidelM]. Hoboken, NJ, USA: Wiley-IEEE Press, 2018, 86-90.

[48] S. Pavan and P. Sankar, "Power reduction in continuous-time delta-sigma modulators using the assisted opamp technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1365–1379, Jul. 2010.

[49] Liu C C, Chang S J, Huang G Y, et al. A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 _m CMOS process. Symposium on VLSI Circuits Digest of Technical Papers, 2009: 236

[50] Lei, KM., Mak, PI. & Martins, R.P. Systematic analysis and cancellation of kickback noise in a dynamic latched comparator. *Analog Integr Circ Sig Process* **77,** 277–284 (2013).

[51] Song H, Leea M. Asymmetric monotonic switching scheme for energy-efficient SAR ADC. IEICE Electronics Express, 2014, 11(12): 1–5

[52] Shahmohammadia M, Ashtiani S J. Energy and area efficient tri-level switching procedure based on half of the reference voltage for SAR ADC. IEICE Electronics Express, 2012, 9(17): 1397–1401

[53] Zhang Y, Chen H, Guo G, et al. Energy-efficient hybrid split capacitor switching scheme for SAR ADCs. IEICE Electronics Express, 2016

[54] Zhu Y, Chan C H, Chio U F, et al. A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. IEEE J Solid-State Circuits, 2010, 45(6): 1111–1121

[55] Texas Instruments, "ADS8881x 18-Bit, 1-MSPS, Serial interface, microPower, Miniature, True-Differential Input SAR Analog-to-Digital Converter" ADS8881 Datasheet, May. 2013.

[56] Linear Technology, "18-Bit, 1Msps, Low power SAR ADC with 102 dB SNR," LT2378 Datasheet, July 2011.

[57] Texas Instruments, "Very Low Power, Negative Rail Input, Rail-to-Rail Output, fully-differential Amplifier," THS4521 Datasheet, Dec. 2008.

[58] Linear Technology, "Precision, Low Power, Rail-to-Rail Input/Output, Differential Op Amp/SAR ADC Driver," LT6362 Datasheet, May. 2012.

[59] Analog Devices, "Single Supply Differential ADC Driver," ADA4941 Datasheet, Apr. 2006.

[60] G. F. Luff, "A 3.3V-supply 120mW differential ADC driver amplifier in 0.18 μm SiGe BiCMOS," Proc. 2011 ISSCC, Feb. 2011, pp. 250-251.

[61] J.-S. Kim, D.-K. Jeong, and G. Kim, "A multi-level multi-phase charge recycling method for low-power AMLCD column drivers," IEEE J. Solid-State Circuits, vol. 35, no. 1, pp. 74–84, Jan. 2000.

[62] Y.-S. Son, J.-H. Kim, H.-H. Cho, J.-P. Hong, J.-H. Na, D.-S. Kim, D.-K. Han, J.-C. Hong, Y.-J. Jeon, and G.-H. Cho, "A column driver with low-power area-efficient push-pull buffer amplifiers for activematrix LCDs," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2007, pp. 142–143.

[63] P.-C. Yu and J.-C. Wu, "A class-b output buffer for flat-panel-display column driver," IEEE J. Solid-State Circuits, vol. 34, no. 1, pp. 116–119, Jan. 1999.

[64] T. Itakura and H. Minamizaki, "A two-gain-stage amplifier without an on-chip miller capacitor in an LCD driver IC," IEICE Trans. Fundamentals, vol. E85-A, no. 8, pp. 1913–1920, Aug. 2002.

[65] C.-W. Lu and C. L. Lee, "A low power high speed class-AB buffer amplifier for flat panel display application," IEEE Trans. VLSI Syst., vol. 10, no. 2, pp. 163–168, Apr. 2002.

[66] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," IEEE J. Solid-State Circuits, vol. 35, no. 2, pp. 221–230, Feb. 2000.

[67] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," IEEE J. Solid-State Circuits, vol. 38, no. 3, pp. 511–520, Mar. 2003.

[68] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[69] E. N. Y.Ho and P. K. T.Mok, "A capacitor-less CMOS active feedback low-dropout regulator with slew-rate enhancement for portable on-chip application," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 2, pp. 80–84, Feb. 2010.

[70] Y. P. Tsividis and R. W. Ulmer, "A CMOS voltage reference," IEEE J. Solid- State Circuits, vol. 13, no. 6, pp. 774–778, Dec. 1978.

[71] A.P. Brokaw, A simple three-terminal I.C. bandgap reference, IEEE J. Solid- State Circuits (1974).

166

[72] P. B. Basyurt and D. Y. Aksin, "Design of a curvature-corrected bandgap reference with 7.5ppm/C temperature coefficient in 0.35 μm CMOS process," in Proc. IEEE Int. Symp. Circuits Syst., Seoul, South Korea, May 2012, pp. 3142–3145.

[73] B. Ma and F. Yu, "A novel 1.2–V 4.5-ppm/°C curvature-compensated CMOS bandgap reference," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 4, pp. 1026–1035, Apr. 2014.

[74] Q.Duan and J. Roh, "A 1.2-V 4.2-ppm/°C high-order curvature compensated CMOS bandgap reference," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 3, pp. 662–670, Mar. 2015.

[75] J.-H. Li, X. Zhang, and M. Yu, "A 1.2-V piecewise curvature-corrected bandgap reference in 0.5 um CMOS process," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 6, pp. 1118–1122, Jun. 2011.

[76] P.Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature compensated BiCMOS bandgap with 1-V supply voltage," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1076–1081, Jul. 2001.

[77] Z.-K. Zhou et al., "A 1.6-V 25- A 5-ppm C curvature- compensated bandgap reference," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 59, no. 4, pp. 677– 684, Apr. 2012.

[78] B.-S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap voltage reference," IEEE J. Solid-State Circuits, vol. SC-18, no. 6, pp. 634–643, Dec. 1983.

[79] Tianlin Cao, et al. "A 0.9-V high-PSRR bandgap with self-cascode current mirror," 2012 IEEE International Conference on Circuits and Systems (ICCAS), 2012, pp. 267- 271.

[80] G. A. Rincon-Mora and P. E. Allen, "A 1.1-V current-mode and piecewise linear curvature-corrected bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1551–1554, Oct. 1998.

[81] Yi Huang, *et al.*: "BiCMOS-Based Compensation: Toward Fully Curvature-Corrected Bandgap Reference Circuits," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 65 (2018) 1210

[82] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap voltage reference," *IEEE J. Solid- State Circuits*, vol. 28, no. 6, pp. 667–670, Jun. 1993.

[83] S. R. Lewis and A. P. Brokaw, "Curvature correction of bipolar bandgap voltage reference," US 480 890 8, Feb. 28, 1989.

[84] L. Liu, X. Liao and J. Mu, " A 3.6 μVrms noise, 3 ppm/∘C TC bandgap reference with offset/noise suppression and five-piece linear compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 10, pp. 3786-3796, Oct. 2019, doi: 10.1109/TCSI.2019.2922652.

[85] R. Wang *et al.*, "A sub-1ppm/_C current-mode CMOS bandgap reference with piecewise curvature compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 3, pp. 904–913, Mar. 2017.

[86] H. -M. Chen, C. -C. Lee, S. -H. Jheng, W. -C. Chen and B. -Y. Lee, "A Sub-1 ppm/°C Precision Bandgap Reference With Adjusted-Temperature-Curvature Compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 6, pp. 1308-1317, June 2017,

[87] K. Chen, L. Petruzzi, R. Hulfachor and M. Onabajo, "A 1.16-V 5.8-to-13.5-ppm/°C Curvature-Compensated CMOS Bandgap Reference Circuit With a Shared Offset-Cancellation Method for Internal Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 56, no. 1, pp. 267-276, Jan. 2021,

[88] J. Jiang, W. Shu, and J. S. Chang, "A 5.6 ppm/_C temperature coefficient, 87-dB PSRR, sub-1-V voltage reference in 65-nm CMOS exploiting the zero-temperature-coefficient point," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 623–633, Mar. 2017.

[89] U. Kamath et al., "A 1 V Bandgap Reference in 7-nm FinFET with a Programmable Temperature Coefficient and an Inaccuracy of ±0.2% from −45°C to 125°C," ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC), 2018, pp. 78-81, doi: 10.1109/ESSCIRC.2018.8494284.

[90] S. Mechrmanesh, M. B. Vahidfar, and H. A. Aslanzadeh, M. Atarodi. "A 1-volt, high PSRR, CMOS bandgap voltage reference," *IEEE International symposium on circuits and systems*. vol. 1, pp. I-381-I-384, Bangkok, May 2003.

[91] Shi, Y., Li, S., Cao, J. *et al.* A 180 nm Self-biased Bandgap Reference with High PSRR Enhancement. *Nanoscale Res Lett* **15,** 104 (2020).

[92] H.Y. Zhang, P.K. Chan, and M.T. Tan, "A high PSR voltage reference for dc-to-dc converter applications," *International symposium on circuits and systems*. vol. 1, pp. 816-819, Taipei, May 2009.

[93] A. Dey, and T.K. Bhattacharyya, "A CMOS bandgap reference with high PSRR and improved temperature stability for system-on-chip applications," *International conference of electron devices and solid-state circuits*. pp. 1-2, Tianjin, November 2011.

[94] T.L. Cao, Y. Han, X.P. Liu, H. Luo, and H. Zhang, "A 0.9-V high-PSRR bandgap with self-cascode current mirror," *International conference on circuits and systems*. vol.1, pp. 267-271, Kuala Lumpur, October 2012.

[95] Z. K. Zhou, Y. Shi, Z. Huang, P. S. Zhu, Y. Q. Ma, Y. C. Wang, Z. Chen, X. Ming, and B. Zhang, "A 1.6-V 25-mA 5-ppm/°C curvature-compensated bandgap reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*. vol. 59, pp. 677-684, April 2012.

[96] R. Burt and J. Zhang, "A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path," *IEEE J. Solid-State Circuits,* vol.41, no.12, pp.2729-2736, Dec. 2006.

[97] Y. P. Tsividis, "Accurate analysis of temperature effects in I/SUB c/V/SUB BE/ characteristics with application to bandgap reference sources," in IEEE Journal of Solid-State Circuits, vol. 15, no. 6, pp. 1076-1084, Dec. 1980, doi: 10.1109/JSSC.1980.1051519.

[98] A. D. Grasso, G. Palumbo and S. Pennisi, "Advances in Reversed Nested Miller Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 54, no. 7, pp. 1459-1470, July 2007.

[99] Ka Chun Kwok and P. K. T. Mok, "Pole-zero tracking frequency compensation for low dropout regulator," *2002 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2002, pp. IV-IV, doi: 10.1109/ISCAS.2002.1010562.

[100] A. Garimella, M. W. Rashid and P. M. Furth, "Reverse Nested Miller Compensation Using Current Buffers in a Three-Stage LDO," *IEEE Trans on Circuits and Systems II: Express Briefs*, vol. 57, no. 4, pp. 250-254, April 2010.

[101] C. Zhan and W. Ki, "An Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator With Subthreshold Undershoot-Reduction for SoC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 5, pp. 1119-1131, May 2012, doi: 10.1109/TCSI.2012.2190675.

[102] Hsuan-I Pan, Chin-Hung Cheng, Chern-Lin Chen and Ta-yung Yang, "A CMOS low dropout regulator stable with any load capacitor," *2004 IEEE Region 10 Conference TENCON 2004*., 2004, pp. 266-269 Vol. 4, doi: 10.1109/TENCON.2004.1414920.

[103] M. Ho and K. N. Leung, "Dynamic Bias-Current Boosting Technique for Ultralow-Power Low-Dropout Regulator in Biomedical Applications," *IEEE Transactions on Circuits and Systems II: Express Brief*s, vol. 58, no. 3, pp. 174-178, March 2011, doi: 10.1109/TCSII.2011.2110330.

[104] Y. Lu et al., "A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS," *IET Electron. Lett.*, vol. 52, no. 16, pp. 1368–1370, Aug. 2016.

[105] A. Garimella, M. W. Rashid and P. M. Furth, "Reverse Nested Miller Compensation Using Current Buffers in a Three-Stage LDO," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 4, pp. 250-254, April 2010, doi: 10.1109/TCSII.2010.2043401.

[106] J. Zarate-Roldan, M. Wang, J. Torres, and E. Sánchez-Sinencio, "A capacitor-less LDO with high-frequency PSR suitable for a wide range of on-chip capacitive loads," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 9, pp. 2970–2982, Sep. 2016.

[107] Y. Huang, Y. Lu, F. Maloberti, and R. P. Martins, "Nano-Ampere Low- Dropout Regulator Designs for IoT Devices," *IEEE Trans. on Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 4017–4026, Nov. 2018.

[108] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low dropout regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[109] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.

[110] Y. Lam and W. Ki, "A 0.9V 0.35 μm Adaptively Biased CMOS LDO Regulator with Fast Transient Response," *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008, pp. 442-626, doi: 10.1109/ISSCC.2008.4523247.

[111] M. Ho, K. N. Leung, and K.-L. Mak, "A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2466–2475, Nov. 2010.

[112] X. Ming et al., "A Fast-Transient Capacitorless LDO With Dual Paths Active-Frequency Compensation Scheme," in IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 10332-10347, Sept. 2022, doi: 10.1109/TPEL.2022.3165116.

[113] J. Guo and K. N. Leung, "A 6uW- chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, Sep. 2010.

[114] Y. Lu, M. Huang and R. P. Martins, "PID Control Considerations for Analog-Digital Hybrid Low-Dropout Regulators (Invited Paper)," *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019, pp. 1-3, doi: 10.1109/EDSSC.2019.8754302.

[115] Sung, Eun-Taek, Sangyong Park, and Donghyun Baek. 2018. "A Fast-Transient Output Capacitor-Less Low-Dropout Regulator Using Active-Feedback and Current-Reuse Feedforward Compensation" *Energies* 11, no. 3: 688.

[116] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. of Solid-State Circuits*, vol. 40, no. 4, pp. 933-940, April 2005, doi: 10.1109/JSSC.2004.842831.

[117] Guo, J., Ho, M., Kwong, K.Y., and Leung, K.N.: 'Power-area-efficient transient-improved capacitor-free FVF-LDO with digital detecting technique', *Electron. Lett.*, vol. 51, no. 1, pp. 94–96, Jan. 2015, Jan, 2015.

[118] Assaad, Rim & Silva-Martínez, José. "Enhancing general performance of folded cascode amplifier by recycling current." *Electronics Letters*. vol.43, no. 23, Nov.2007. doi:10.1049/el:20072031.

[119] Seyed Arash Katourani, Omid Hashemipour, Masoud Meghdadi, An ultra high slew rate recycling folded cascode OTA with 100-dB DC gain, *AEU - International Journal of Electronics and Communications*, vol. 147, 2022, 154140, ISSN 1434-8411, https://doi.org/10.1016/j.aeue.2022.154140.

[120] X. L. Tan *et al.*, "A FVF LDO regulator with dual-summed miller frequency compensation for wide load capacitance range applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1304–1312, May 2014.

[121] Y.-J. Lee *et al.*, "A 200-mA digital low dropout regulator with coarse fine dual loop in mobile application processor," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan. 2017.

[122] L. G. Salem, J. Warchall, and P. P. Mercier, "A successive approximation recursive digital low-dropout voltage regulator with PD compensation and sub-LSB duty control," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 35–49, Jan. 2018.

[123] S. Kundu, M. Liu, R. Wong, S.-J. Wen, and C. H. Kim, "A fully integrated 40pF output capacitor beat-frequency-quantizer-based digital LDO with built-in adaptive sampling and active voltage positioning," *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2018, pp. 308–309.

[124] M. Huang, Y. Lu, U. Seng-Pan, and R. P. Martins, "An analog-assisted tri-loop digital low-dropout regulator," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 20–34, Jan. 2018.

[125] X. Ma *et al.*, "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS," *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2018, pp. 306–307.

[126] X. Liu *et al.*, "14.7 a modular hybrid LDO with fast load transient response and programmable PSRR in 14 nm CMOS featuring dynamic clamp tuning and time-constant compensation," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 234–236.

[127] J. F. Bulzacchelli *et al.*, "Dual-loop system of distributed micro-regulators with high DC accuracy, load response time below 500 ps, 85-mV dropout voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, Apr. 2012.

[128] Q. Duan, W. Li, S. Huang, Y. Ding, Z. Meng, K. Shi, "A Two-Module Linear Regulator with 3.9-10 V Input, 2.5 V Output, and 500 mA Load." *Electronics* 2019, 8, 1143.

[129] Principles of coherent communication, A. J. Viterbi, McGraw-Hill, 1966 - 321 pages.

[130] M.L.Meade, Lock-in amplifiers: Principles and Applications, Peter Peregrinus Ltd., London, UK, 1983. 2nd edit. 1989, 246 p., ISBN 0906048 94 X

[131] R. Burdett, "Amplitude Modulated Signals - The Lock-in Amplifier". Handbook of Measuring System Design (Wiley). ISBN 978-0-470-02143-9, 2005.

[132] Lock-in amplifiers and pre-amplifiers PAR124A, Princeton Applied Research/EG&G, now: AMETEK Advanced Measurement Technology, 801 South Illinois Avenue, Oak Ridge, Tennessee 37831-0895, United States, http://www.ametek.com/

[133] Application Note #3, About Lock-In Amplifiers, Stanford Research Systems, Inc., 1290-D Reamwood Avenue, Sunnyvale, CA 94089, http://www.thinksrs.com.

[134] Blair, D.P.: 'Phase sensitive detection as a means to recover signals buried in noise', J. Phys. E, Sci. Instrum., 1975.

[135] J. Dratler, Inexpensive linear displacement transducer using a low power lock-in amplifier, Rev. Sci. Instrum. 48, 327 (1977).P.A. Probst, B. Collet, Low-frequency digital lock-in amplifier, Review of Scientific Instruments (AIP) 56 (3): 466, March 1985.

[136] K. Ramani and S. Ganapathy , Simple lock-in amplifier using a four-quadrant analog multiplier and a phase lock loop, Rev. Sci. Instrum. 52, 1364 (1981).

[137] P. K. Dixon., L. Wu, Broadband digital lock-in amplifier techniques Review of Scientific Instruments (AIP) 60 (10): 3329, October 1989.

[138] L. G. Rubin, The new(?) wave: Digital lock-in amplifiers, Rev. Sci. Instrum. 59, 514 (1988) 2 pages.

[139] Carrato, S. , Paolucci, G., Tommasini, R. , Rosei, R., Versatile low-cost digital lock-in amplifier suitable for multichannel phase-sensitive detection, Review of Scientific Instruments, Vol. 60, Issue 7, 1989, Pages 2257-2259.

[140] SR124 Analog lock-in amplifier, Stanford Research Systems, Inc., 1290-D Reamwood Avenue, Sunnyvale, CA 94089, http://www.thinksrs.com/products/SR124.htm

[141] M. Gabal, N. Medrano, B. Calvo, P. Martinez, S. Celma, M. Valero, "A Complete Low Voltage Analog Lock-in Amplifier to Recover Sensor Signals Buried in Noise for Embedded Applications", Proc. Eurosensors XXIV, pp. 74-77, Linz, September 2010.

[142] Aguirre, J. ; Medrano, N. ; Calvo, B. ; Celma, S. , Lock-in amplifier for portable sensing systems , Electronics Letters , October 13 2011, Volume : 47 , Issue:21 pp. 1172 – 1173.

[143] Rafati, M., Qasemi, S.R. & Alvandpour, A. A configurable fluorescence sensing front-end for ultra-low power and high sensitivity applications. *Analog Integr Circ Sig Process* **110**, 3–17 (2022). https://doi.org/10.1007/s10470-021-01953-5

[144] T. Costa, F. A. Cardoso, J. Germano, P. P. Freitas and M. S. Piedade, "A CMOS Front-End With Integrated Magnetoresistive Sensors for Biomolecular Recognition Detection Applications," in IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 5, pp. 988-1000, Oct. 2017, doi: 10.1109/TBCAS.2017.2743685.

[145] M. N. Khiarak et al., "A high-precision CMOS biophotometry sensor with noise cancellation and two-step A/D conversion," 2017 15th IEEE International New Circuits and Systems Conference (NEWCAS), 2017, pp. 293-296, doi: 10.1109/NEWCAS.2017.8010163.

[146] De Marcellis, G. Ferri, A. D'Amico, C. Di Natale and E. Martinelli, "A Fully-Analog Lock-In Amplifier With Automatic Phase Alignment for Accurate Measurements of ppb Gas Concentrations," in IEEE Sensors Journal, vol. 12, no. 5, pp. 1377-1383, May 2012, doi: 10.1109/JSEN.2011.2172602.

[147] C. Sawigun and W. A. Serdijn, "A modular transconductance reduction technique for very low-frequency Gm-C filters," in Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2012, pp. 1183-1186.

[148] Yu, S.; Park, Y. SLUA-WSN: Secure and Lightweight Three-Factor-Based User Authentication Protocol for Wireless Sensor Networks. *Sensors* 2020, *20*, 4143. https://doi.org/10.3390/s20154143

[149] Gupta, R. (2017). Biomedical Sensors and Their Interfacing. In: George, B., Roy, J., Kumar, V., Mukhopadhyay, S. (eds) Advanced Interfacing Techniques for Sensors . Smart Sensors, Measurement and Instrumentation, vol 25. Springer, Cham. https://doi.org/10.1007/978-3-319-55369-6_7