Ultra Low-voltage Multiple-loop Feedback Switched-capacitor Filters

By

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Dedicated to my Parents, my cousin Nithinsimha, my Friends and Teachers

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ABSTRACT

This work presents an SC filter design technique based on a CMOS inverter. The proposed technique is demonstrated by the design of the sixth-order Follow the Leader Feedback (FLF) Chebyshev low-pass filter. This technique resulted in filters with reduced sensitivities compared to the cascade realization. This design was simulated using the TSMC65nm technology at a low supply voltage of 0.7V. The characteristics of the designed filter are 1dB pass band ripple with a 3dB bandwidth of 0.8MHz and an attenuation of 40dB with an ultra low power consumption of only 1.8μW which is far less compared to the existing op-amp based filter designs. Also, the Dynamic Threshold MOS (DTMOS) integrator for ultra-low supply voltage (sub-threshold operation) is proposed and a low frequency SC filter is realized for biomedical application where ultra low-voltage operation and ultra low power consumption is an important factor.

LIST OF ABBREVIATIONS USED

IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
NMOS	N-type Metal-Oxide-Semiconductor
OP-AMP	Operational Amplifier
DT	Dynamic Threshold
SC	Switched-Capacitor
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
DR	Dynamic Range
CBSC	Comparator Based Switched-Capacitor
PSRR	Power Supply Rejection Ratio
FLF	Follow-the-Leader Feedback
LTI	Linear Time Invariant
VTC	Voltage Transfer Characteristics
GB	Gain Bandwidth
UGB	Unity Gain Bandwidth
PSS	Periodic Steady-State

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CHAPTER 1 Introduction

1.1 Motivation

The monolithic integrated circuits (ICs) were invented in the late 1950s. At that specific time, it was expensive to manufacture and was only used to make ICs for certain military applications. However, after a few years with increasing manufacturing yield and shrinking transistor sizes, the ICs manufacturing cost went down [1]. In the most recent times, we find inbuilt IC's, which are integrated into our day-to-day electronic gadgets. On the other hand, resistors in ICs were problematic due to their physical size and accuracy of the component value during the manufacturing process, which would degrade the performance of the circuit. Later, switched-capacitor (SC) circuits addressed these problems by simulating a resistor with two MOS switches and a capacitor. SC circuits became popular due to their ability to save the chip area. Furthermore, the characteristics of the SC circuit are less sensitive to component variation as it is determined by the ratios of capacitor values(which can be precisely determined by laser),use less power than similar continuous-time circuit, and better on-chip implementation [2] [3].

SC integrators are the basic building block of a SC circuit. Most of the analog signal processing and mixed-signal processing involve SC circuits and are the most widely used. Its uses include data converters (ADCs and DACs [4] [5]), analog filters [7] [12], Delta-sigma modulators [8], sensor interfaces [9], etc.

Operational amplifier (Op-amp) is a common analog building block used along with switches and capacitors to construct SC circuit. Ever since the ICs came into existence, the parameters such as the supply voltage, threshold voltage, oxide thickness have been scaled down with technology. Supply voltage scaling affects the dynamic range of the op-amp and further scaling will result in reduced voltage headroom. The rate at which supply voltage is being scaled is much higher than the rate at which the threshold voltage is scaled. This prevents

sufficient voltage from driving all the transistors into the saturation region. The performance of the op-amp is usually limited due to various factors such as bandwidth, gain, power consumption, output voltage swing, slew rate, noise etc [10].

Gain and bandwidth of an op-amp can be tuned at the cost of power consumption. It is well known that total power is calculated by multiplying the supply voltage and total current. From this, it follows that operating the op-amp at low supply voltage and high current-efficiency can lower the power consumption. Technology scaling can lead to lower supply voltages. However, the threshold voltage is not scaled according to the transistor dimensions. This puts a limit on the supply voltage. From some of the points discussed above, we can conclude that designing an op-amp at low supply voltage has become very challenging with technology scaling. Low voltage op-amps [11][13][14]have been explored, but they have reached their limit on supply voltage, which is further restricted by the common mode voltage.

Low voltage applications are some of the fastest growing segments of the market due to the demand for battery operated mobile electronic devices (biomedical application) and the need to interface with low voltage electronics.

Some of the low voltage, low power SC filter design techniques are: switched op-amp [16] [17], multistage amplifier [18] SC circuits, digitally assisted [19] [20] SC circuits, comparator-based [21] SC circuits, unity-gain buffer based [22] [23] SC circuit. In switched op-amp technique, switches which require more power than an op-amp are replaced with an op-amp that increases the overhead of the op-amp by 1.5 times and decreases the power consumption to 0.75 of its original value. This is because the replaced op-amp's are switched off for 50% of the time. Multistage amplifiers use a compensation scheme to stabilize the closed loop gain, wherein the compensation capacitor consumes more power to maintain the speed of the amplifier. Digitally assisted op-amp consumes additional power for digital calibration circuits. Comparator-based switched-capacitor circuits suffer from overshoot voltage at the output due to finite comparator delay and voltage error caused by non zero switch resistance.

1.2 Conventional SC amplifiers used in SC filter design

1.2.1 Op-amp based SC amplifier

The basic operation of a SC circuit is analysed by the amount of charge transferred from the input to the output. During ϕ_1, C_1 is charged from the input and during ϕ_2, the charge from C_1 is transferred to C_2. This charge transfer takes place in the presence of virtual ground and the accuracy of charge transfer is also determined by the virtual ground voltage.

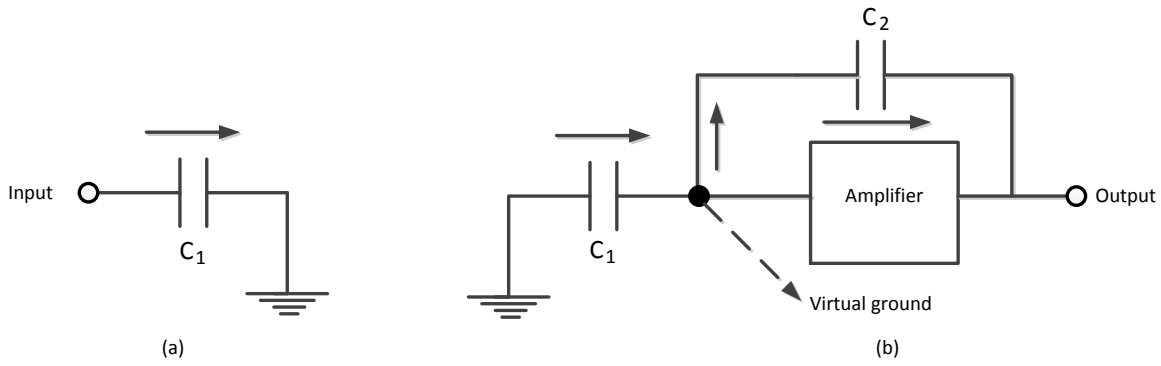

Figure 1. Charge transfer operation (a) Sampling (b) Charge transfer

In an op-amp, the virtual ground is created by connecting the positive terminal to signal ground and forcing the negative terminal to act as virtual ground during charge transfer phase.

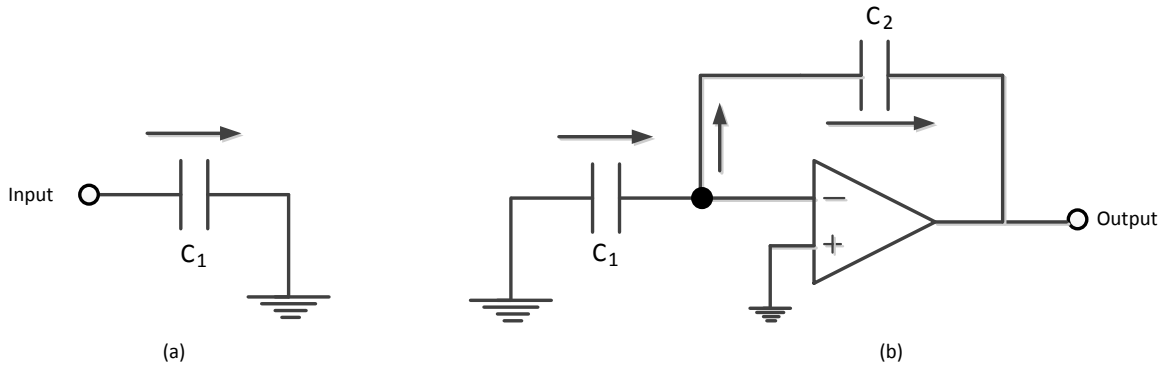

Figure 2. (a) Sampling phase (b) Charge transfer phase.

It is really hard to obtain full output swing for an op-amp operating at low-supply voltage. When the power supplies were ±15V, the output voltage swing of an op-amp did not seem important because with a 30V power supply the designer could sacrifice 3V from each end to provide enough voltage to operate the transistors in the saturation region. With single power supply and technology scaling the supply voltage is being scaled at a faster rate compared to the threshold voltages of the transistors and continuing in scaling process will result in insufficient voltage to operate the transistors in the saturation region.

Say, an op-amp operating with a power supply voltage of 1.8V would only have an output swing of 1.63V [24]. The Dynamic Range of an op-amp is given by

$$Dynamic\ Range\ (DR) = 20Log_{10}\left(\frac{V_{OUT\ (max\ )}}{V_{OUT\ (min\ )}}\right)\text{in dB}$$

Lower supply voltage affects the dynamic range and to maintain the dynamic range, circuit capacitance has to be increased. A corresponding increase in power consumption is needed to maintain the speed of operation. Additionally, the low output resistance in scaled CMOS technology results in lower op-amp gain. The traditional solution to the gain problem is to cascade the amplifier stages, but this approach does not solve the low swing problem. The alternative to cascading is to cascade several low gain stages, but stability becomes an issue and additional stabilizing techniques consume more power in order to maintain the same speed of operation. Most recently, digital calibration has been used to

address the above mentioned problems; however, additional power is consumed for calibration circuits.

1.2.2 Comparator-Based SC amplifier

An alternative approach was proposed in [57], where an op-amp in a SC circuit was replaced by 'a comparator and a current source' which eliminates the need for an op-amp. The operation of op-amp based and comparator-based SC is similar except that the op-amp forces the virtual ground condition and the comparator detects the virtual ground condition with the help of a current source and triggers the charge transfer.

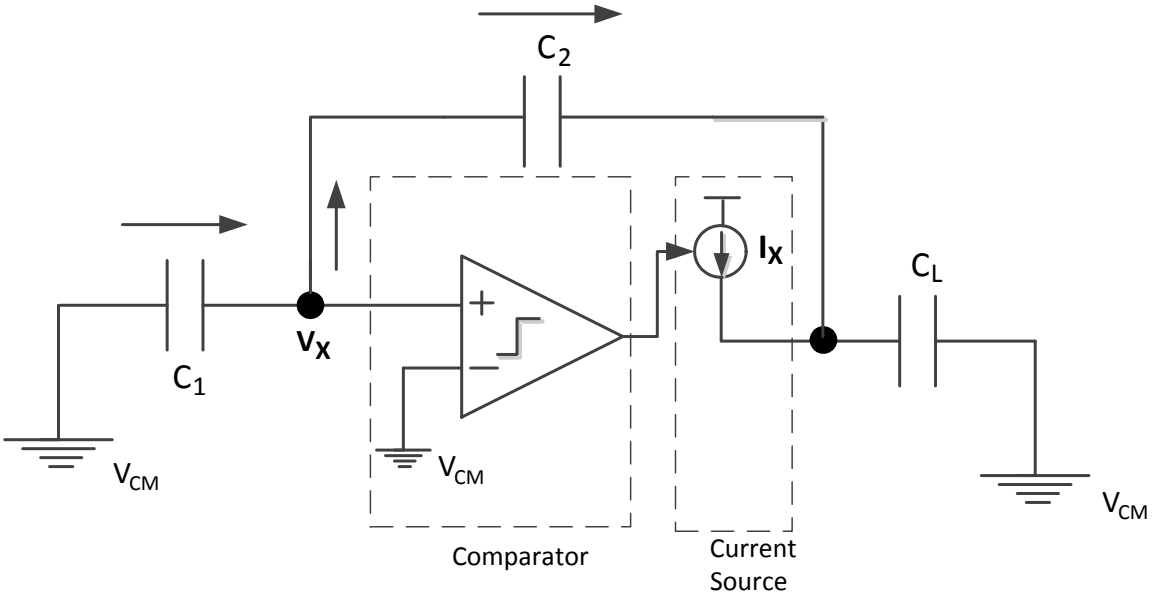

Figure 3.Comparator-based SC circuit

The sampling phase of comparator based SC is similar to op-amp based SC. During the charge transfer phase, for a short period of time, the output is grounded and the current source is turned on, charges up the capacitor network consisting of C_1, C_2 and C_L. The voltage at the output and V_X is ramped up until the comparator detects the virtual ground voltage condition, which is $V_X = V_{CM}$ for the Figure3, and turn off the current source. The

sampling instant is determined by the comparator and the charge is transferred from C_1 to C_2 and the same output voltage is sampled on C_L.

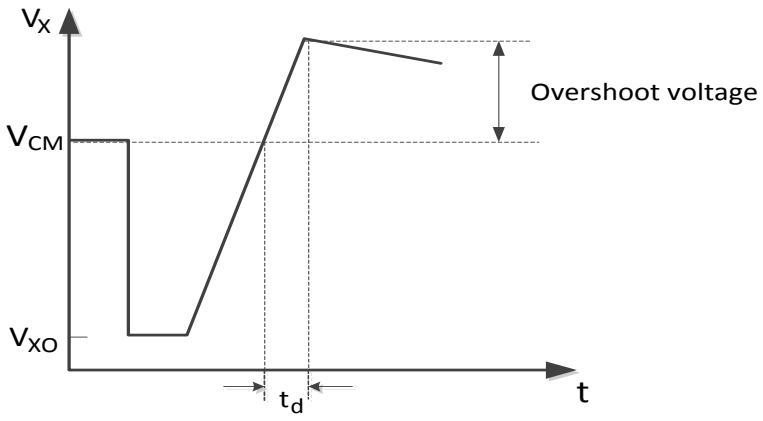

Figure 4. Overshoot voltage error at a comparator output

The comparator-based SC technique suffers from overshoot voltage error at the comparator output as shown in Figure 4 and special techniques has to be adopted to cancel this error but even then the over shoot error can only be reduced to certain level and it cannot be eliminated completely and also has problems with low-supply voltage causing low voltage headroom.

1.3 Thesis objective

Based on the above discussion, the main objective of this thesis is to develop techniques for designing SC filters to be able to

1. Operate at ultra low supply voltage
2. Consume ultra low power
3. Provide high slew rate
4. Provide faster settling time
5. Less sensitive to component variation

1.4 Thesis contribution

1.4.1 Low-supply voltage

The existing SC filter designs using op-amps and comparators require supply voltage of 1V or higher to turn *on* the transistors, low supply voltage results in low voltage headroom. CMOS inverter-based SC design is capable of operating at supply voltage as low as 0.7V, because it has fewer transistors in the amplifier section. Advancement in CMOS technology demands a design to operate at even lower supply voltages. In this thesis, DTMOS inverter-based SC filter has been proposed, which operates at a supply voltage of 0.4V.

1.4.2 Low-power consumption

The low supply voltage requirement is the key to design circuits to consume less power. Because, reducing the supply voltage will minimize the static power consumption of the device. The proposed DTMOS integrator operates with ultra low voltage and the power consumption is very less compared to the existing designs.

1.4.3 High Slew rate and faster Settling time

The speed of a circuit is determined by how fast a circuit responds at the output after the input is changed from one state to another. High slew rate and faster settling time results in higher speed of operation. The proposed design has a high slew rate and a faster settling time which is achieved by lowering the threshold voltage during the *on* state of the transistor to provide high current drive by replacing conventional MOS transistors with DTMOS transistors.

In this thesis, a CMOS inverter-based SC integrator using TSMC65nm technology is designed. A CMOS inverter-based sixth-order Chebyshev low-pass filter implemented

using Follow-the-Leader Feedback (FLF) architecture is proposed and it proves to be less sensitive to component variation compared to the cascade design. Comparing the proposed work to op-amp based design and comparator-based design, the proposed design operates with a low supply voltage with an ultra low power consumption of only 1.8μW. A SC integrator design based on an inverter using dynamic threshold MOS transistor is proposed for ultra low supply voltages and a fourth-order Chebyshev filter has been realized using the proposed DTMOS integrator for low frequency biomedical application.

1.5 Thesis organization

The organization of the remaining parts of this thesis is as follows:

Chapter2 briefly describes SC circuits and its z-domain transfer function along with the operation of op-amp-based SC integrator, the concept of state-variable approach and how it is adopted for SC application using FLF approach.

Chapter3 provides detailed operation of a CMOS inverter-based integrator and the simulation results obtained with Cadence in the TSMC65nm technology for CMOS inverter-based SC integrator and its performance parameter.

Chapter*4* presents a SC biquad design based on CMOS inverter-based integrator technique, sixth-order Chebyshev filter based on cascade design and implementation of Follow-the-Leader Feedback technique.

Chapter5 presents the results obtained for different techniques implemented in chapter 4.

Chapter6 discusses about ultra-low supply voltage design solutions and a DTMOS integrator based on inverter design is proposed for ultra low supply voltage. A fourth-order Chebyshev filter is designed for low frequency biomedical application.

Chapter7 provides conclusions about the DTMOS inverter-based SC design using FLF technique designed in this thesis and compared with other existing SC filters. Few suggestions for future work is discussed.

CHAPTER 2 Switched-capacitor and state-variable approach

2.1 General Switched-capacitor network

In general, a switched-capacitor integrator consists of switching elements (capacitor and MOS transistor as switches [34]) and an op-amp, as shown in Figure 5, and operates with two non-overlapping clock phase $\phi_1$and ϕ_2, as shown in Figure 6. The switching elements are controlled through clock signals which determine whether a switch should be closed to charge or discharge the capacitor it is connected to. Usually, the charge is transferred from the input capacitor to the feedback capacitor connected to the output. Thus, the output of the integrator is determined by the switching elements in the input node and the feedback elements. Depending on the switching elements various z-domain transfer functions can be derived [35].

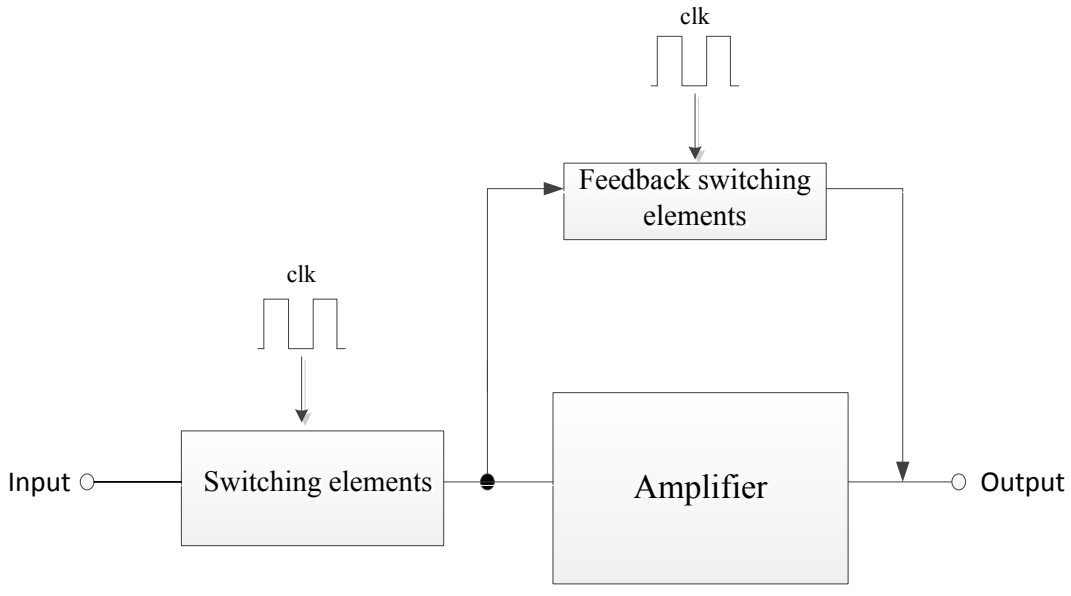

Figure 5. A general switched-capacitor network

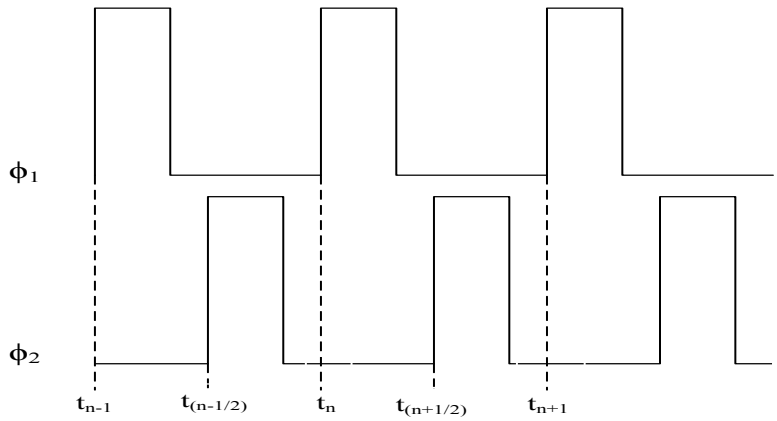

Figure 6. Two phase non-overlapping clocks

2.2 Conventional op-amp based SC integrator

2.2.1 Non-inverting Switched-capacitor integrator

A switched capacitor integrator design based on an op-amp operates with two phase clocks, ϕ1 and ϕ2. The circuit in Figure 7 samples the input into the capacitor C_1 during ϕ1 and transfers the total charge from C_1 to feedback capacitor C_2 during ϕ2 for an ideal op-amp with zero input offset. This charge transfer takes place in the presence of virtual ground in an op-amp which is created by connecting the positive terminal of the op-amp to the ground [37].

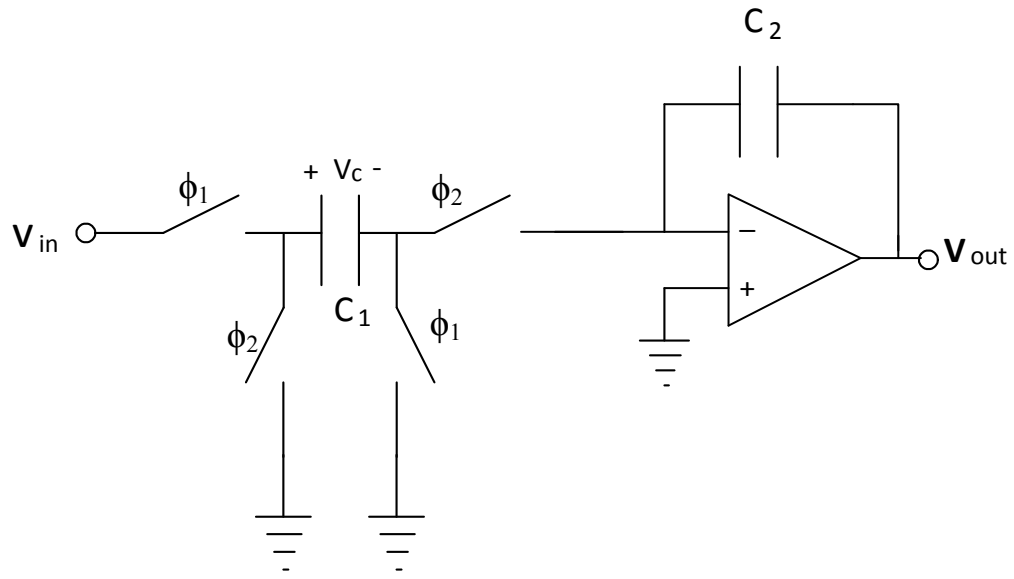

Figure 7. Non-inverting Switched-capacitor integrator

The charge transfer equation for the above integrator can be deduced as follows [36],

During $\phi_{1,}$ (n)

$$C_2 V_{out}(n) = C_2 V_{out}\left(n - \frac{1}{2}\right) - 0 \quad (1)$$

During $\phi_{2,}$ $\left(n - \frac{1}{2}\right)$

$$C_2 V_{out}\left(n - \frac{1}{2}\right) = C_2 V_{out}(n-1) - C_1[0 - V_{in}(n-1)] \quad (2)$$

Combining the above equations (1) and (2) we obtain,

$$C_2 V_{out}(n) = C_2 V_{out}(n-1) + C_1 V_{in}(n-1) \quad (3)$$

Obtaining z-transform for the above equation (3) result in a transfer function,

$$\frac{V_{out}(Z)}{V_{in}(Z)} = \frac{C_1}{C_2} \cdot \frac{Z^{-1}}{1 - Z^{-1}} \quad (4)$$

The above obtained transfer function is for the output evaluated during $\phi_{1,}$ If the output is evaluated during $\phi_{2,}$ then the numerator would have a half a cycle delay $Z^{-\frac{1}{2}}$.

2.2.2 Inverting Switched-capacitor integrator

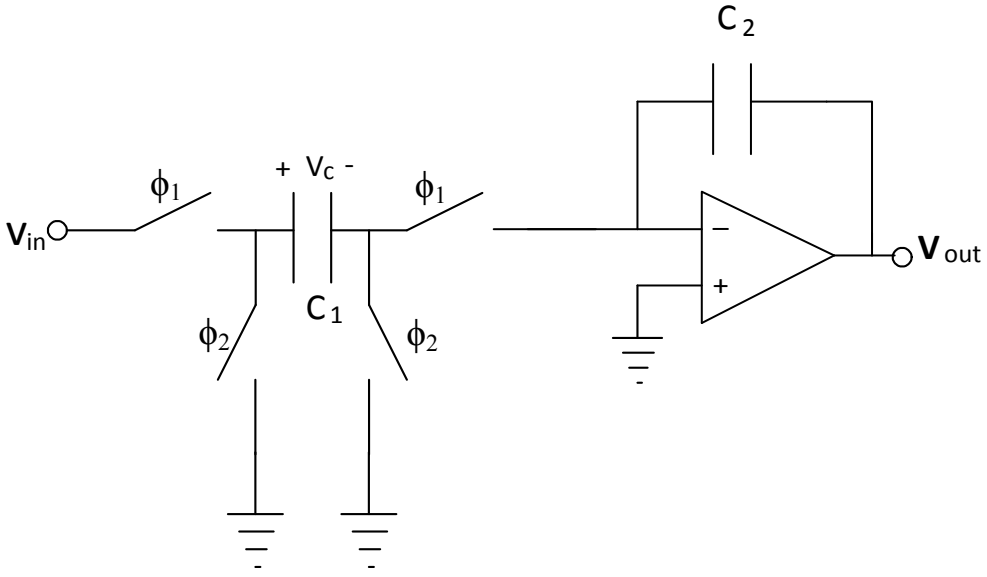

Figure 8. Inverting Switched-capacitor integrator

The charge transfer equation for the above integrator can be derived as follows [36],

During $\phi_{1,}$ (n)

$$C_2V_{out}(n) = C_2V_{out}\left(n-\frac{1}{2}\right) + C_1[-V_{in}(n)+0] \quad (5)$$

During $\phi_{2,}\left(n-\frac{1}{2}\right)$

$$C_2V_{out}\left(n-\frac{1}{2}\right) = C_2V_{out}(n-1)+0 \quad (6)$$

Combining the above equations (5) and (6),

$$C_2V_{out}(n) = C_2V_{out}(n-1) - C_1V_{in}(n) \quad (7)$$

Obtaining z-transform for the above equation (7) results in a transfer function

$$\frac{V_{out}(Z)}{V_{in}(Z)} = -\frac{C_1}{C_2}.\frac{1}{1-Z^{-1}} \quad (8)$$

The above obtained transfer function is for the output evaluated during ϕ_1. If the output is evaluated during ϕ_2, then the numerator would have a half a cycle delay $Z^{-\frac{1}{2}}$.

From the above equations (1) – (8), output evaluated during clock phase $\phi_1$and $\phi_2$with the input being available during $\phi_1$is shown in Table 1.

	Output evaluated during ϕ_1	Output evaluated during ϕ_2
INVERTING SC INTEGRATOR	$\frac{V_{out}(Z)}{V_{in}(Z)} = -\frac{C_1}{C_2}.\frac{1}{1-Z^{-1}}$	$\frac{V_{out}(Z)}{V_{in}(Z)} = -\frac{C_1}{C_2}.\frac{Z^{-\frac{1}{2}}}{1-Z^{-1}}$
NON-INVERTING SC INTEGRATOR	$\frac{V_{out}(Z)}{V_{in}(Z)} = \frac{C_1}{C_2}.\frac{Z^{-1}}{1-Z^{-1}}$	$\frac{V_{out}(Z)}{V_{in}(Z)} = \frac{C_1}{C_2}.\frac{Z^{-\frac{1}{2}}}{1-Z^{-1}}$

Table 1.The output transfer function of inverting and non-inverting SC integrators

2.3 State-variables approach

2.3.1 Definition of state-variables

The state of a system at time t_o is defined as the minimal information that is sufficient to determine the state and the output of the system for all times $t \geq t_o$ when the input to the system is also known for all times $t \geq t_o$. The variables that contain this information are called the state variables [40].

2.3.2 Selection of state-variables

The state variables of the system can also be interpreted as the "memory elements" of the system, since we are dealing with discrete time systems which are usually formed by amplifiers and delay elements. The outputs of the delay elements are chosen as state variables.

2.3.3 Canonical simulation of the first form

Consider a discrete-time 2nd-order LTI system with transfer function [40],

$$H(z) = \frac{Y(Z)}{X(Z)} = \frac{b_o + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}} \quad (9)$$

we have, $(1 + a_1 Z^{-1} + a_2 Z^{-2})Y(Z) = (b_o + b_1 Z^{-1} + b_2 Z^{-2})X(Z)$

The above equation can be rearranged as,

$$Y(Z) = -a_1 Z^{-1} Y(z) - a_2 Z^{-2} Y(z) + b_o X(z) + b_1 Z^{-1} X(z) + b_2 Z^{-2} X(Z) \quad (10)$$

A block diagram representation of the above equation, utilizing unit-delay elements, is as shown below.

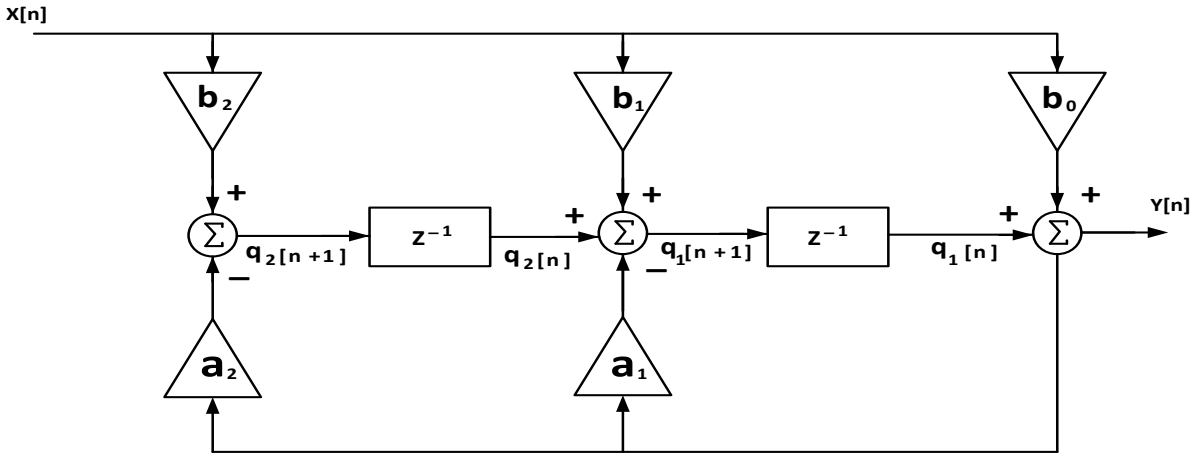

Figure 9. Canonical simulation of the first form

The outputs of the delay elements are chosen as the state-variables. From Figure 9, one obtains:

$$y[n] = q_1[n] + b_o x[n]$$

$$q_1[n+1] = -a_1 y[n] + q_2[n] + b_1 x[n]$$

$$= -a_1 q_1[n] + q_2[n] + (b_1 - a_1 b_0) x[n]$$

$$q_2[n+1] = -a_2 y[n] + b_2 x[n]$$

$$= -a_2 q_1[n] + (b_2 - a_2 b_0) x[n]$$

In matrix form, it can written as

$$q[n+1] = \begin{bmatrix} -a_1 & 1 \\ -a_2 & 0 \end{bmatrix} q[n] + \begin{bmatrix} b_1 & -a_1 b_o \\ b_2 & -a_2 b_o \end{bmatrix} x[n]$$

$$y[n] = [1 \quad 0] q[n] + b_o x[n]$$

2.4 Follow-the-Leader Feedback (FLF) technique

2.4.1 Why choose the FLF topology

Higher order filters are implemented using different approaches [41][42]. The most popular and simplest way to implement the higher-order transfer function is to cascade second-order filters (if *n* is even) and one first-order (if *n* is odd). The cascade topology is a straight-forward topology that doesn't involve any feedback paths. Another alternative way of implementing higher-order filter is the Leap-Frog (LF) approach. The difference between these two approaches is that the overall transfer function of the cascade filter is highly sensitive to variations of the second-order section, while the Leap-Frog approach exploits low-sensitivity. The main drawback of the LF approach is that it is relatively difficult to tune [43].

FLF architecture was proposed in 1970s [44][45]. A new structure for the SC biquad was developed based on the FLF configuration, which can realize any n^{th}-order discrete-time transfer function [38]. This approach has the advantage of reduced sensitivity of the overall transfer function with respect to capacitances ratios and is easy to tune structure, unlike the LF technique, where varying only a few coefficients will alter the filter characteristics. The coefficients of the FLF design are obtained using a state-space variable approach.

2.4.2 State-space representation

For a transfer function H(z),

$$H(z) = \frac{V_{out}}{V_{in}}(z) = \frac{\sum_{j=0}^{n} \alpha_j z^{-j}}{1 + \sum_{k=1}^{n} \beta_k z^{-k}}$$

A signal flow graph similar to Figure 9 can be obtained for the above transfer function. The state-space representation is given as [38]

$$z\begin{bmatrix} x_o \\ x_1 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}\begin{bmatrix} x_o \\ x_1 \end{bmatrix}\begin{bmatrix} B_e \\ B_o \end{bmatrix} V_{in}$$

$$V_{out} = x_n + \alpha_o V_{in}$$

where

$$x_o = [x_1 x_3 x_5, \ldots\ldots, x_{n-3} x_{n-1}]$$

$$x_e = [x_2 x_4 x_6, \ldots\ldots, x_{n-2} x_n]$$

$$B_e = [b_0 b_2 b_4, \ldots\ldots, b_{n-4} b_{n-2}]$$

$$B_o = [b_1 b_3 b_5, \ldots\ldots, b_{n-3} b_{n-1}]$$

$$A_{11} = \left[\begin{array}{c} -\beta_1 \quad -\beta_3 \quad -\beta_5, \ldots\ldots, -\beta_{n-3} \quad -\beta_{n-1} \\ \hline 0 \end{array}\right]$$

$$A_{12} = \left[\begin{array}{c:c} -\beta_2 \quad -\beta_4 \quad -\beta_6, \ldots\ldots, -\beta_{n-2} & -\beta_n \\ \hline I_{(n/2)-1} & 0 \end{array}\right]$$

$$A_{22} = 0$$

$$A_{21} = I_{n/2}$$

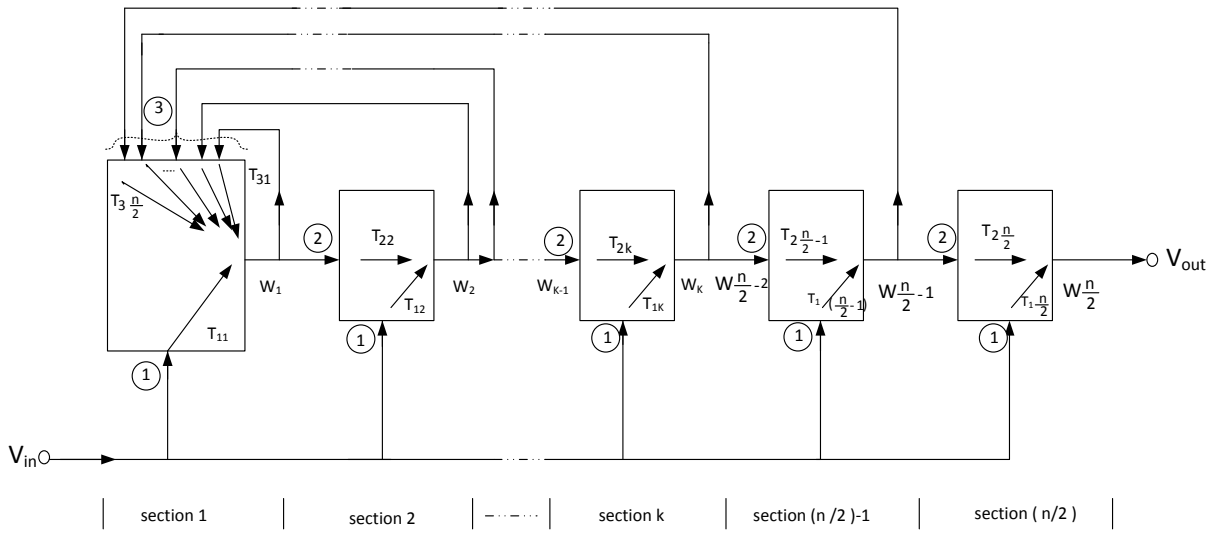

Figure 10. Generalized FLF architecture for a SC circuit.

According to Figure 10, we have

$$w_1 = T_{11}(z)V_{in} + \sum_{k=1}^{n/2} T_{3k}(z)\, w_k \tag{11}$$

$w_k = T_{1k}(z)V_{in} + T_{2k}(z)W_{k-1}$ for k = 2,3,…, n/2

where the transfer functions in equation (11) are defined as

$$T_{11}(z) = (b_1 + b_n\beta_{n-1})z^{-1} + \left(\alpha_n - \sum_{i=1}^{n/2} b_{2i}\beta_{2i}\right) z^{-2}$$

$T_{1k}(z) = b_{2k-1}z^{-1} + b_{2k-2}z^{-2}$ for k = 2, 3, …. , (n/2) -1

$T_{1n}(z) = b_n + b_{n-1}z^{-1} + b_{n-1}z^{-2}$

$T_{2k}(z) = z^{-2}$ for k = 2, 3, …., n/2 (12)

and

$T_{3k}(z) = -\beta_{2k-1}z^{-1} - \beta_{2k}z^{-2}$ for k = 1, 2, …., n/2

2.4.3 Switched-capacitor realisation

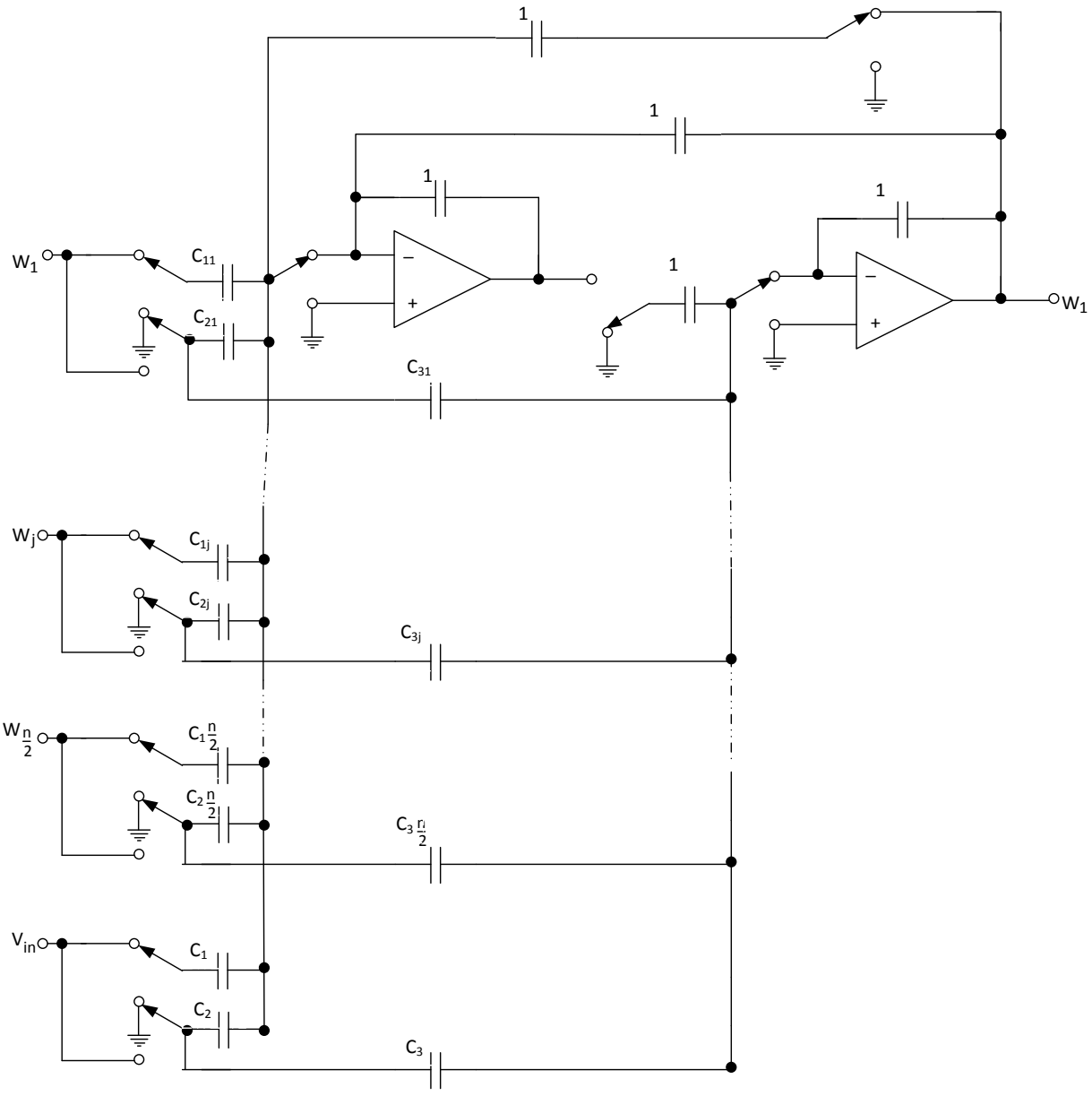

Figure 11.Switched-capacitor realization of input section (section 1) of Figure 10.

An FLF architecture for a SC is realized using two different sections. The above shown in Figure 11 is used to realise "section 1" of Figure 10, and a general biquad is modified to accommodate more than one input signal. The remaining sections are realised using Figure 12.

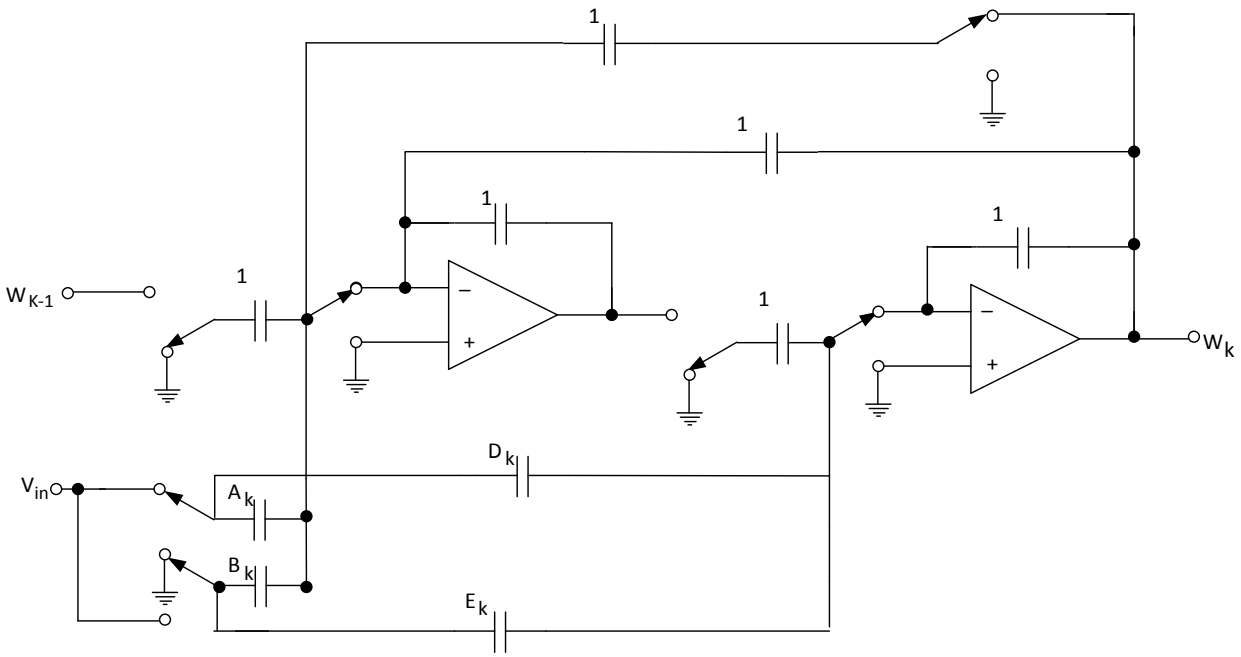

Figure 12. Switched-capacitor realization of Kth section of Figure 18

$$w_1 = T_{11}(z)V_{in} + \sum_{k=1}^{n/2} T_{3k}(z)w_k$$

And

$w_k = T_{1k}(z)V_{in} + T_{2k}(z)W_{k-1}$ for k = 2, 3, ….., n/2

The outputs of Figures 11 and 12 are obtained from [39], and are given as

$$w_1 = [(C_3 - C_1)z^{-1} + (C_2 - C_3)z^{-2}]V_{in} +$$

$$\sum_{k=1}^{n/2}[(C_{3k} - C_{1k})z^{-1} + (C_{2k} - C_{3k})z^{-2}]w_k \quad (13)$$

$$w_k = [-D_k + (E_k + D_k - A_k)z^{-1} + (B_k - E_k)z^{-2}]V_{in} + z^{-2}w_{k-1}$$

for k = 2, 3, …, (n/1)-1 (14)

2.4.4 Obtaining the feedback and feed forward design co-efficient

The design coefficients for n[th] order Follow-the-Leader Feedback based switched-capacitor filter can be obtained by comparing the design equations (12) (13) and (14)

$$b_i = \alpha_{n-i} - \sum_{\substack{k=1 \\ i \neq n}}^{n-i} \beta_k b_{i+k} \text{ for } i = 0, 1, \dots, n \tag{15}$$

$$\left.\begin{aligned} C_3 - C_1 &= b_1 + b_n \beta_{n-1} \\ C_2 - C_3 &= \alpha_n - \sum_{i=1}^{(n/2)-1} b_{2i} \beta_{2i} \end{aligned}\right\} \tag{16}$$

$$\left.\begin{aligned} C_{3k} - C_{1k} &= -\beta_{2k-1} \\ C_{2k} - C_{3k} &= -\beta_{2k} \text{for} k = 1, 2, \dots, n/2 \end{aligned}\right\} \tag{17}$$

$$\left.\begin{aligned} E_k - A_k &= b_{2k-1} \\ B_k - E_k &= b_{2k-2} \text{ for } k = 2, 3, \dots, (n/2) - 1 \end{aligned}\right\} \tag{18}$$

$$\left.\begin{aligned} D_{n/2} &= -\alpha_o \\ E_{n/2} + D_{n/2} - A_{n/2} &= b_{n-1} \end{aligned}\right\} \tag{19}$$

$$B_{n/2} - C_{n/2} = b_{n-2}$$

2.5 Chebyshev low-pass filter design procedure

SCs have become increasingly popular in recent years in filter design, because of the availability of the high quality switches that CMOS technology provides. The dependence of filter coefficients on capacitance ratios allows for precision on the order of 0.1% in switched capacitor filter implementations [47].

2.5.1 Low-pass filter response

A low-pass filter passes low frequency signals and attenuates frequency signals higher than the specified cutoff frequency. It is most widely used in conditioning signals prior to the analog-to-digital conversion, digital filters for image processing [46], and to filter high frequency noise signals [48].

A typical low-pass frequency response is shown in Figure 21. The frequency response of a low-pass filter is determined by 3dB cutoff frequency (f_c) after which the magnitude decreases for higher frequencies (ideally with a slope of 20dB per decade for a first-order filter).

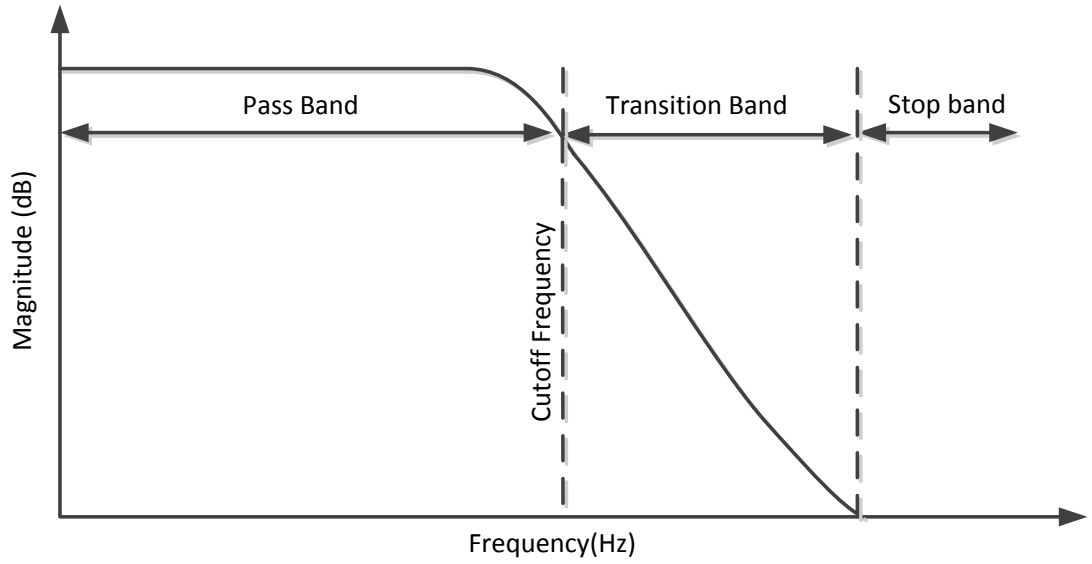

Figure 13. Normal low-pass filter frequency response

2.5.2 Chebyshev low-pass filter response

Generally, there are two types of Chebyshev low-pass filters

*Type 1*Chebyshev low-pass filter has an all-pole transfer function, an equi-ripple pass band and a monotonically decreasing stop band.

Type II Chebyshev low-pass filter has both poles and zeroes, and an equi-ripple stop band.

A steeper passband to stop-band transition region is achieved when compared to the Butterworth filter of the same order. The Chebyshev Type I filter is designed in this thesis, which will be discussed in later chapters.

2.5.2.1Chebyshev low-pass filter *Type I*

The Chebyshev *Type I* low-pass filter has ripples in passband and a flat stop band. Odd order filters have an attenuation band that extends from 0 dB to the ripple value. Even order filters have a gain equal to pass band ripple, and the number of cycles in the passband ripple is equal to the order of the filter, as shown in Figure 14.

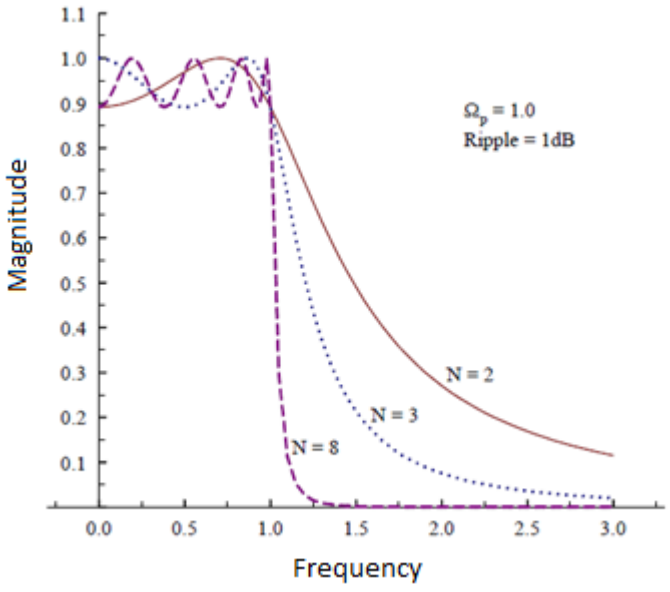

Figure 14. A Chebyshev low-pass filter response with even and odd orders

2.5.3 Filter design procedure

Step 1 :

The magnitude response of Chebyshev filter is given to be [56],

$|H(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2}}$ for any *N*

Where *N* is the order of the filter

The order of the filter *'N'* can be determined by using

$$N \geq \frac{cosh^{-1}\sqrt{(10^{0.1As}-1)/\varepsilon^2}}{cosh^{-1}(\omega_s/\omega_p)}$$

$\varepsilon = \sqrt{10^{0.1Ap}-1}$

Where As is the stop band attenuation (dB)

Ap is the passband ripple magnitude (dB)

ω_s = stop band attenuation frequency (Hz)

ω_p = pass band frequency (Hz)

Step 2 :

Once the order of the filter is determined, the pole location of the filter can be determined by using the following set of equations,

$s = \sigma + j\omega$

$$\sigma_k = \pm \sin(2K+1)\frac{\pi}{2N}\ sinh\frac{1}{N}sinh^{-1}\frac{1}{\varepsilon}$$

$$\omega_k = \cos(2K+1)\frac{\pi}{2N}cosh\frac{1}{N}cosh^{-1}\frac{1}{\varepsilon}$$

Where $K = 0, 1, \ldots., 2N - 1$

Step 3:

The values obtained in the *step 2* are compared to the biquadratic transfer function to design individual sections of higher order filters.

Another way to obtain the denominator polynomials is by using the Chebyshev low-pass filter table [56], where the values are denormalized according to the filter specification, and bilinear transformation is applied to the s-domain transfer function to obtain its equivalent z-domain transfer function.

CHAPTER 3 Inverter-based switched-capacitor design

3.1 CMOS inverter-based amplifiers

A single NMOS or PMOS at the inputs of an op-amp was replaced with a CMOS inverter [25] [26] to achieve a wide output swing and good dynamic range but with an increased power consumption due to the additional components and it would require an supply voltage of 1V or higher to provide enough voltage to drive the transistors into the saturation region. Rather than using a CMOS inverters to design an amplifiers, a CMOS inverter itself can be used as an amplifier [27] [28] [29], .

The advantages of using a CMOS inverter as an amplifier are

- Design simplicity with fewer components (less area).
- Ability to operate under lower supply voltage which is less than the sum of the threshold voltage of PMOS and NMOS ($V_{DD} \leq V_{thn} + |V_{thp}|$).

Very low power consumption is achieved by operating the transistors in weak inversion region during steady-state (low static power consumption) and high slew rate is achieved by driving one of the transistors into saturation during the switching process.

However, there are some disadvantages in the inverter-based design. Firstly, the design is highly sensitive to self-generated biasing point to process variation, which could be eliminated by auto-zeroing technique [30]. Secondly, the DC gain of a simple CMOS inverter-based amplifier can further be enhanced by using a cascaded inverter design and using current-starved inverter design with the cost of power consumption and overload of supply voltage for all those additional transistors [31]. Last but not least, the power supply rejection ratio (PSRR) is poor which make the noise effect on both ends (supply and ground) a serious issue.

Traditional op-amp designs have better PSRR compared to inverter-based amplifiers due to the presence of PMOS current source in the top which provide the supply current to the differential pair. A similar approach can be used in the inverter-based design to obtain an adequate PSRR of about 60dB [32]. The high output impedance of the tail current source makes the bias point of the inverter insensitive to power supply, hence increases the associated noise immunity. Additional NMOS current sink can be added at the bottom to provide better negative supply (suppress possible disturbance from the substrate noise) rejection ratio, forming a current-starved inverter. As mentioned above, all of these can be achieved with additional supply voltage.

3.2 CMOS inverter-based SC integrator

The op-amp is replaced with a simple CMOS inverter. The main concept of virtual ground, which is essential to initiate the charge transfer in a switched capacitor circuit is not available with a CMOS inverter as in the case of an op-amp. An op-amp has two input terminals, where the positive terminal is connected to ground and the negative terminal is forced to act as a virtual ground; however, a CMOS inverter is a single input and single output device. Even though a CMOS inverter does not have a virtual ground, the offset voltage of the inverter can be used to create a virtual ground at the inverter input terminal with the help of the offset storing capacitor C_C when a closed loop is formed [37]. The concept of creating virtual ground and charge transfer in an inverter based SC integrator is clearly explained in the forthcoming topics.

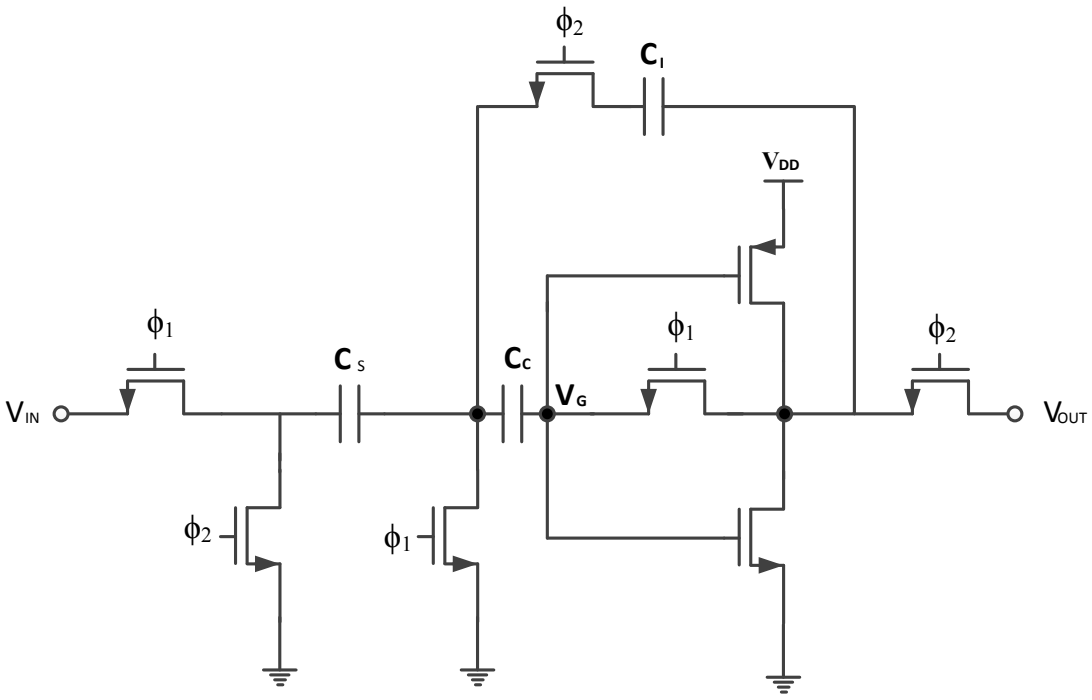

Figure 15. Schematic of a CMOS inverter-based SC integrator

During ϕ1, the offset of the inverter is sampled into C_C and, at the same time the input is sampled into the sampling capacitor C_S. During ϕ2, node V_G is forced to be the signal virtual ground in the presence of C_C (holding the offset of the inverter) and the closed loop formed by C_I provides the path for charge to transfer from C_S to C_I.

During phase ϕ1, both the transistors are turned off and operate in weak inversion, thus minimizing the steady state leakage current. During phase ϕ2, one of the transistors is turned on depending upon the node voltage V_G after the input signal is applied; this transistor operates in a strong inversion region. Again both transistors are turned off at the beginning of ϕ1.

The output is available only during clock phase ϕ2

$$\frac{V_O(Z)}{V_I(Z)} = \left(\frac{C_S}{C_I}\right)\frac{Z^{-1/2}}{1-Z^{-1}}$$

3.3 Operation of CMOS inverter

3.3.1 Operation of CMOS inverter during ϕ1

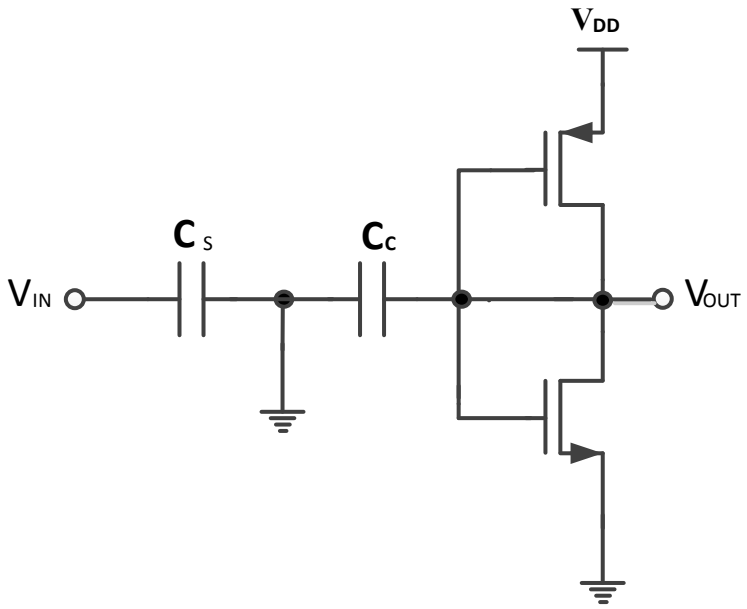

Figure 16.Operation of CMOS inverter based integrator during ϕ1

During ϕ1, the feedback switch is closed and a closed loop is formed by the feedback path and the offset of the inverter, which appears at the input, is stored in Cc. At the same time, Cs is charged with the input voltage V_{IN}. At this point, both PMOS and NMOS stay in the weak inversion region.

3.3.2 Operation of CMOS inverter at the beginning of ϕ2 :

Depending on the polarity of the input V_{IN}, either PMOS or NMOS is driven into the strong inversion region and a charge transfer occurs because of the negative feedback that is formed. This provides a high slew rate at the output because one of the transistors is operating in the strong inversion region during the charge transfer.

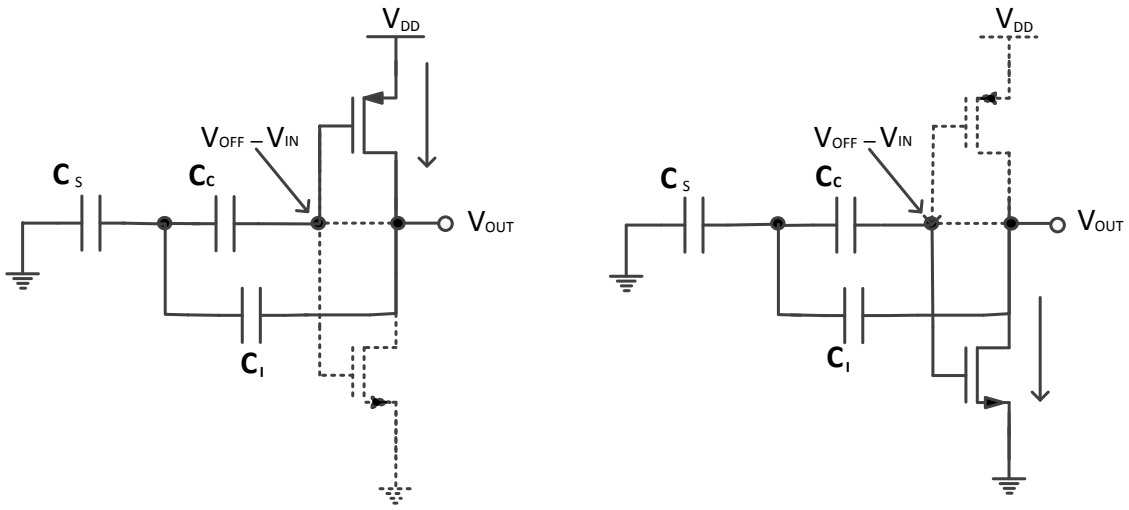

Figure 17. (a) When Vin >0 (b) When Vin < 0, NMOS

3.3.3 Steady state operation of CMOS inverter at ϕ2 :

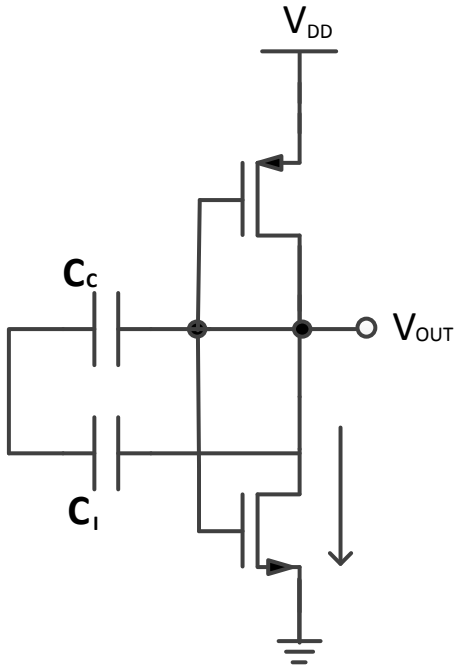

Figure 18. Steady state operation during ϕ2

During the steady state operation, both PMOS and NMOS are driven into the weak inversion region since the supply voltage V_{DD} chosen is $V_{DD} \leq V_{th(n)} + |V_{th(p)}|$, thereby reducing the static power consumption of the inverter.

3.4 Design of CMOS inverter-based SC Integrator in Cadence

The CMOS inverter-based integrator is designed with the TSMC 65nm technology with the following specifications,

VDD = 0.7V Vin = 50mV Fin = 1 MHz C_S = 250fF C_I = 1pF

The inverter is designed to operate with the supply voltage VDD ≤ Vth(n) + Vth(p) in order to reduce the static power dissipation of the inverter during the idle state. The circuit in Figure 19 was simulated to measure the threshold voltage of NMOS transistor, which is 0.353V. Performing a similar analysis with a PMOS transistor resulted in |-0.360V|.

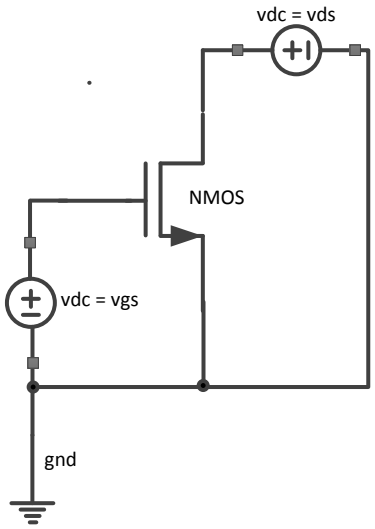

Figure 19.NMOS configuration to obtain its threshold voltage.

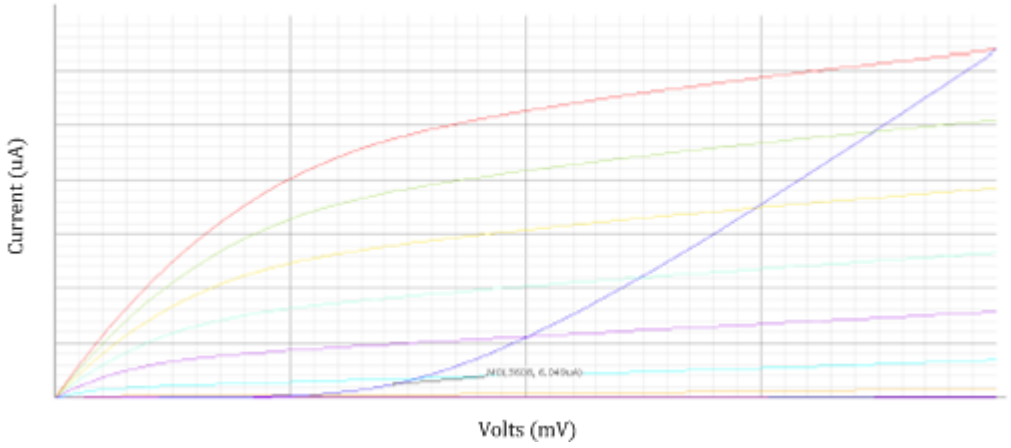

Figure 20. Ids vs Vth plot for NMOS transistor

The designed inverter based SC integrator is verified for a sine wave input as shown in Figure 21 and Figure 22 respectively.

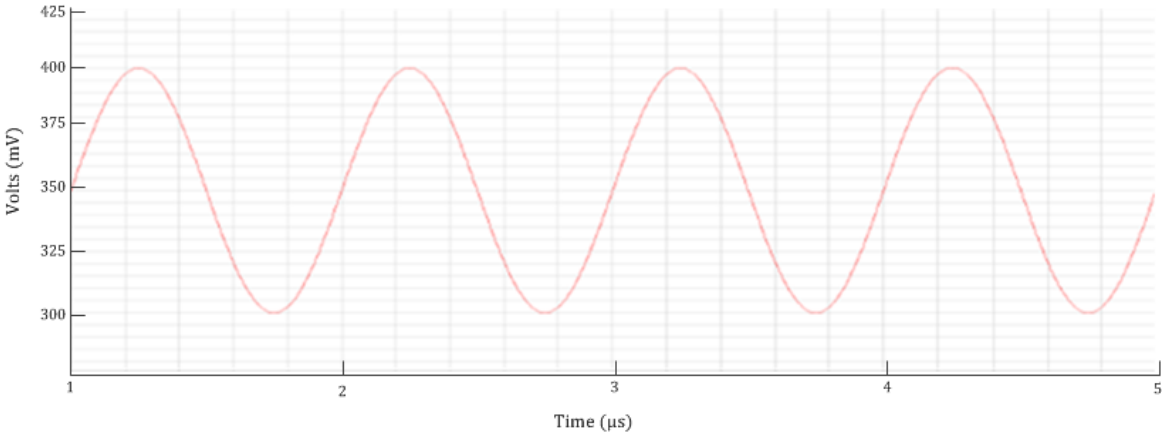

Figure 21. Input sine wave for the integrator

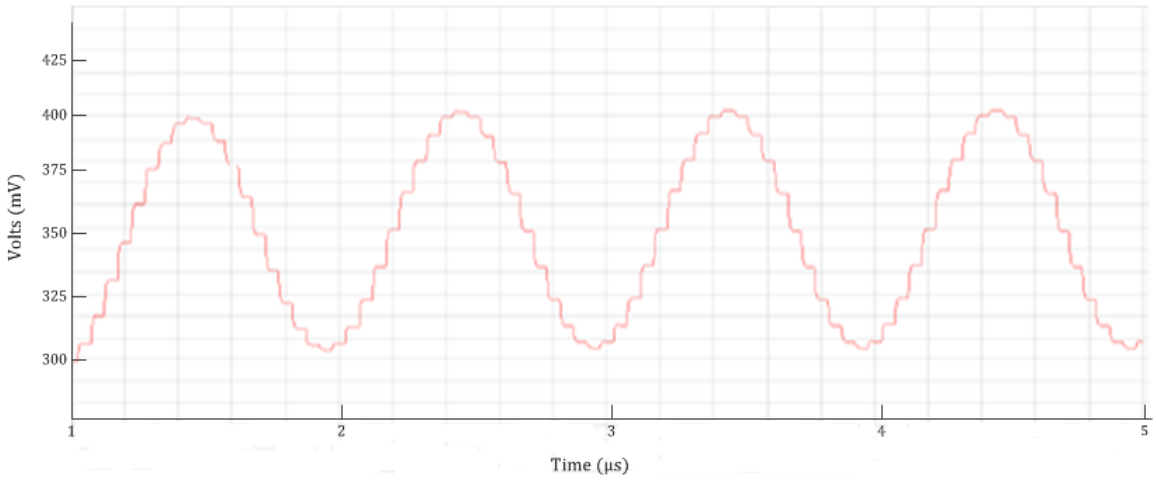

Figure 22. Output of the integrator for a sine wave input

3.5 Parameters of CMOS Inverter-based Integrator

3.5.1 Supply Voltage

An inverter circuit has to be designed to provide a high slew rate with minimum power dissipation, which is achieved by selecting the supply voltage Vdd <= Vtn+|Vtp|. The threshold voltage of NOMS and PMOS are 0.353V and |-0.360V|, respectively, in TSMC65nm technology; hence, 0.7 volts is chosen, which drives both PMOS and NMOS into weak inversion during the steady state (sampling phase) in order to reduce static power dissipation. A high slew rate is achieved by driving one of the transistors into the saturation region during the integrating phase, depending on the input. The VTC characteristics show that full output swing is obtained with the CMOS inverter circuit even at a lower supply voltage.

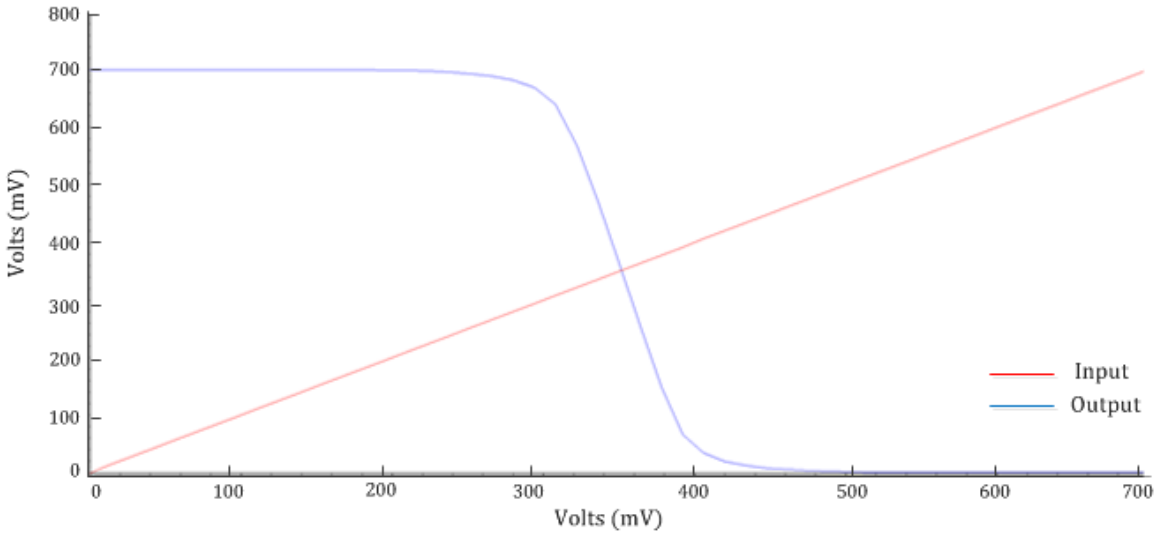

Figure 23. VTC characteristics of a CMOS inverter

3.5.2 Power Consumption

In a CMOS inverter, the total power consumption is usually the sum of static power: when input is not switching, and dynamic power: this is caused due to charging and discharging of load capacitance and the short circuit path that exists when both PMOS and NMOS are turned *on* at the same time. Static power in a CMOS inverter can be due to leakage sources in the transistors which include subthreshold conduction between the source and drain, and reverse bias pn-junction leakage between the source/drain and the substrate. In order to measure the static power dissipation, a static input signal is applied so that no switching action occurs.

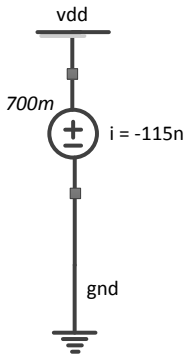

Figure 24. Static current from a power supply of 0.7V

Static power consumed when V_{in} = 0.7V is $P_{stat} = 115*10^{-9} + 0.7 = 80.5nW$

Dynamic power is due to the charging and discharging of the load capacitance when a transition take place at the input from high to low or low to high, which is given by

$C_L * (V_{dd})^2 * f = 1pF * (0.7)^2 * (1/10us) = 49nW$

Hence the total power consumption is 129.5nW

The CMOS inverter-based SC operates in the weak inversion region during the steady state and consumes significantly less power.

3.5.3 Settling Time and Slew Rate

Slew rate is the rate at which output changes for a step change in the input, which is how quickly the systems responds to a large signal change. Settling time is the time taken for the output to settle to a final value within the specified error band. It is shown in the figure that the time taken to reach its maximum value is 20ns with a load capacitor of 1pF. The CMOS inverter has a high slew rate of 2.5 V/µs and settling time of 20ns.

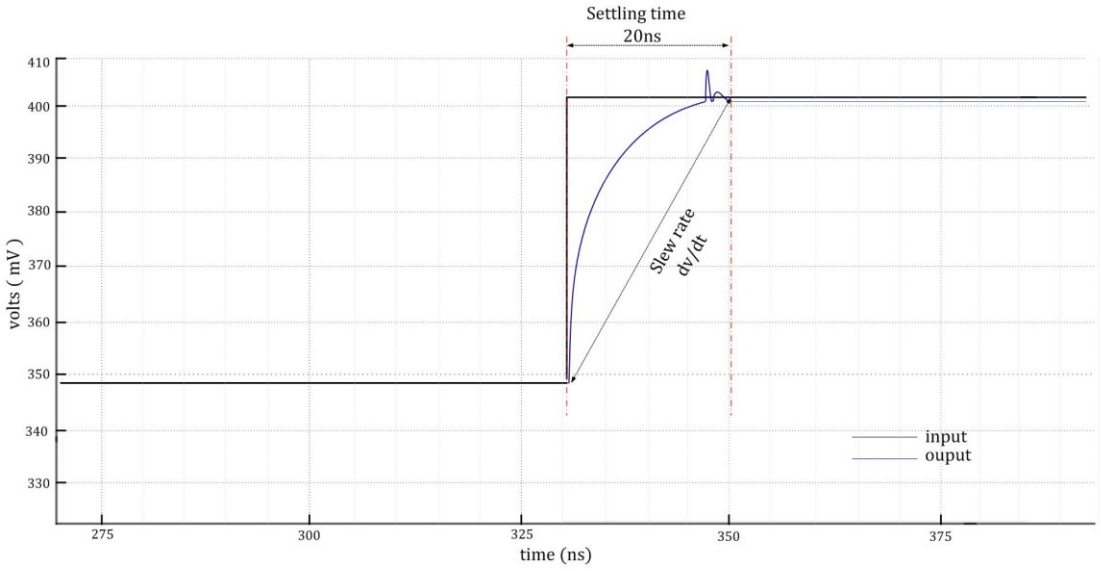

Figure 25.Output response to a step input signal

$$Slewrate = \frac{400mV(high) - 350mV\ (low)}{350ns - 330ns} = \frac{50mV}{20ns} = 2.5\ \text{V/}\mu\text{s}$$

The settling time at the output depends on the transistor size and the supply voltage, faster settling can be achieved by increasing the size of the transistor and also at the cost of supply voltage.

3.5.4 Power Supply Rejection Ratio (PSRR)

In general, the supply voltage of any circuit should be steadily maintained in order for the circuit to be stable and produce the desired results. However, in practical considerations, the supply voltage is not stable and it affects the output. In a CMOS inverter, both PMOS and NMOS operate in the weak inversion region during the steady state period to reduce the power consumption of the circuit. The weak inversion region operation of PMOS depends on the gate voltage (V_{GS}) at the input and the supply voltage (V_{DD}). In a simple CMOS inverter, PMOS is directly tied to the supply voltage and any change in V_{DD} will drive the transistor into either the cut-off region or saturation. The change in supply voltage will produce an output voltage change. This ratio is generally called the Power Supply Rejection Ratio (PSRR), expressed in dB.

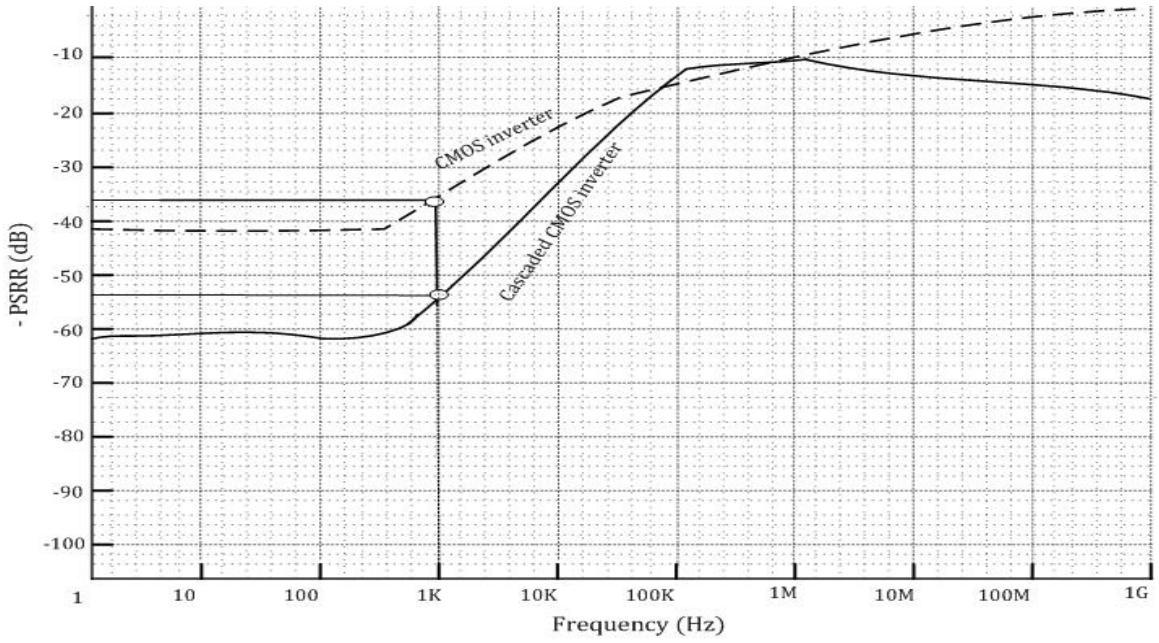

Figure 26. PSRR vs. frequency plot of CMOS inverter

The PSRR is measured at the negative terminal of the supply voltage, hence " -dB ". It is seen from the plot, a simple CMOS inverter has a poor PSRR which is around 37dB at 1KHz and with increasing frequency degrades to 15dB at 1MHz which is very low comparing to [49]. A good supply voltage rejection ratio is achieved by adding a PMOS current source in addition to the existing PMOS and NMOS transistors that certainly increases the power consumption of the circuit, which is still significantly low compared to traditional op-amp designs. The PSRR for the cascaded inverter design is around 54dB at 1KHz and 15dB at 1MHz.

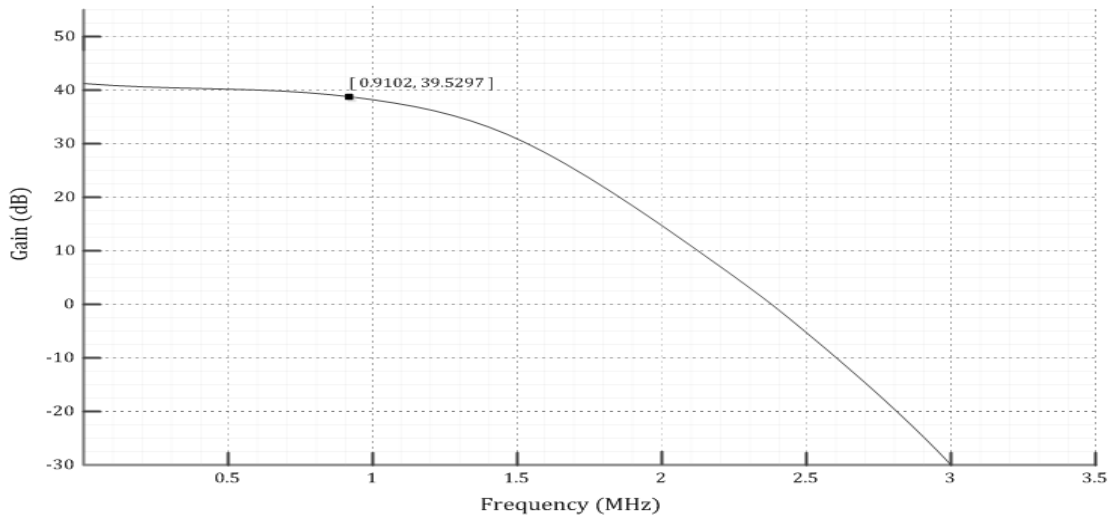

Figure 27. DC gain plot of a CMOS inverter

3.5.5 Noise Analysis

The dominant noise sources in an MOS transistor are flicker noise and thermal noise. The flicker noise dominates at a low frequency because it has an increasing spectral density (1/f) slope towards low frequency and thermal noise, otherwise known as white noise, dominates at higher frequencies.

Thermal noise:

The channel noise of a MOSFET in saturation is usually written as [50],

$$\frac{i^2}{\Delta f} = 4kT \in g_m \quad (20)$$

$\in$ is a bias dependent parameter which is known to be $\in$ = 2/3 for a MOSFET in strong inversion and $\in$ = 1/2 for a weak inversion MOSFET.

g_m is the transconductance of the device.

Equation (20) can also be written as

$$I^2_{(thermalnoise\ )} = 4kT \in g_m [A^2/Hz] \quad (21)$$

Assuming that the transconductance of both PMOS and NMOS are nearly the same, the thermal noise voltage of CMOS inverter is

$$v^2_{(thermalnoise\ )} = \frac{2kT\in}{g_m}[v^2/Hz] \quad (22)$$

Since the g_m of a transistor operating in a weak inversion region is five times larger than that of the transistor operating in the saturation region [51], the thermal noise of the CMOS inverter operating in weak inversion is much less.

Flicker noise :

Another dominant noise source of a CMOS inverter is flicker noise, which is given by [37]

$$v^2_{(flickernoise\ )} = \frac{K}{C_{ox}WL}\frac{1}{f}\ \ [\ v^2/Hz\ ] \quad (23)$$

Where W and L are the width and length of a transistor,

C_{ox} is the gate capacitance per unit area

f is the frequency

K is a process-dependent parameter

The auto zeroing technique used in the integrator structure strongly reduces the low frequency flicker noise [51]. This advantage is obtained at the cost of an increased white noise floor due to the noise folding associated with sampling. The foldover thermal noise of a CMOS inverter based integrator is expressed as

$$v^2_{(foldovert\ hermalnoise\ )} = \frac{GB}{f_s}\cdot v^2_{(thermalnoise\ )} = \frac{GB}{f_s}.\frac{kT}{g_m}[v^2/Hz] \quad (24)$$

Where f_s the sampling frequency and GB is is the gain bandwidth of an inverter. It can be seen that the thermal noise is amplified by a factor GB/f_s which is chosen to be 5 [37] while the flicker noise is attenuated by an auto zeroing process, foldover thermal noise is the dominant in a CMOS inverter-based SC integrator.

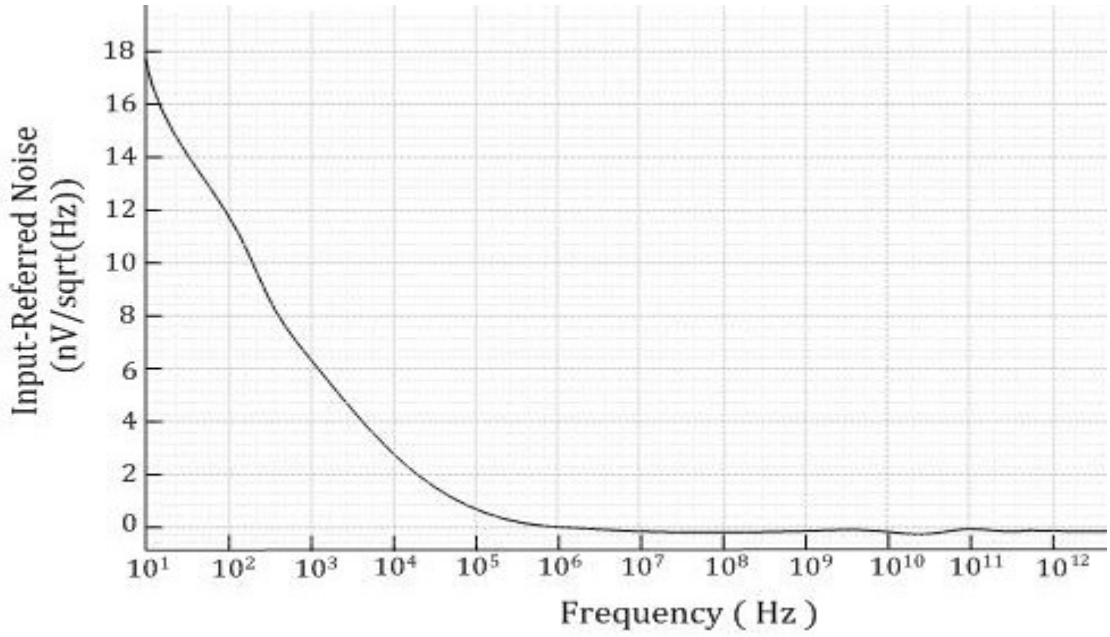

Figure 28. Input-referred noise of a CMOS inverter

Intrinsic noise in an op-amp is given as [53],

$$\frac{16\ kT}{3\ g_m} + \frac{K}{C_{ox} WL}\frac{1}{f} \approx \frac{16\ kT}{3\ g_m} \quad (25)$$

Intrinsic noise in a CMOS inverter is [37],

$$\frac{GB}{f_s} \cdot \frac{kT}{g_{mw}} \approx \frac{kT}{g_m} \quad (26)$$

Thus, from (25) and (26) the noise in both designs is inversely proportional to the input transconductance. The input transconductance of a CMOS inverter is high compared to an

op-amp because in an op-amp the input drives either an NMOS or PMOS, whereas in a CMOS inverter the input is applied to the gates of both NMOS and PMOS which are tied together (twice the transconductance), eventually reducing the noise in a CMOS inverter.

	Noise v_{noise}^2 [V^2/Hz]
Op-amp based SC integrator	$\frac{16}{3}\frac{kT}{g_m} + \frac{K}{C_{ox}WL}\frac{1}{f}$
CMOS inverter based SC integrator	$\frac{GB}{f_s}\cdot\frac{kT}{g_{mw}} \approx \frac{kT}{g_m}$

Table 2. Intrinsic noise comparison of op-amp and CMOS inverter

Performance parameters of the designed CMOS inverter

Gain	42.34 dB
Gain bandwidth product	35.98MHz
Unity gain bandwidth	2.23MHz
Supply voltage	0.7V
Power consumption	129.5nW
Input-Referred Noise at 1KHz	6.1nV/sqrt(Hz) @ $V_{in\ p\text{-}p}$ = 100mV
PSRR	43dB
Slew rate	2.5 V/μs
Settling time	20ns

Table 3. Performance parameters of a CMOS inverter-based integrator

CHAPTER 4 Switched-capacitor filter design

4.1 CMOS Inverter-based SC Biquad

A CMOS inverter-based SC circuit capable of realizing a biquadratic transfer function based on [36] is shown in Figure 29.

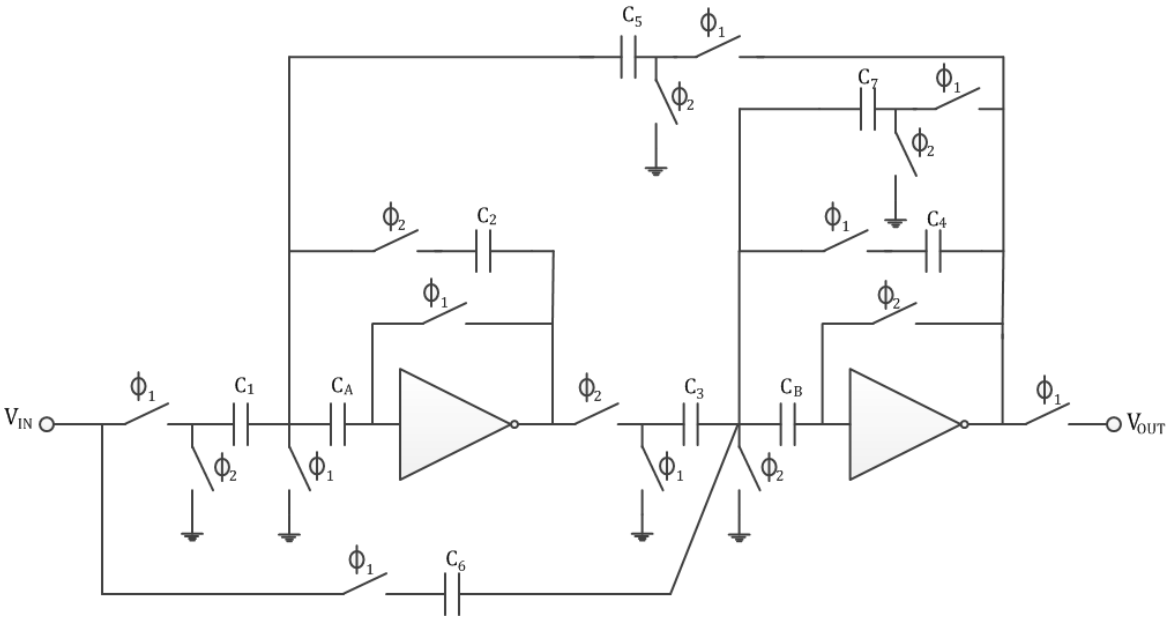

Figure 29. CMOS inverter-based SC biquad design

The z-domain biquadratic transfer function for the above shown SC biquad is obtained to be

$$\frac{V_o(Z)}{V_I(Z)} = \frac{\left(\frac{C_6}{C_4}\right)Z^2+\left(\frac{C_1C_3}{C_2C_4}-2\frac{C_6}{C_4}\right)Z+\frac{C_6}{C_4}}{\left(1+\frac{C_7}{C_4}\right)Z^2+\left(\frac{C_5C_3}{C_2C_4}-\frac{C_7}{C_4}-2\right)Z+1} \quad (26)$$

4.2 Cascade realization of Sixth-order Chebyshev Low-pass Filter

A sixth-order filter is designed using three biquad sections in cascade. Sixth order Chebyshev filter is chosen because it has passband ripples, and the order of the filter can be verified. The transfer used for the biquads are given below,

$$H_1(Z) = \frac{0.7050\ Z^2 + 1.4100\ Z + 0.7050}{1.1147\ Z^2 + 1.0499\ Z + 1} \quad (27)$$

$$H_2(Z) = \frac{0.7152\ Z^2 + 1.4304\ Z + 0.7152}{1.5647\ Z^2 + 0.6457\ Z + 1} \quad (28)$$

$$H_3(Z) = \frac{0.5844\ Z^2 + 1.1689\ Z + 0.5844}{3.8197\ Z^2 - 2.1951\ Z + 1} \quad (29)$$

The above transfer functions (27) (28) (29) were obtained for the filter specifications of a passband ripple magnitude (A_P) of 1dB, and a stop-band attenuation (ω_s)of40dB with a sampling frequency (f_s) of 3MHz.

The SC filter is designed with cadence TSMC65nm technology, as a simple AC analysis will not produce the desired results for an SC circuit. Hence, a PSS (Periodic Steady-State) analysis has to be performed with only clock signals and the transient input is disabled, followed by a PAC analysis.

The capacitor values for the cascaded design are obtained by comparing (27) (28) and (29) with (26) and given in Table 4 below,

	Biquad I	Biquad II	Biquad III
C_1	1.6792	1.6913	1.5289
C_2	1	1	1
C_3	1.8845	1.8981	1.7166
C_4	1	1	1
C_5	1.6792	1.6913	1.5289
C_6	0.7050	0.7152	0.5844
C_7	0.1147	0.5647	2.8197

Table 4. Capacitor values for sixth-order Chebyshev low-pass filter cascade design

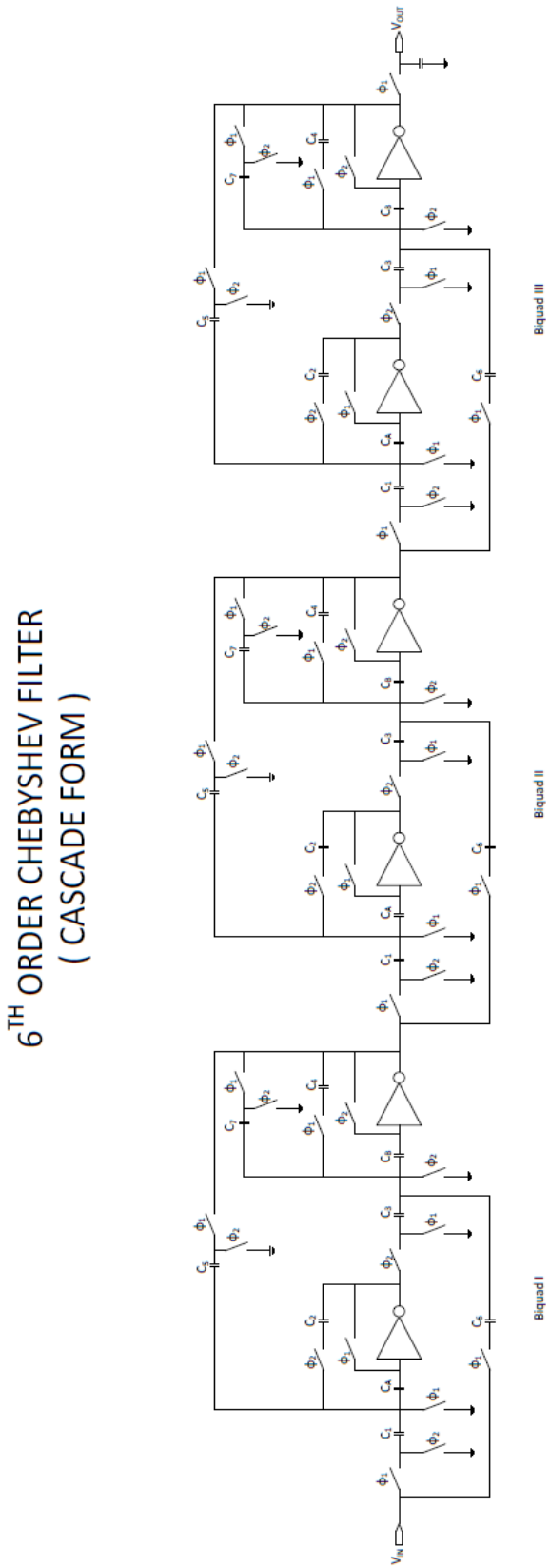

Figure 30. Sixth-order Chebyshev low-pass filter cascade design

4.3 Implementation of Inverter-based FLFSC Filter

$$H(Z)$$

$$= -\frac{0.0442 + 0.2653\,Z^{-1} + 0.6633\,Z^{-2} + 0.8844\,Z^{-3} + 0.6633\,Z^{-4} + 0.2653\,Z^{-5} + 0.0442\,Z^{-6}}{1 + 0.7799\,Z^{-1} + 1.4082\,Z^{-2} + 0.2205\,Z^{-3} + 0.5185\,Z^{-4} - 0.0749\,Z^{-5} + 0.1500\,Z^{-6}} \quad (30)$$

Above the sixth-order transfer function is compared to (32),

$$H(Z) = \frac{\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2} \alpha_3 Z^{-3} \alpha_4 Z^{-4} \alpha_5 Z^{-5} \alpha_6 Z^{-6}}{1 + \beta_1 + \beta_2 + \beta_3 + \beta_4 + \beta_5 + \beta_6} \quad (31)$$

And the values of α's and β's obtained are given in Table 5.

The values b_o, b_1,…., b_6 obtained using the equation (32)

$$b_i = \alpha_{n-i} - \sum_{\substack{k=1 \\ i \neq n}}^{n-i} \beta_k b_{i+k} \text{ for} i = 0, 1, \ldots., n \quad (32)$$

For example,

$$b_6 = \alpha_{6-6} = \alpha_0 = -0.0442$$

$$b_5 = \alpha_{6-5} - \sum_{k=1}^{1} \beta_1 b_{1+5} = \alpha_1 - \beta_1 b_6 = -0.2308$$

$\alpha_o = -0.0442$	$\beta_1 = 0.7799$	$b_0 = -0.1277$
$\alpha_1 = -0.2653$	$\beta_2 = 1.4082$	$b_1 = 0.1183$
$\alpha_2 = -0.6633$	$\beta_3 = 0.2205$	$b_2 = 0.1759$
$\alpha_3 = -0.8844$	$\beta_4 = 0.5185$	$b_3 = -0.2213$
$\alpha_4 = -0.6633$	$\beta_5 = -0.0749$	$b_4 = -0.4210$
$\alpha_5 = -0.2653$	$\beta_6 = 0.1500$	$b_5 = -0.2308$
$\alpha_6 = -0.0442$		$b_6 = -0.0442$

Table 5.Values of α's, β's and b's for FLF implementation

The design equations (15) – (19) are solved using the values of α's, β's and b's and the obtained capacitor values are displayed in Table 6. Since the number of unknowns is greater than the number of equations, the equations are solved by assuming certain initial values for some capacitors in such a way to avoid negative capacitance which is impossible to realize in an SC circuit.

The capacitance values shown in the Table 6are the final scaled values.

C_1	0
C_2	1
C_3	1
C_{11}	45.57
C_{12}	15.39
C_{13}	1.564
C_{31}	1.408
C_{32}	4.262
C_{33}	1.233
C_A	20.83
C_B	8.22
C_C	1
C_D	1
C_E	3.289
C_F	22.62
A_{11}	20.83
A_{12}	20.83
A_{21}	1
A_{22}	1
A_{31}	3.289
A_{32}	3.289
B_{11}	8.220
B_{21}	1
B_{22}	1
B_{31}	3.289
B_{32}	22.62
A_2	1.221
B_2	1.175
E_2	1
A_3	3.289
B_3	1
E_3	16.39
D_3	1

Table 6. Capacitor values for FLF implementation

6th ORDER CHEBYSHEV FILTER BASED ON FLF

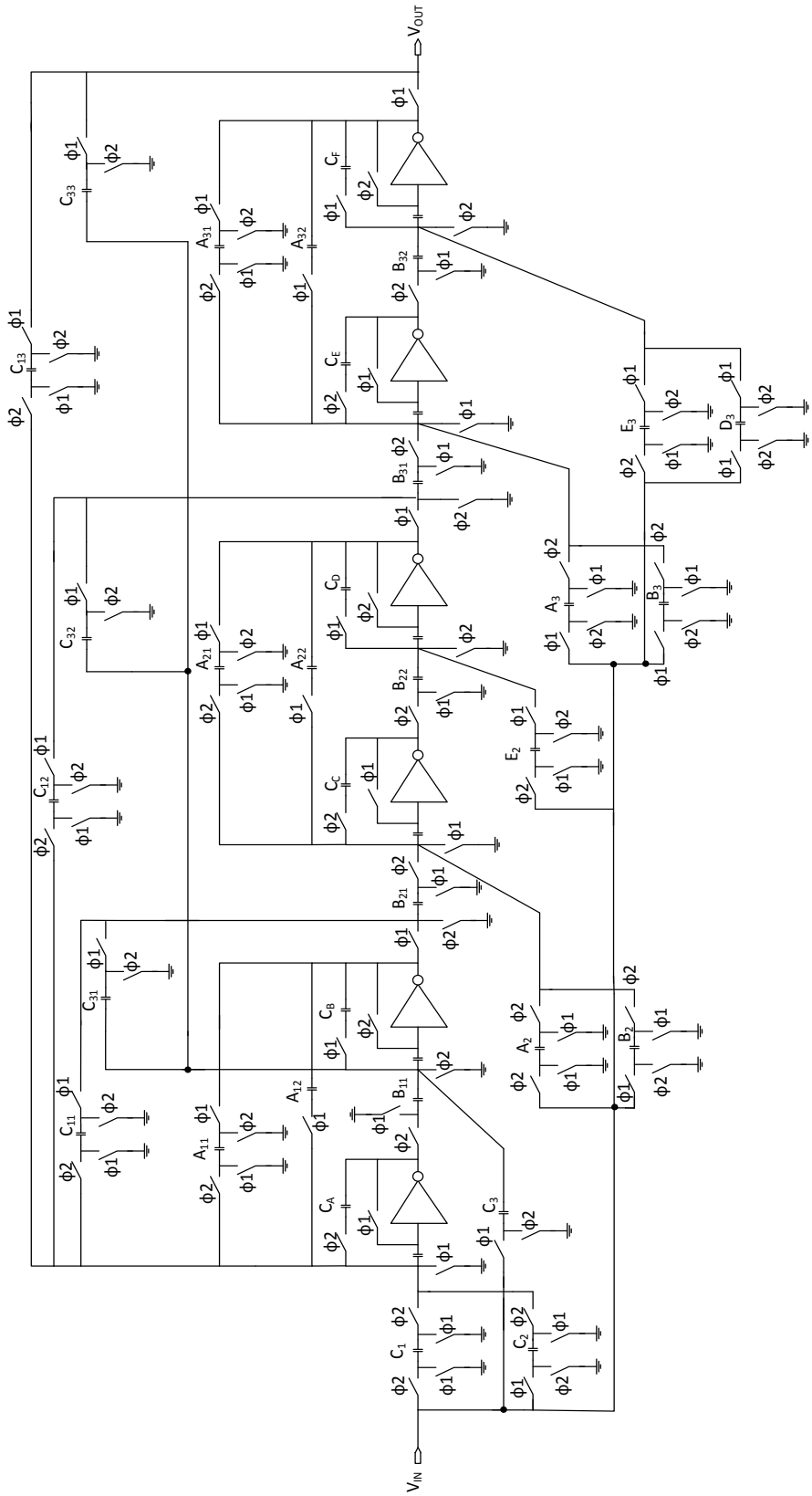

Figure 31. Sixth-order Chebyshev low-pass filter FLF design

CHAPTER 5 Simulation results

5.1 Simulating SC Circuit in Cadence

Periodic Steady-State (PSS) analysis has to be performed as step one, in order to calculate the periodic steady-state response of a circuit. It is a large-signal analysis and uses a simulation technique known as the *shooting method* to perform the analysis. This analysis is performed to determine the initial conditions of the circuit in steady-state.

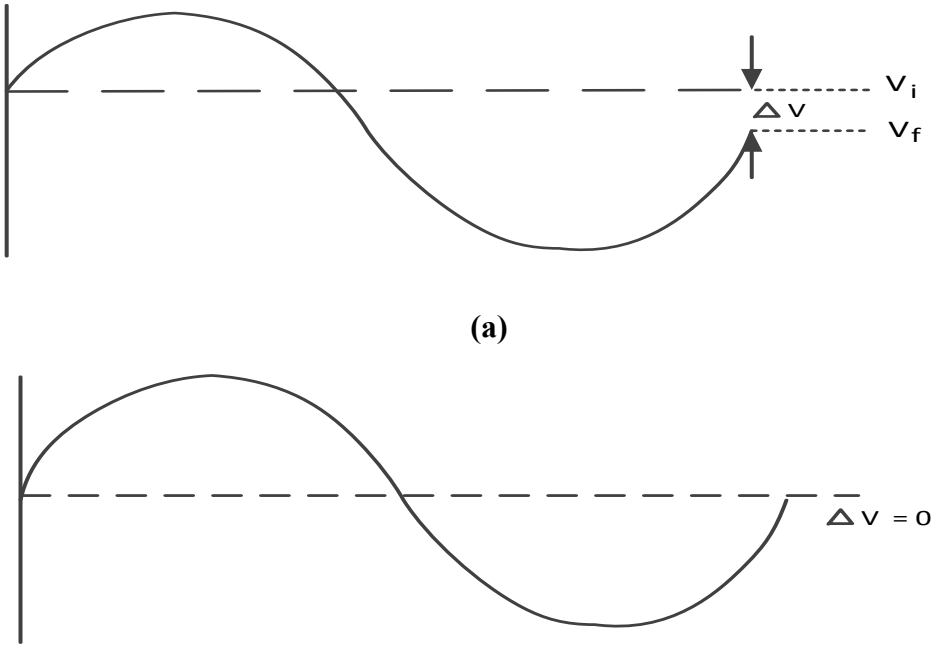

Figure 32. (a) Non-periodic signal (b) Periodic signal

Shooting methods are iterative methods that begin the simulation with an estimation of the desired initial condition that result in the signal being periodic as defined by $v_f - v_i = \Delta v = 0$. The signal in Figure 32 (a) start at v_i and end at v_f does not result in periodicity. For the signal in Figure 32 (b), the starting point was adjusted by the shooting method to directly result in a periodic steady-state. The circuit is evaluated for one period starting with the initial condition and the final state (v_f) of the circuit is computed along with the sensitivity of the final state with respect to the initial state. The non-periodicity ($\Delta v =$

$v_f - v_i$) and the sensitivities are used to compute a new initial condition. If the final state obtained is a linear function of the initial state, then the new initial condition results in periodicity. If not, the process repeats and additional iterations are needed [54].

Periodic Small-Signal (PAC) analysis is similar to the conventional-small signal analysis, but can be applied to periodic circuits. The conventional small-signal analyses do not linearize about the DC or time-invariant operating point and they can cannot be used for circuits that include frequency conversion effects. Once the circuit is linearize about a periodic operating point using the PSS analysis, a periodic AC analysis can be performed to determine the frequency response characteristics of the switched capacitor circuits.

5.2 Monte Carlo Analysis

5.2.1 CMOS Inverter-based Cascade Sixth-order Chebyshev Filter

The sensitivity performance of the designed filter is demonstrated by the Monte Carlo simulations using Cadence, and the generated results are plotted using Matlab. It is assumed that all the capacitors are randomly perturbed about their nominal value by random percentages. The parametric simulation in Cadence is performed for 100 runs based on the fact that the capacitances on a single circuit are highly correlated, and that they deviate from their nominal values by random percentage of the same sign and nearly the same values [38]. Performing more runs will provide more accurate results but it is time consuming; the result obtained for 100 runs is shown in Figure 33.

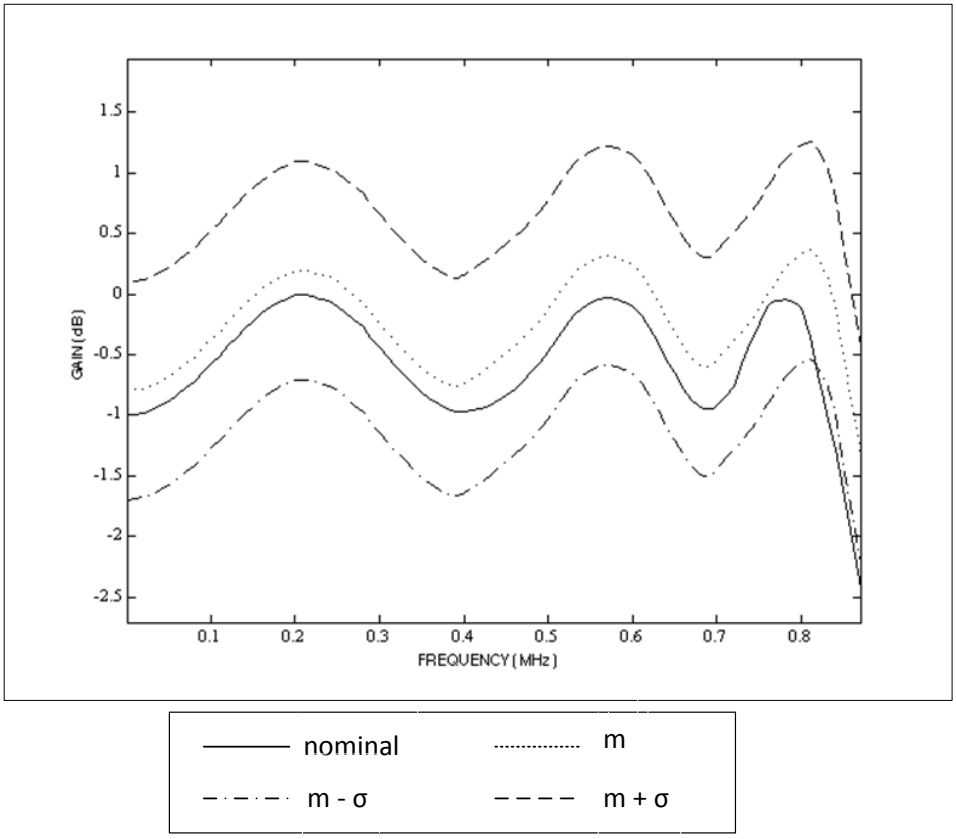

Figure 33. Response of CMOS inverter based SC filter (Cascade design)

Frequency (MHz)	Nominal (dB)	Mean (dB)	Mean + Standard deviation (dB)	Mean – Standard deviation (dB)
0.1	-0.9901	-0.3742	0.5321	-1.2710
0.3	-0.4462	-0.2472	0.6671	-1.1405
0.5	-0.4872	-0.1316	0.7757	-1.0378
0.7	-0.9216	-0.5502	0.3593	-1.4595
0.8	-0.1217	0.3391	1.2372	-0.5761

Table 7.Monte Carlo analysis for Cascade design

It is seen that the design is highly sensitive to component variation. The sensitivity of the design with respect to transfer function can be reduced using the FLF approach illustrated in Figure 31.

5.2.2 CMOS Inverter-based FLF Sixth-order Chebyshev Filter

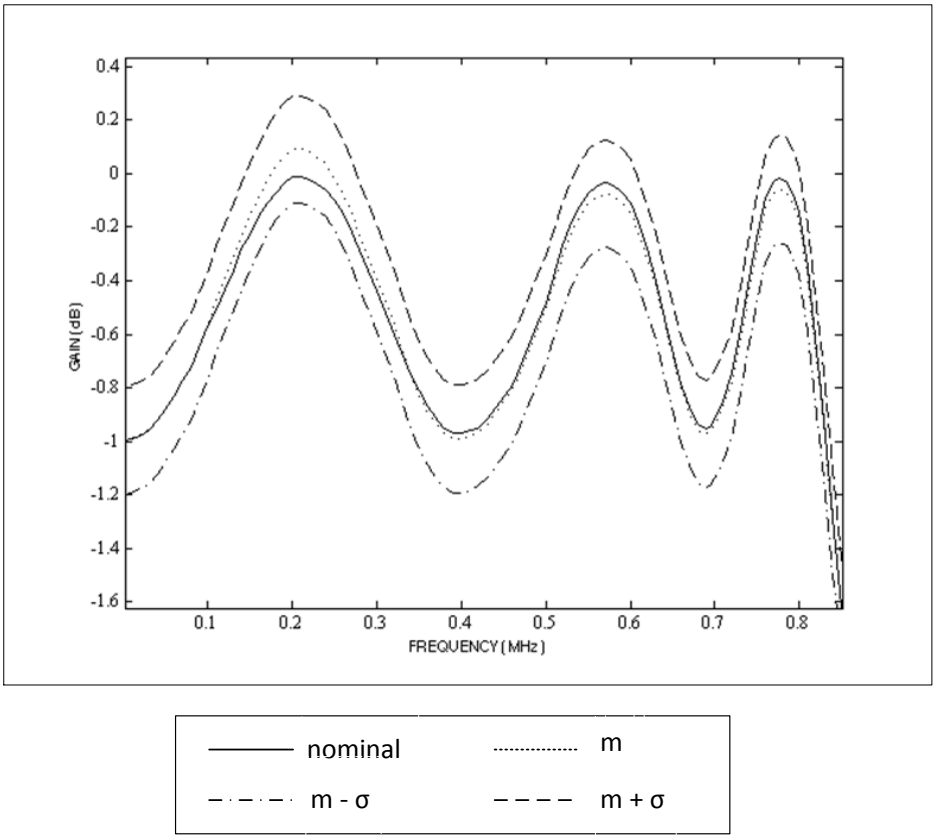

Figure 34. Response of CMOS inverter based SC filter design (FLF)

Frequency (MHz)	Nominal (dB)	Mean (dB)	Mean + Standard deviation (dB)	Mean – Standard deviation (dB)
0.1	-0.5712	-0.5782	-0.3719	-0.7719
0.3	-0.4485	-0.3918	-0.1972	-0.5962
0.5	-0.4890	-0.5048	-0.3094	-0.7079
0.7	-0.9217	-0.9483	-0.7428	-1.1429
0.8	-0.1452	-0.1894	0.0292	-0.3817

Table 8. Monte Carlo analysis for CMOS inverter based FLF

The obtained results in Figure 34 clearly show that the component variation of FLF based SC design is less sensitive compared to cascade design.

5.2.3 CMOS Op Amp-based FLF Sixth-order Chebyshev Filter

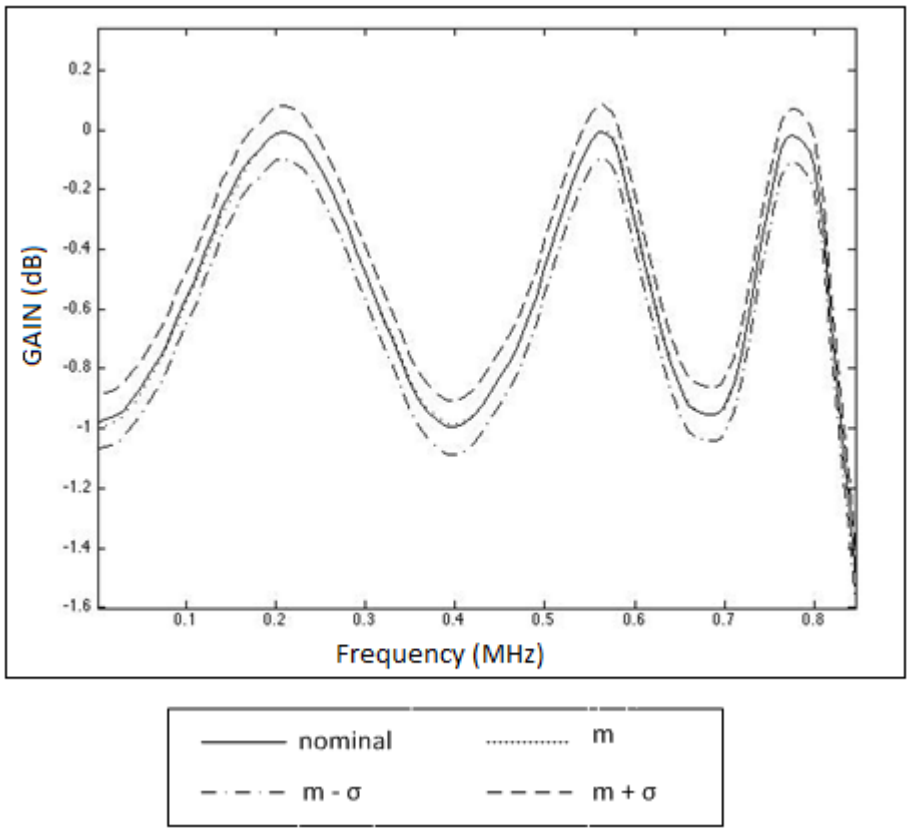

Figure 35.Response of op-amp based SC filter design(FLF)

Frequency (MHz)	Nominal (dB)	Mean (dB)	Mean + Standard deviation (dB)	Mean – Standard deviation (dB)
0.1	-0.5619	-0.5701	-0.4729	-0.6563
0.3	-0.4882	-0.4890	-0.3918	-0.5794
0.5	-0.4651	-0.4695	-0.3715	-0.5541
0.7	-0.9229	-0.9228	-0.8378	-1.0182
0.8	-0.1249	-0.1283	-0.0310	-0.2177

Table 9. Monte Carlo analysis for op-amp based FLF

It is seen from Figure 35 that the transfer function sensitivity of the op-amp based filter is considerably less compared to that of Figure 34. However, the inverter-based SC filter design is superior in other aspects such as low power consumption, low supply voltage, fast settling time and a high slew rate. The purpose of this thesis is to illustrate that an SC filter design is capable of operating under low supply voltage, while consuming far less power.

CHAPTER 6 DTMOS based switched-capacitor design

6.1 Ultra low-voltage and low-power design solutions

One of the most important parameter to be considered in low-voltage and low-power designs is the dynamic range of a circuit. The dynamic range is defined as the range between the maximum and minimum signal amplitude. The maximum signal level is limited by the power supply and the minimum signal level by the noise floor. The amplifiers, filters and other analog signal processing circuit blocks are often realized using op-amps. The dynamic range of the op-amp is affected at very low supply voltages and the low supply voltage limits the input signal common-mode rage (CMR). However, a rail-to-rail input CMR can be achieved with nonconventional techniques such as a floating-gate (FG), quasi-floating-gate (QFG), bulk-driven (BD), dynamic threshold MOS (DTMOS) input transistors rather than conventional gate driven input stage.

6.1.1 Floating-gate input stage:

Floating-gate (FG) MOS transistor is a device whose gate terminal is not resistively connected to anywhere. The gate voltage is set by the capacitive voltage division given by

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{Q_{FG}}{C_T}$$

Where N is the number of inputs, V_i, V_D and V_s are the input, drain and source voltages, C_{GD}, C_{GS} and C_{GB} are the parasitic capacitances and C_T is the sum of all capacitors connected to the floating gate.

$$C_T = \sum_{i=1}^{N} C_i + C_{GD} + C_{GS} + C_{GB}$$

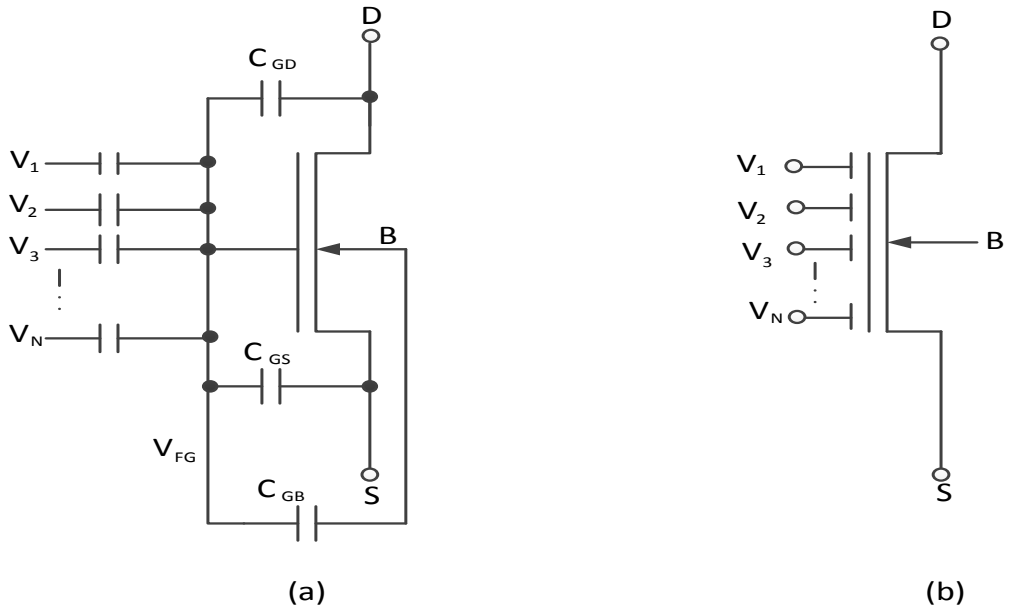

Figure 36. (a) Floating gate (b) circuit symbol

The issue with floating gate is the residual charge that gets trapped on the gate during the manufacturing process. This charge is random in nature and directly has an impact on the threshold voltage. Therefore, it is important to accurately control this charge and several techniques were reported, using ultra-violet (UV) light irradiation, the use of the Fowler-Nordheim tunnelling effect and hot electron injection [63], forcing initial conditions using a switch. The UV method is not a standard procedure and might compromise the reliability of the chip in long run. The second technique requires an extra circuitry and involves high voltages, which are not compatible with low-voltage technologies. The third solution involves quasi-floating-gate operation using switches since the DC voltage at the floating gate is no longer controllable with the input capacitors and their input voltages,

6.1.2 Bulk-driven input stage

A bulk-driven (BD) MOS transistor is a device with five terminals, namely gate, source, drain, bulk and substrate (usually grounded). The bulk terminal is the transistor's local substrate, i.e. n- or p- well. Therefore, only n- or p-type of BD MOS is available in a standard CMOS process. Unlike the conventional gate driven transistors, the input is

applied to the bulk terminal of the transistor while the gate terminal is connected to a suitable bias voltage (normally ground) to turn on the transistor$\left(V_{bias} = V_{SG} \geq |V_T| + V_{SD(sat)}\right)$.

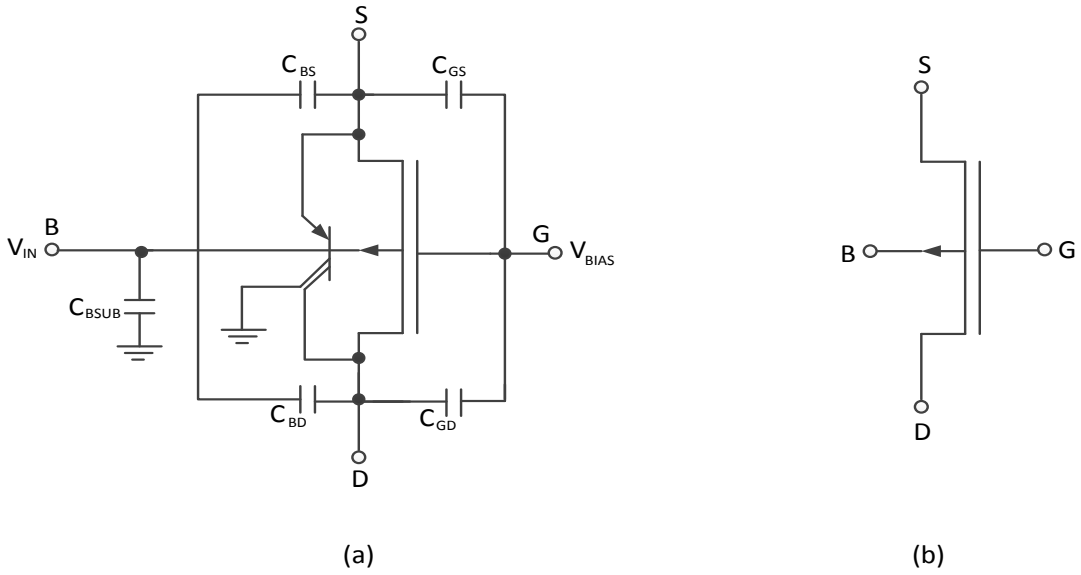

Figure 37. (a) Bulk driven MOSFET (b) circuit symbol of (a)

The drawbacks of a BD MOS transistor compared to a conventional gate-driven MOS transistor of the same size are smaller transconductance because of smaller capacitance of the depletion layer, high input referred noise, lower frequency transition. These drawbacks can be compensated to some extent by resizing the device or increasing the bias current.

6.1.3 Dynamic threshold MOS

The threshold voltage of a MOSFET is one of the most important parameter that influences the operation of MOS transistor apart from the width, the length and the supply voltage. As discussed, the supply voltage of a transistor is scaled at a rate higher than the threshold voltage scaling for a given CMOS technology. Lowering the magnitude of threshold voltage further give rise to more leakage current and may disqualify the device for low-power applications. Dynamic Threshold MOS (DTMOS) is a technique where the gate and the bulk terminal of a transistor are tied together. This proves to have a better sub

threshold slope compared to conventional transistors with almost same leakage current. This technique enables the low power supply voltage operation, it is seen that when the gate voltage increases, DTMOS has larger drain current. This increase in drain current is due to the decrease in the threshold voltage from body effect and the enhanced mobility caused by the decrease field from the shrunk depletion region in the thin film with a positive back gate bias[58].

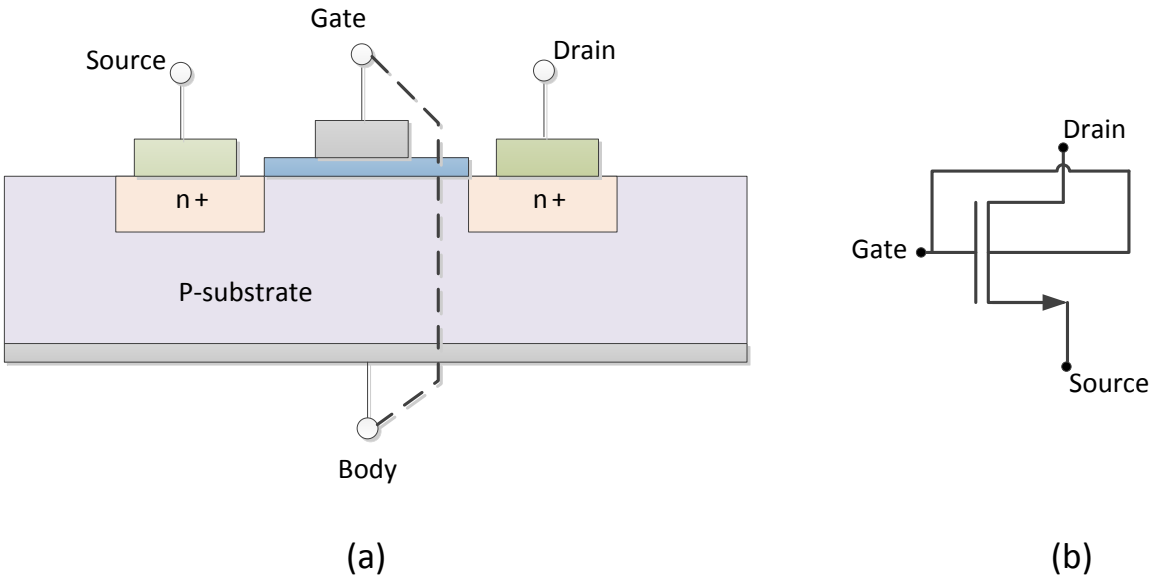

Figure 38. (a) Cross-section view of DTMOS (b) Circuit symbol of (a)

6.2 Dynamic Threshold MOSFET

The low supply voltage CMOS design is a straight-forward method used to achieve low power dissipation. However, with low supply voltages, the voltage across the gate and the source terminal is also low. Therefore, the threshold voltage of the device has to be lowered for low supply voltages, which can be done during fabrication. This process increases the fabrication cost. An efficient way to lower the threshold voltage is by employing innovative circuit design techniques. Amongst the other techniques discussed in section 6.1, DTMOS is proves to be efficient, since the DTMOS technique compared to another body bias technique, has no effect on circuit complexity and the silicon area.

Other body bias techniques involve extra circuitry to generate body bias voltage. The DTMOS transistor is forced to forward bias when the transistor is 'on' and to reverse bias when the transistor is 'off'. In addition, the threshold voltage of DTMOS can be reduced without any technology modifications, which proves to be one of the more efficient solutions to threshold voltage scaling limitations.

6.2.1 Circuit description of DTMOS

The circuit symbol of a DTMOS transistor is shown in Figure39. The gate terminal of a transistor is connected to its substrate (bulk), allowing its threshold voltage to be controlled dynamically. Therefore, in a DTMOS device, the substrate voltage varies along with its gate voltage.

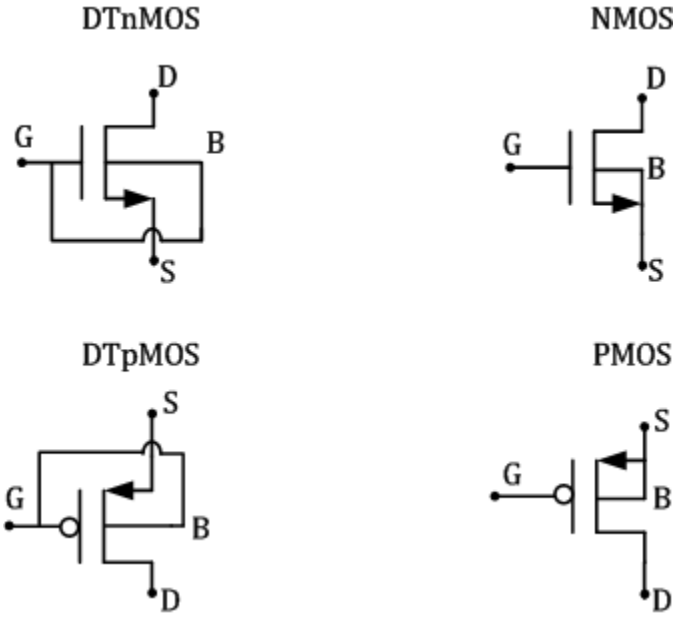

Figure 39.Circuit symbol of MOS and DTMOS

The threshold voltage of the device is given to be [59]

$$|V_{th,p}| = V_{th0,p} + \boldsymbol{\gamma}_p \left(\sqrt{|2\varphi_F| + V_{BS}} - \sqrt{|2\varphi_F|}\right)$$

Where $V_{th0,p}$ is the zero bias threshold voltage, γ_p is the bulk effect factor, φ_F is the Fermi (or) inversion layer potential and V_{BS} is the bulk-to-source junction voltage. The threshold voltage reduction continues until $V_{GS} = V_{BS}$ reaches $2\varphi_F$.

When the input voltage at the gate is high for p-type DTMOS, the device is in the *off* state and therefore has the same threshold voltage, off-current and sub-threshold slope as a normal PMOS transistor. The concept of dynamic threshold is observed when the transistor is in the *on* state; that is, when the input gate voltage is decreased below the source voltage(V_{DD}). When the device turns *on*, the bulk-source junction reduces and the source-substrate junction gets forward biased. There is then an increase of inversion charge and a reduction of body charge, thereby reducing the threshold voltage of the device. This reduction in threshold, caused by an increase of gate capacitance, leads to an increase in the drain-to-source current (I_{DS}) of a DTMOS device, which is considerably higher than a typical MOS transistor as shown in Figure 40. Thus, an area efficient design with high current drive can be obtained by replacing a traditional transistor with a DTMOS transistor. In addition, in this region of operation (sub-threshold), its flicker noise is less than that of a typical MOS transistor.

The drain current expression for a DTMOS transistor in the linear region is given as [62],

$$I_{DS} = \frac{W}{L} C_{ox} \mu_n \left[\left(V_G - V_T(V_{BS}) \right) V_{DS} - \frac{m}{2} V_{DS}^2 \right]$$

In the saturation region,

$$I_{DS} = \frac{W}{L} C_{ox} \mu_n \frac{\left(V_G - V_T(V_{BS}) \right)^2}{m}$$

where

$$m = 1 + \delta$$

$$\delta = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}}\sqrt{\frac{q\varepsilon S_i N_a}{2(2\phi_{fp} - V_{BS})}}$$

$m$is the body effect coefficient, C_{ox} is the gate oxide capacitance per unit area, $\mu_n$is the effective channel mobility, N_a is the uniform channel doping, and W and L are the channel width and length respectively. Since DTMOS is operated by connecting the gate with the bulk terminal, the substrate bias is given as

$$V_{BS} = \alpha\, V_G 0 \;\leq\; \alpha \;\leq 1$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. For an n-type DTMOS device, while $\alpha = 0$ it operates as a normal transistor and for $\alpha > 0$ it operates as a DTMOS transistor.

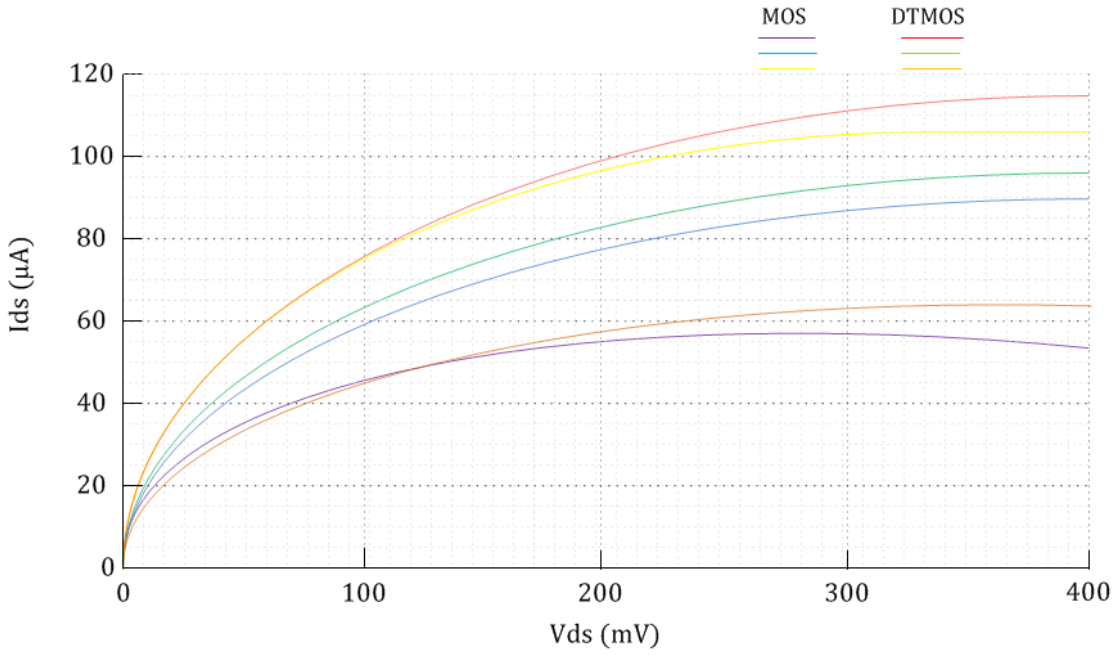

Figure 40.I_{ds} - V_{ds} for MOS and DTMOS varying V_{gs}

6.3 Proposed Switched-capacitor DTMOS integrator

The key feature of using a DTMOS transistor in a CMOS inverter, replacing a conventional MOS transistor is to utilize the body effect and lower the power supply voltage for low voltage applications. The PMOS and the NMOS transistors are replaced with dynamic threshold transistors which are denoted as DTpMOS and DTnMOS respectively. The threshold voltage of these transistors change dynamically based on the input voltage applied at the gate. When the input is 'low', DTpMOS turns 'on' and the threshold voltage drops below 0.4V, due to body effect, DTnMOS remains 'off' with a threshold voltage the same as that of a conventional NMOS transistor. The advantage of using DTMOS transistors is that, during the 'on' state, there is an increase in the transistor's overdrive voltage ($V_{gs} - V_T$). During the 'off' state, the threshold voltage of a DTpMOS transistor rises, decreasing the leakage current. Furthermore, the gate capacitance and current drive of a DTMOS transistor is much higher than a regular MOS transistor, which result in faster switching [59]. A DTMOS transistor can be created without any additional processing steps in a standard CMOS technology.

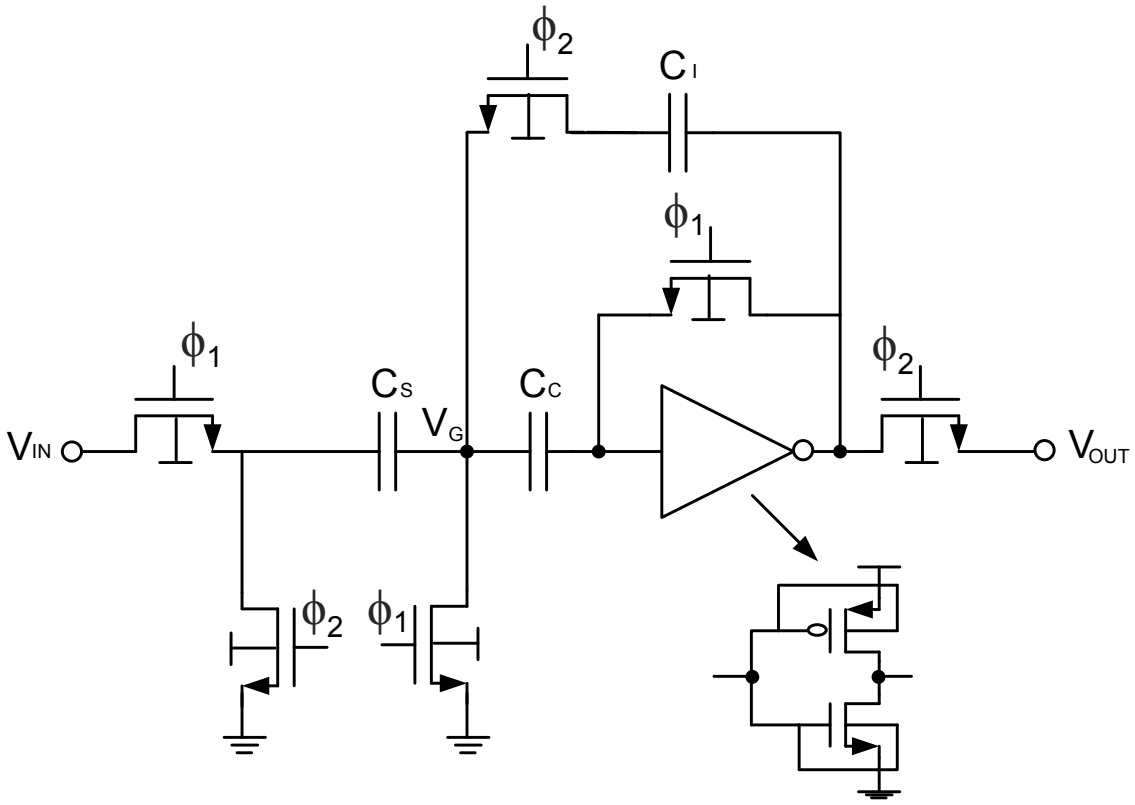

Figure 41.Switched-capacitor DTMOS integrator

The supply voltage of a conventional CMOS inverter has to be chosen so that it is the sum of the threshold voltages of PMOS and NMOS, which is $V_{dd} \leq |V_{thp} + V_{thn}|$ in order to reduce the static power dissipation, which limits the operation for supply voltages under 0.7V due to the threshold limitation. The maximum value of body-source voltage of a DTMOS transistor is about 0.6V, which is limited by its static current. Thus, the static power dissipation increases at a higher voltage due to the inherent parasitic bipolar transistor. However, it can be used at higher supply voltages with an auxiliary transistor [60]. For DC analysis, the voltage transfer characteristics of both the CMOS and DTMOS were identical and both demonstrate very good noise margins and an exponentially high gain. The dynamic power consumption is significantly reduced by using a low power supply voltage.

$$P_{dynamic} = C_L * (V_{DD})^2 * f = 1pf * (0.4)^2 * \left(\frac{1}{10\,s}\right) = 16nW$$

The static leakage current of the device is also reduced because the threshold voltage reaches its maximum value when the transistor is in the 'off' state.

$$P_{static} = I_{leakage} * V_{DD} = 54.6nA * 0.4 = 21.84nW$$

The power consumption of the SC integrator based on the DTMOS inverter is 37.84nW.

6.4 Limitations of DTMOS

It is well known that different body biasing techniques are available in literature; likewise DTMOS can be implemented using appropriate biasing techniques. The speed of the device depends on the biasing scheme. A direct implementation of DTMOS results in a circuit which operates at a higher speed than using auxiliary body biasing circuits. The auxiliary biasing schemes are used where a DTMOS circuit need to operate with a power supply voltage of above 0.6V.

DTMOS has large body capacitance and body resistance. Therefore, it requires significant time to charge the body after the body bias is applied. An increase in width results in an increase in the delay of the circuit. Normally, the delay of a DTMOS inverter is less than that of a conventional CMOS inverter, and the delay of DTMOS is less for very low supply voltage in comparison to MOS transistors, as shown in Figure 42, where the supply voltage was varied from 0.1V – 0.4V.

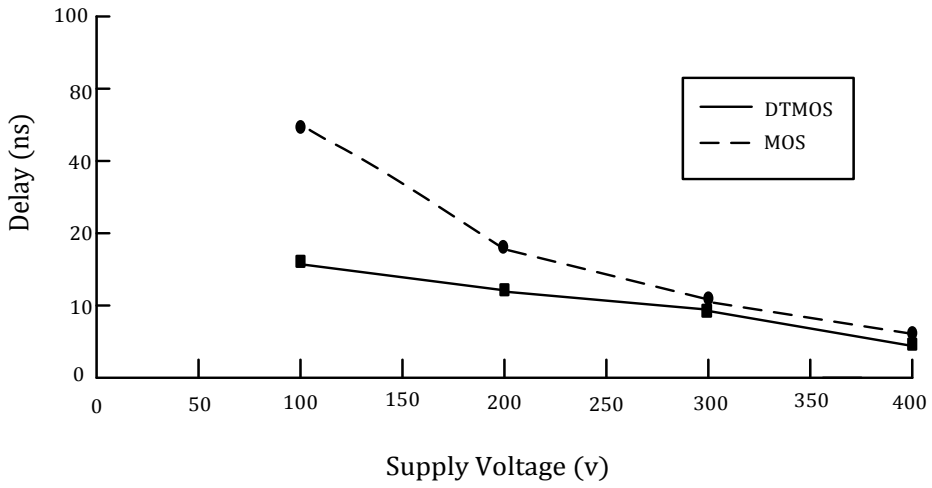

Figure 42.Delay characteristics of MOS and DTMOS inverter

6.5 Filter design using Switched-capacitor DTMOS integrator

The proposed integrator is used in the design to implement an SC filter to demonstrate its suitability in an ultra low-voltage and low-power SC filter design application. Filter design specifications from *Chapter 4* have been used to implement the switched-capacitor filter using SC DTMOS integrator. A Monte Carlo analysis has been done to check the sensitivity of the circuit with respect to the transfer function. The Chebyshev Low pass filter response is shown in Figure 44and its corresponding values are tabulated in Table 10. The SC filter has been designed using 0.4V supply voltage and the power consumption is only 276.41nW. This ultra low power consumption is achieved by utilizing a DTMOS integrator scheme which operates in the sub-threshold region. Low-threshold voltage devices suffer from leakage current during the off-state. DTMOS increases its threshold voltage during the off state, thereby minimizing the power dissipation.

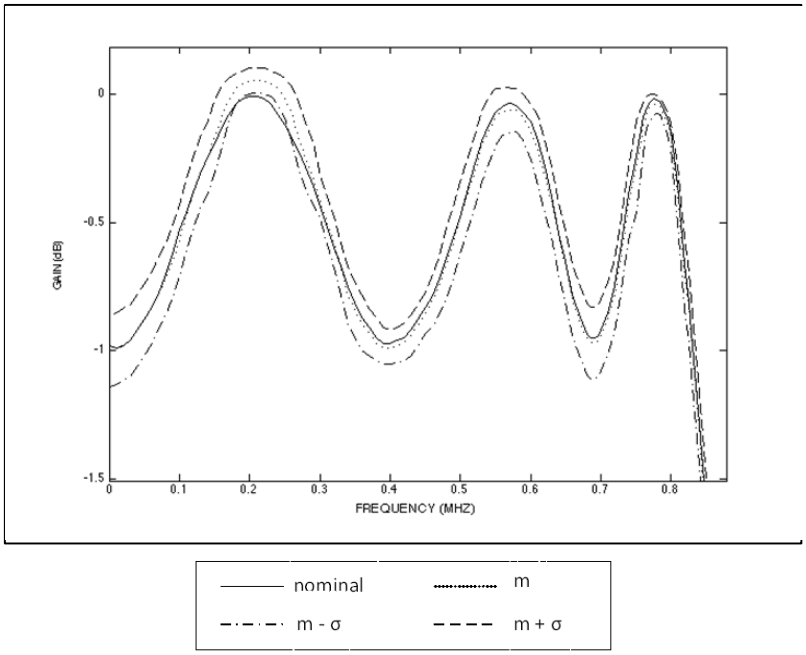

Figure 43. Response of DTMOS integrator based SC filter design (FLF)

Frequency (MHz)	Mean (dB)	Nominal (dB)	Mean + Standard deviation (dB)	Mean – Standard deviation (dB)
0.1	-0.5927	-0.5863	-0.5158	-0.7483
0.3	-0.4561	-0.4471	-0.3619	-0.5118
0.5	-0.4792	-0.4790	-0.3763	-0.7596
0.7	-0.8674	-0.8679	-0.7818	-1.1868
0.8	-0.2428	-0.2485	-0.2363	-0.2528

Table 10. Monte Carlo analysis of DTMOS integrator based SC filter

6.6 Low frequency SC filter design for biomedical application

In biomedical applications such as ECG(0.01-300Hz), EEG(0.1-100Hz), EOG(0.1-10Hz), EMG(50-3000Hz) [64], temperature sensing, and blood pressure for signals are measured in small portable wireless devices, so, low-voltage design is an important factor for extended battery life. The frequency range of the signal is usually very low, which normally ranges from 10 Hz - 3 KHz depending on the application. The SC integrator proposed in this thesis work operates with ultra low-voltage and ultra low power consumption which is best suitable for this kind of applications. Since, the frequency rage is low, and more significantly around 100Hz, to eliminate the noise at higher frequencies we use low pass filter of cut-off frequency around 100Hz. To demonstrate the usefulness of the proposed power efficient SC filter design for biomedical applications, a fourth order Chebyshev low-pass filter design has been realized with a cutoff frequency around 100Hz. The transfer function used in this design is given below,

$$H(Z) = -\frac{0.0494+0.1978Z^{-1}+0.2967Z^{-2}+0.1978Z^{-3}+0.04943Z^{-4}}{1-0.7494Z^{-1}+1.0720Z^{-2}-0.5597Z^{-3}+-0.2337Z^{-4}}$$

$\alpha_0 = -0.0494$		$b_0 = -0.0609$
$\alpha_1 = -0.1978$	$\beta_1 = -0.7497$	$b_1 = -0.1039$
$\alpha_2 = -0.2967$	$\beta_2 = \quad 1.0726$	$b_2 = -0.1737$
$\alpha_3 = -0.1978$	$\beta_3 = -0.5597$	$b_3 = -0.2348$
$\alpha_4 = -0.0494$	$\beta_4 = \quad 0.2337$	$b_4 = -0.0494$

Table 11. Values of α's, β's and b's for FLF implementation

Solving the equations (15) – (19) using the values in Table 11, resulted in capacitor spread around 25pF for a minimum capacitance value of 500fF. The capacitor values obtained with a sampling frequency of 400Hz are C_1 = 12.27pF, C_2 = 11.50pF, C_3 = 10.12pF, C_{31} = 10.85pF, C_{11}= 3.26pF, C_{32} = 11.32pF, C_{12} = 6.59pF, A_2 = 4.13pF, C_2 = 1.75pF, D_2 = 500fF.

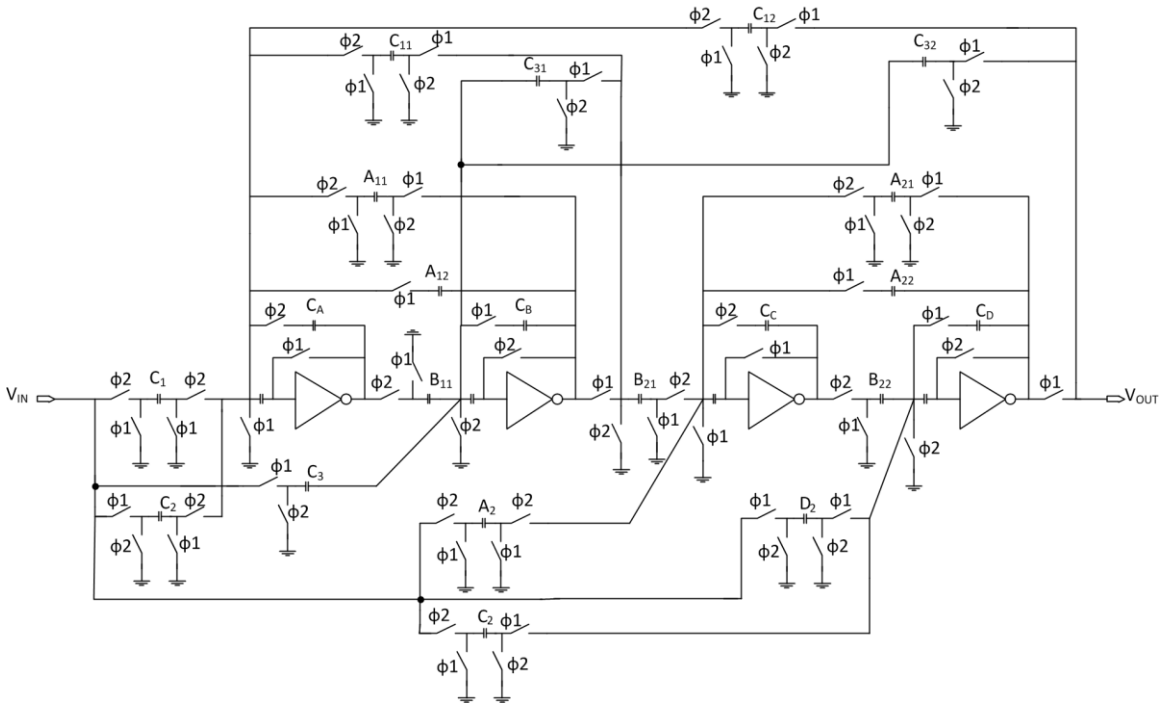

Figure 44. FLF realization of fourth-order Chebyshev low-pass filters design.

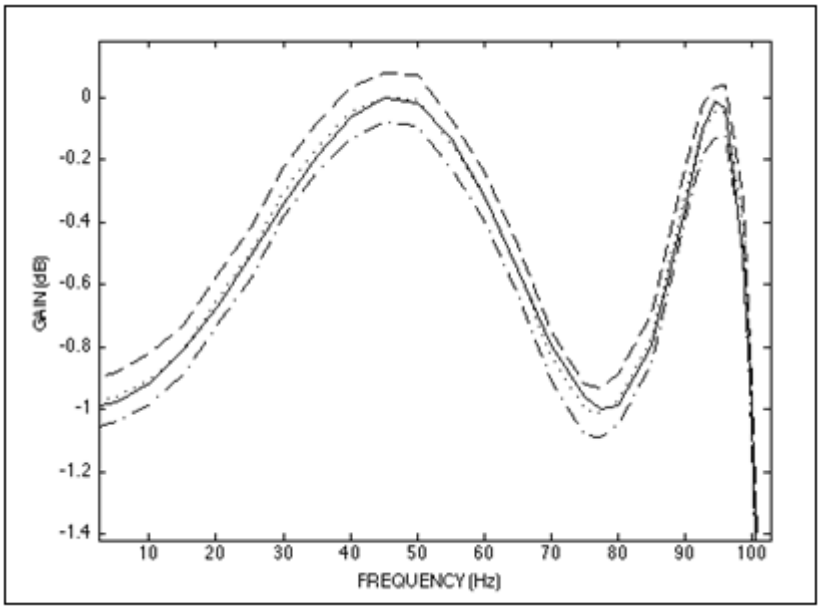

Figure 45. Response of DTMOS inverter-based SC filter for low frequency application

Frequency (Hz)	Nominal (dB)	Mean (dB)	Mean + Standard deviation (dB)	Mean – Standard deviation (dB)
10	-0.9112	-0.8084	-0.8510	-0.9531
20	-0.6691	-0.6521	-0.6110	-0.7692
40	-0.0664	-0.0571	-0.0192	-0.1582
60	-0.3189	-0.3182	-0.2680	-0.3681
80	-0.9873	-0.9670	-0.9174	-1.0170
100	-0.9910	-0.9818	-0.9562	-1.0526

Table 12. Monte Carlo analysis of DTMOS inverter-based SC filter

CHAPTER 7 Conclusions

7.1 Summary of thesis

The initial objective of this thesis was to design an SC filter to operate at low supply voltage. As the op-amp in an SC filter consume most power, a power-efficient circuit should be employed. Moreover, it has become more and more challenging to achieve the design requirements on dynamic range, speed, noise, and power efficiency at lower supply voltages using the traditional op-amp designs. In this work, an op-amp in an SC filter was replaced with a CMOS inverter-based design to enable the circuit to operate with low supply voltage and with better performance.

Detailed operation of CMOS inverter-based integrator in different operating regions has been analysed and an optimized inverter-based SC integrator design was presented to operate with 0.7V. The supply voltage of the CMOS inverter is as low as the sum of the threshold voltage of PMOS and NMOS |-0.360|V and 0.353V (hence, V_{dd} = 0.7V) respectively in the TSMC65nm technology. The designed integrator is superior in many aspects compared to an op-amp at lower supply voltage. The inverter-based integrator has a faster settling time of 20ns and high slew rate of 2.5 V/μs with only 129.5nW power consumption. The input-referred noise is 6.1nV/sqrt(Hz) at 1KHz for $V_{in\ p\text{-}p}$ = 100mV. The usefulness of a CMOS inverter-based integrator in an SC filter application is presented by designing a sixth-order Chebyshev LP filter which can operate at lower supply voltage compared to the conventional filter designs using op-amp and comparator.

Firstly, a Chebyshev filter using cascade topology was implemented using CMOS inverter-based integrator, the design was more sensitive to transfer function variation. Hence, a Chebyshev filter design using FLF architecture was realized using inverter-based integrator which showed to be less sensitive to transfer function variation by performing Monte Carlo analysis in Cadence. A sixth-order Chebyshev filter was designed with a pass band frequency of 840KHz driven by 3MHz clock signal with an attenuation of 40dB in

the stop band. The power consumption of the designed sixth-order filter was only about 1.8μW which is nearly 100 times lower than conventional designs [8] [9].

It is very clear that the continuing technology scaling will result in supply voltage lower than 0.7V. Hence, we have to come up with a design which can operate with a supply voltage lower than 0.7Vwithout sacrificing the performance parameters. Therefore, a new type of SC integrator was proposed using DTMOS transistors which have the capability to operate at supply voltage lower than the threshold voltage of the conventional MOS transistor. The proposed technique does not suffer from leakage current problems that the other body biased techniques experience at lower supply voltage, because the threshold voltage of the DTMOS device is lowered when the transistor turn *on*, high current drive is achieved and the threshold voltage level reaches its maximum value when the device turn *off*, which minimizes the leakage current. The proposed DTMOS integrator based SC filter has the same performance as that of a CMOS inverter based SC filter with ultra low power consumption of only 276.41nW with an operating voltage of 0.4V. The designed DTMOS inverter-based SC filter prove to be one of the power efficient methods to design SC filters in ultra low supply voltage scenarios and can be used in the field of biomedical application where battery operated devices demand for circuit designs with ultra low power consumption.

This work titled “Ultra Low-voltage Multi-loop Feedback Switched-capacitor Filters”, has been submitted to *International Journal of Electronics and Electrical Engineering* (*IJEEE)* for publication.

7.2 Performance comparison table

	[This work] DTMOS 2014	[This work] CMOS 2014	[7] 2013	[10] 2013	[12] 2010	[15] 2004
Process	65nm	65nm	180nm	65nm	180nm	180nm
Voltage	0.4V	0.7V	1.8V	1.2V	1.8V	1.8V
Order	6	6	4	3	N/A	N/A
Clock	3MHz	3MHz	100KHz	N/A	80MHz	2.5MHz
Pass-band	820KHz	840KHz	20KHz	50MHz	8.72MHz	0.5MHz
Ripple	0.97dB	1dB	0.5dB	N/A	<2dB	1dB
Attenuation	38dB	40dB	40dB	30dB	40dB	60dB
Power	276.41nW	1.8uW	208uW	1.56mW	44.2mW	0.85mW

Table 13. Performance comparison table for the proposed design

7.3 Scope for future work

Utilizing DTMOS inverter to design SC filters, it is possible to achieve high frequency operation at ultra-low supply voltage and the simplicity in the design promotes its application in portable devices. The proposed DTMOS amplifier can also be used in mixed-signal CMOS circuits such as ADCs and DACs.

The designed filter is sensitive to component variation compared to an op-amp based design. The filter design was implemented using a simple DTMOS inverter architecture. The DC gain of the proposed DTMOS inverter is around 43dB, which is considered to be less for certain applications that require a gain of 60dB or higher. Thus, utilizing different inverter architecture such as current-starved inverter or a cascade inverter might result in a design with low sensitivity, higher DC gain and a better PSRR. As mentioned earlier, better performance characteristics can be obtained at the cost of increased power consumption.

An additional switch can be introduced to the DTMOS inverter-based integrator circuit to further reduce the power consumption of the device during the steady-state operation. As shown in Figure 45, adding an extra switch to disable the device once the offset value is stored in the Cc, will reduce the static power consumption of the device: since, we do not require the DTMOS inverter to be *on* during the entire sampling period.

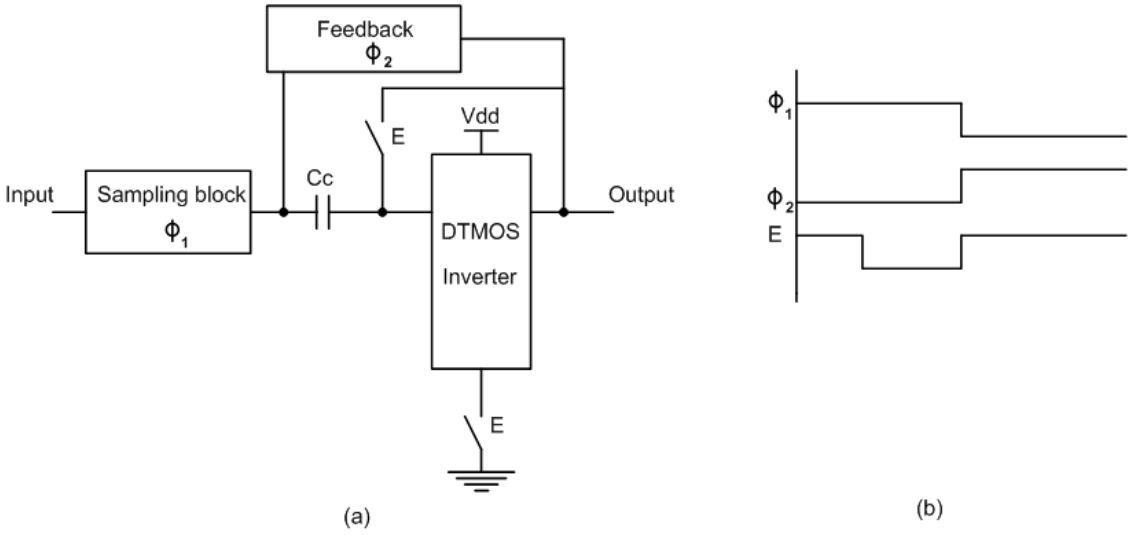

Figure 46. (a) DTMOS integrator using power-down switch (b) Clock diagram

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PVT variation is one of the factors which has to be considered for ultra low power, high-performance sub-threshold circuits. Process corner can be performed to verify the robustness of the design and further modifications can be done if needed.

The leakage current of a DTMOS device is same as that of a CMOS device; further research can be done to reduce leakage current issue by using different body biasing techniques which also improves the power efficiency.

Even though a DTMOS transistor has better delay characteristics and high current drive compared to a CMOS transistor at low voltages, increasing the width of a DTMOS transistor will increase the delay of the circuit. Further research can be done to compensate for the increase in delay.

APPENDIX

The data required to simulate the circuits discussed in this thesis is given in this section. Simulations were done using the Cadence tool with the TSMC65nm technology.

I. CMOS inverter input data

Input voltage (Vin) :50mV

Supply voltage (V_{DD}) : 0.7V

Input frequency (f_{in}) : 1MHz

Input sampling capacitor (Cs) : 250f

Threshold voltage of N-type transistor ($V_{th(n)}$) : 0.353V

Threshold voltage of P-type transistor ($V_{th(p)}$) : |-0.360| V

In Cadence, a switched-capacitor circuit cannot be simulated using direct method like the other CMOS circuit designs. Hence, PSS has to be performed prior to AC analysis to obtain the frequency response of any circuit.

II. Periodic Steady State Analysis

Analysis type : PSS

Engine : Shooting

Beat Frequency : Auto calculate

Output Harmonics (Number of Harmonics) : 10

Accuracy Defaults (errpreset) : Moderate

Additional Time for stabilization (tstab) : 10µs

III. Periodic AC Analysis

Sweeptype : relative

Relative Harmonics : 0

Input Frequency Sweep range (Hz)

Start : 10

Stop : 1 M

Sweep Type : Automatic

Maximum sidebands : 5

Specialized analysis : None

IV. Direct plot form

Plotting Mode : Append

Analysis : PAC

Function : Voltage

Select : Net

Sweep :Sideband

Signal level : Peak

Modifier : dB20

Output sideband : 0 10 – 1MHz

V. DTMOS inverter input data

Input voltage (Vin) :25mV

Supply voltage (V_{DD}) : 0.4V

Input frequency (f_{in}) : 1MHz

Input sampling capacitor (Cs) : 250f

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