TRANSIT AND DC MODEL OF FLOATING GATE TRANSISTOR IN 90NM CMOS TECHNOLOGY

by

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Signature of Author

To my husband

Hani and my beloved children Sara and Anas

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ABSTRACT

This thesis presents a new simulation model for floating gate transistor (FGMOS) in nanometer scale technology where the transistors suffer from non-negligible gate leakage current due to the very thin Silicon oxide (SiO_2) layer. The new FGMOS simulation model is used for transient and DC simulation and with any industry standard simulators such as Spector and various SPICE programs (i.e. HSPICE, WinSPICE, etc.). This model can be used for any technology that has SiO_2 thickness less than 3nm and suffer from gate leakage current with no changes to the model itself; however, minimal changes need to be done to the gate tunnelling cell to comply with the technology parameters where the gate tunnelling current exponentially increases as tox decreases.

LIST OF ABBREVIATIONS USED

FG	Floating Gate
DT	Direct Tunneling
IC	Integrated Circuit
CMOS	Complementary-Metal-Oxide-Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
V_{THFG}	Floating gate Threshold Voltage
SiO_2	Silicon Oxide
FGMOS	Floating Gate Metal Oxide Semiconductor
t_{ox}	Silicon Oxide thickness
AHDL	Analog Hardware design Language
EPROM	Erasable Programmable Read Only Memory
FPGA)	Field Programmable Analog Array
ECB	Electron Conduction band
EVB	Electron Valence Band
HVB	Hole Valence Band

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CHAPTER 1 INTRODUCTION

This chapter presents an introduction about floating gate transistor and discus the motivation behind this research and the objectives.

2.1 Motivation

The floating gate transistor (FG) is very similar to standard Metal Oxide Semiconductor Field Effect Transistor (MOSFET), but it differs by having no DC path to ground with double poly layers at the gate where multiple inputs are capacitively connected and that makes the gate is electrically floating.

The ability to tune the threshold voltage of FG transistor (V_{THFG}) reduces the headroom supply voltage and gives it the advantages of low voltage circuits. Having a multiple inputs at the FG transistor is one of the important advantages that provide the ability to do summation, subtraction, multiplication and tune the $V_{THFG.}$

In the last ten years, analog designers start to use FG transistor (FGMOS) in low voltage, low power circuits and in computational designs due to their features of having multiple inputs at the gate and threshold voltage programmability.

Due to the structure of FGMOS where there is no DC path to ground, a simulation model is needed in order for the simulator to converge to the correct result.

As the Complementary-Metal-Oxide-Semiconductor (CMOS) technology scaling down, Silicon Oxide (SiO_2) thickness became very thin (few nanometers). When SiO_2 is less than 3nm, gate direct tunneling (DT) leakage current becomes a dominant problem that can increase the power dissipation and degrade the CMOS performance.

In ultra-thin CMOS technologies, the carriers (electrons or holes) are able to tunnel through the oxide to the channel and the bulk. DT current increases exponentially as SiO_2 thickness (t_{ox}) reduced and gate voltage increased.

The available simulation models for FGMOS for analog circuits design in the literature did not account for gate leakage current impact on FGMOS behavior; furthermore, there is no accurate measurement for FGMOS for analog applications implemented in sub 100nm technology.

2.2 Objective

FGMOS simulation models available in the literature work reasonably well in the micro-meter scale. CMOS technology, however, they are not suitable for nano-meter scale technology due to the leakage current effect.

The objective of this research is to develop a simulation model for FG transistor in nanometer (sub 100nm) technologies where the gate leakage current has been taken into account.

In order to achieve that, a FG experimental chip has been fabricated using TSMC 90nm process and tested. As a result, accurate measurements for FGMOS performance have been obtained. The gate leakage current is studied and parameters from BSIM4 model have been incorporated in the proposed simulation model.

The new FGMOS simulation model is used for transient and DC simulation. A standard MOSFET and behavioural modelling using Verilog-A have been used in the development of the proposed model. This model can be used for any industry standard simulators such as Spector Cadence and various SPICE programs (i.e. HSPICE, WinSPICE, etc.).

The proposed model accounts for two important characteristics of FG transistor:

- DC characteristics
- Direct tunneling gate leakage current.

The proposed model is based on the testing measurements conducted during this research work and analytical analysis and calculations that take into account the impact of DT gate leakage current on FGMOS behavior. Having an accurate model for FG transistor in nanometer technologies will help the analog designers to simulate and test FG transistors in circuits and expect accurate results before fabrication.

2.3 Organization

This thesis is organized as follows:

Chapter 2, describes FG transistor DC characteristics, design issues and reviews previous works for modeling FGMOSFET and gate leakage current.

Chapter 3, examines the limitation of available FGMOS model through case study of FG operational amplifier, simulation results are included.

Chapters 4, discuss the fabrication of FGMOSFET in nanometer technology (sub 100nm) and the layout design of an experimental chip. The testing setup and equipment used are included also, the methodology to conduct FG measurement are explained.

Chapters 5, focus on the testing measurements and the developed analytical equations. A new simulation model is proposed for the FGMOS transistor in nanometer technology with simulations results. Furthermore, simulation results of FG current mirror using the proposed model were presented.

Chapter 6, conclusion and considerations for future work are suggested.

CHAPTER 2 FLOATING GATE TRANSISTOR

The background of floating gate transistor, characteristics and its fabrication are introduced. Design issues with FGMOS in sub 100nm technologies are discussed where the gate leakage current has a pronounced effect on the transistor's performance. Some previous models of FGMOS and gate leakage current are also reviewed.

2.1 FGMOS history

Since the FG transistor has been introduced for the first time in 1967, it has been widely used in EPROMs, EEPROMs, and flash memories due to its ability to store charges for long time. Furthermore, these charges can be controlled by:

(a) Using an ultra violet (UV) lights projected at the chip.
(b) By adding a high voltage across the gate capacitor to tunnel electrons through the oxide.
(c) By adding electrons using hot-electron injection [1].

In the last ten years, the usage of FGMOS did not stop at digital memories but it is extended to include analog design [2]. As a result of V_{THFG} tunability FGMOS has been used to design analog circuits that can be operated at much lower power supply than the one with standard MOS (for same technology). Also, the designers made

advantage from the sum operation at the gate to design circuits like multipliers, integrators and amplifiers [3-5].

2.2 Device characteristics

A FGMOS is very similar to standard MOS transistor but it differs in a way that it has no resistive connections to its gate and numbers of inputs are deposited above the FG and these inputs are only capacitively connected to the FG.

FGMOS usually fabricated using double poly structure where the first poly is the FG gate and the second poly is the control gate where all the inputs are deposited as shown in Figures 1 and 2.

With no DC path to ground at the gate and having multiple input (where each voltage is coupled to the FG through an input capacitor) has resulted into several changes in the DC characteristics from the standard MOSFET.

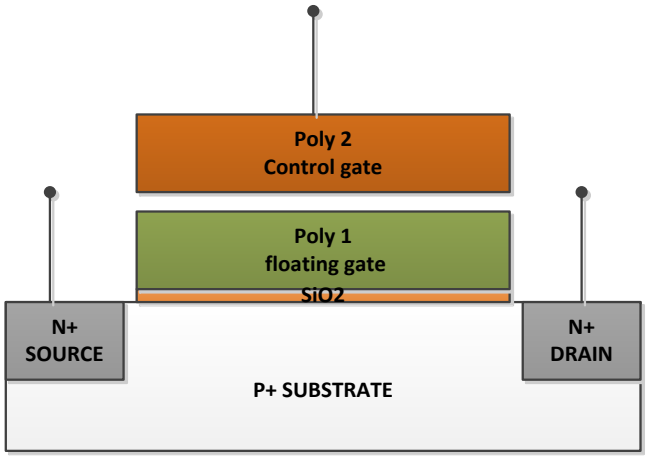


Figure 1: N-type FGMOS using double poly structure

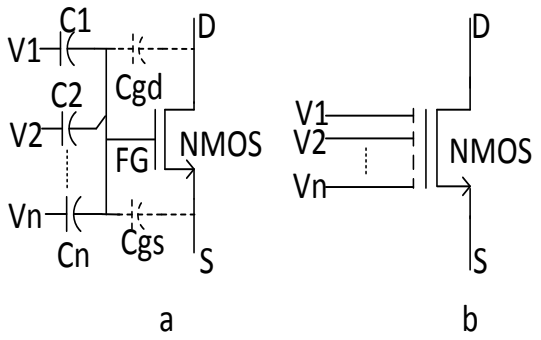


Figure 2: n-inputs FGMOSFET: a: equivalent circuit, b: the symbolic representation

Due to the nature of FGMOS, the gate is electrically isolated and no DC path to ground, a charge can be stored in the FG and this charge directly affects the drain current and the threshold voltage. This feature helps to use FGMOS in analog memories like Field Programmable Analogue Array (FPAA) [6].

The FG voltage is the weighted sum of all the coupled inputs voltages connected at the gate, by assuming that the gate is surrounded by very strong insulator (SiO_2) and there is no leakage current [7], the FG voltage is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{Q_{FG}}{C_T} \tag{2.1}$$

$$\boldsymbol{C_T = \sum_{i=1}^{N} C_i + C_{gs} + C_{gd}} \tag{2.2}$$

By assuming zero charge accumulated at the gate, Eq. (2.1) can be re-written as:

$$V_{FG} = \frac{C_1}{C_T} V_1 + \frac{C_2}{C_T} V_2 + \frac{C_3}{C_T} V_3 + \cdots + \frac{C_n}{C_T} V_n \tag{2.3}$$

From Eq. (2.3) FGMOS can be used to reduce the complexity in certain circuits that require adders and decrease the power dissipation and noise in such circuits [8] as shown in Figure 3.

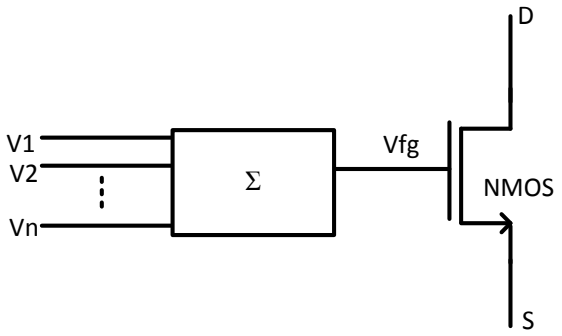


Figure 3: equivalent circuit for floating gate transistor [8]

For FGMOS working in saturation region, the current equations can be written as:

$$I_D = \mu_N C_{OX} \frac{W}{2L} (V_{FG} - V_T)^2 \quad (2.4)$$

By assume zero Q_{fg} and replacing V_{FG} in Eq. (2.1) will result in

$$I_D = \mu_N . C_{OX} . \frac{W}{2L} (\sum_{i=1}^{N} \frac{C_i}{C_T} V_i - V_T)^2 \quad (2.5)$$

$$I_D = \mu_N . C_{OX} . \frac{W}{2L} . \beta (\sum_{i=1}^{N} V_i - \left(\frac{C_T}{C_i}\right) V_T)^2 \quad (2.6)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L} \beta (\sum_{i=1}^{N} V_i - V_{THFG})^2 \quad (2.7)$$

Where: $\beta = \sum_{i=1}^{N} \left(\frac{C_i}{C_T}\right)^2$ and $V_{THFG} = \sum_{i=1}^{N} \left(\frac{C_T}{C_i}\right) V_T$

From these equations, the drain current in multiple input FGMOSFET is a function of the capacitor ratio of the effective input voltage to the total capacitances seen at the gate.

Let's assume that V_1 is the effective input, then, the drain current can be written as :

$$I_D = \mu_N . C_{OX} . \frac{W}{2L} . \beta . \left(V_1 - \left(\frac{C_T}{C_1} V_T - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n \right) \right)^2 \quad (2.8)$$

In this case, $\beta = \left(\frac{C_1}{C_T}\right)^2$

$$V_{THFG} = \frac{C_T}{C_1} V_T - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n \quad (2.9)$$

$$I_D = \mu_N . C_{OX} \frac{W}{2L} . \beta \left(V_1 - V_{THFG} \right)^2 \quad (2.10)$$

$$gm_i = \frac{C_i}{C_T} \quad \text{Where i=1, 2, N} \quad (2.11)$$

Where μ is the mobility, C_{OX} is the oxide capacitance per unit area, W is the channel width, L is the channel length, V_{FG} is the floating gate voltage, N is the number of inputs voltages at the gate, C_i are the input capacitors connected at the gate, Vi are input voltages, C_{gs} *and* C_{gd} are the parasitic capacitors, Q_{FG} refers to the charges trapped in FG through fabrication and V_T is the threshold of standard MOS threshold

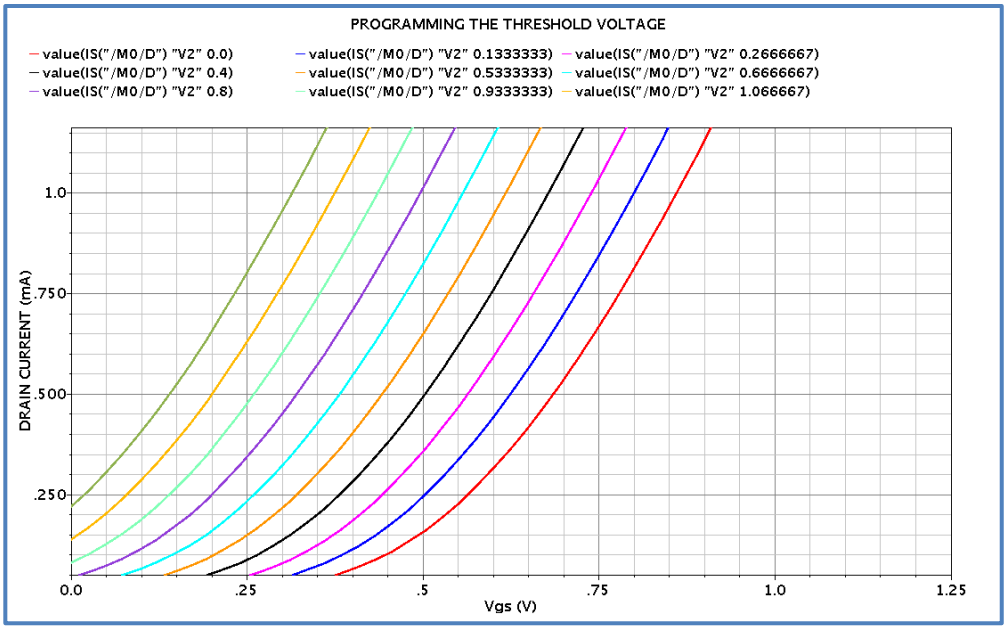
voltage and V_{THFG} is the threshold voltage of FGMOSFET , gm is the FGMOS transconductance .

Eq. (2.10) shows that FGMOSFET behaves as a programmable threshold voltage device where the effective threshold voltage V_{THFG} can be reduced to zero or to a negative value compared to standard MOS threshold. Figure 4 illustrate the tuning capability of the FG transistor with two inputs voltages by increasing one of the input voltages and sweeping the other.

The V_{THFG} can be reduced further by increasing the numbers of the multiple inputs at the gate or the input capacitors ratio. This is the most important advantage that made FG technique ideal for low voltage applications and tunable circuit that need to compensate for mismatch.

As we can see in Eq. (2.10) and (2.11), the drain current I_D and the transconductance in FGMOS is smaller than standard MOSFET due to the scaling factor β which is a function of the coupling capacitors ratio for the effective input seen at the gate as shown in Figure 5.

These are drawbacks of FGMOS transistor however, analogue designers were able to overcome them and use this transistor in different circuits.



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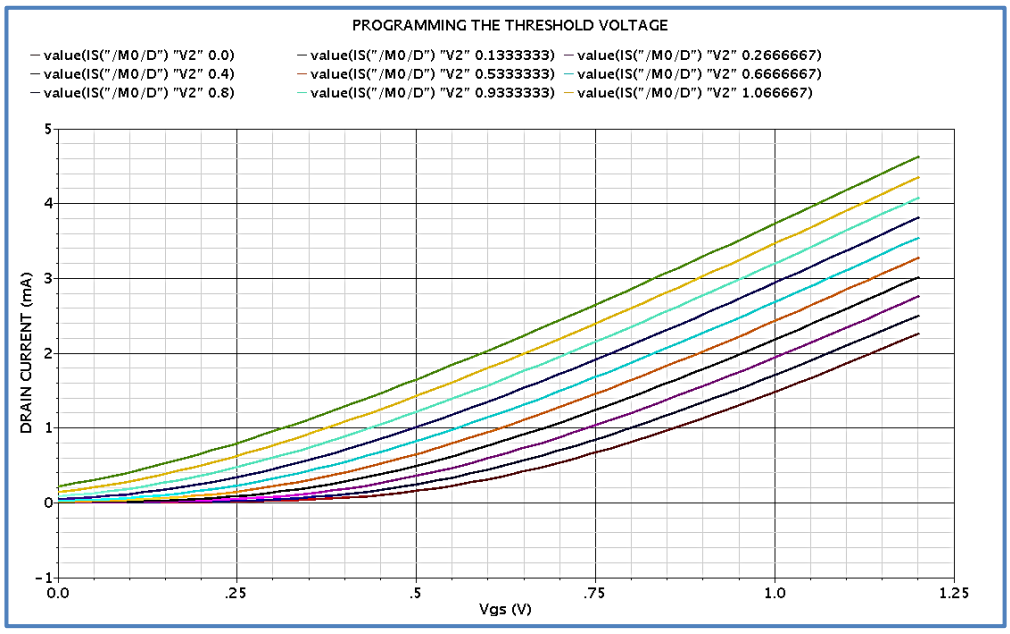


B

Figure 4: FGMOS threshold voltage programmability by changing one of the input voltages, a: zoom in , b: zoom out

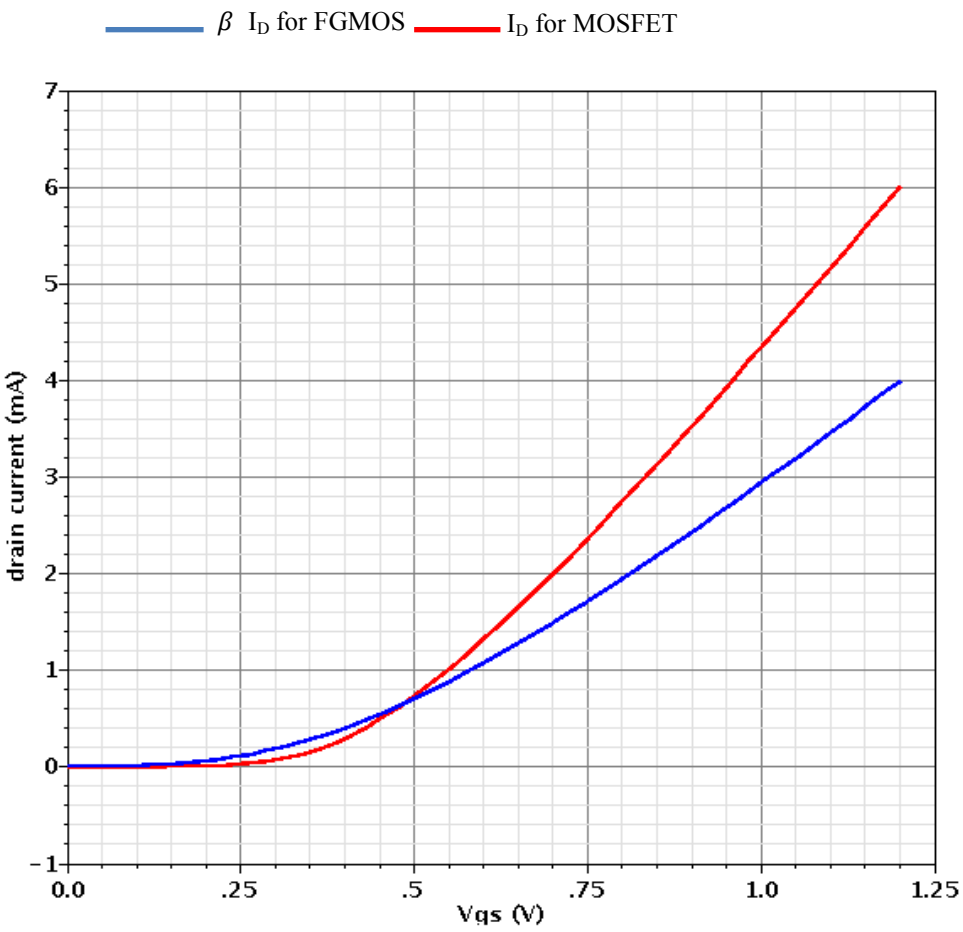


Figure 5: A comparison between standard MOS and FGMOS drain currents

2.3 Charge Accumulation

Due to the oxide that surrounding the silicon at the gate of the FGMOS therefore charges could be accumulated in FGMOS through fabrication and these charges directly affected the threshold voltage of FGMOS and it is indeterminate. The accumulated charges have different effects on different analog circuits, however they had to be eliminated in order the FGMOS can work properly.

Different solutions have been reported in the literature including FGMOS exposure to UV light to get rid of the charges accumulated at the gate [9] but this process is not compatible with CMOS technology and in order to activate light transition, the passivation layer had to be removed.

Another suggested a Fowler–Nordheim tunnelling (FN) current to remove the charges from the FG [10] . The silicon oxide is the insulator that held the electrons and this oxide works as a barrier and electron need high energy to cross through it, therefore, a high voltage applied in order the trapped electrons tunnel through the barrier to the silicon beneath it. The applied voltage is inversely proportional to the oxide thickness so, unless the oxide is very thin, a very high voltage will be needed.

Hot electron injection is another process suggested to deal with the charge in FG where the electrons are added to the FG by applying a high electric field to the gate – drain junction causing the electron to cross the barrier of the oxide to gate and be held there. Hot electron injection can be generated with smaller voltages but it will need extra circuit to control the process [6].

In [11] , a technique was suggested to eliminate that charges from the FG by adding dummy contacts at the gate. This technique is very simple and it does not need extra circuitry and it has been used widely in FGMOS analog circuits.

2.4 Challenges of using FGMOS in nanometer technologies

There are problems facing the analog designers when they use FGMOS in nanometers technology. The first problem is the direct tunneling gate current that occurs in sub 100nm technologies where the silicon oxide is very thin and causing the electrons and holes to tunnel through it. This leakage current will degrade the transistor performance generally and FGMOS specifically. The second problem related to the nature of FGMOS and the need of a model it in order to carry on a simulation in any industry simulator due to the convergence problem.

In the following sections previous simulation models for FGMOS and the gate leakage current will be discussed.

2.4.1 Gate direct tunneling in sub 100nm technologies

The CMOS technology has scaled down dramatically in last decade to meet the industry demand. In fact this scaling improved the CMOS technology by reduce the power dissipation increased the speed and made the fabrication cheaper, however, the reduction of transistor size result into many challenges to predict the transistor performance when the transistor shrinks down.

In the last ten years, the continuous scaling in CMOS technology has led to dramatic reduction in the silicon oxide thickness to few nanometers. Due to the very thin silicon oxide at the gate, direct tunneling (DT) current become a growing issue for analog designers. Gate DT current results from the tunneling of carriers (electrons and holes) from the gate through the oxide to the bulk and source / drain region; respectively.

As presented in Figure 6, DT mechanism in NMOS transistor is determined by the tunneling of carriers from three bands, the first is determined by tunneling the electrons of the conductions band (ECB) in the gate. The second tunneling is from electrons in the valence band (EVB). Third is the tunneling of the holes through the valence band to the gate (HVB). In NMOS device direct tunneling is dominated by ECB and EVB while in PMOS by HVB.

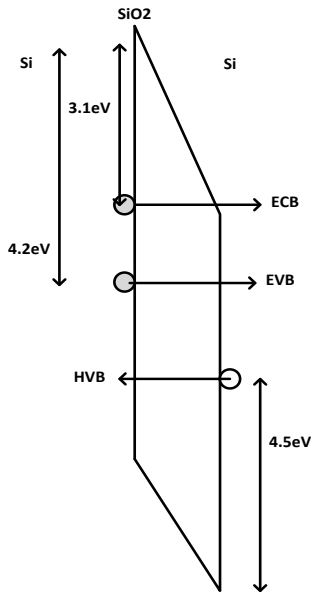


Figure 6: the mechanism of gate tunneling current in CMOS transistor

As illustrated in Figure 7, the gate DT current has three components: the current between gate and substrate (I_{gb}) and the channel current (I_{gc}) where it is divided into two currents between the gate and the source (I_{gcs}) and between the gate and the drain (I_{gcd}); respectively. The total gate current due to the tunnelling can be written as.

$$I_G = I_{gcs} + I_{gcd} + I_{gs} + I_{gd} + I_{gb} \quad (2.12)$$

Igs and Igd are strong function of the terminals gate -source and gate- drain voltages; respectively.

The electrons in NMOS need less energy to cross the barrier than the holes in PMOS therefore, DT gate current for a PMOS device is one order of magnitude smaller than in NMOS device with same value of tox and power supply [12] .

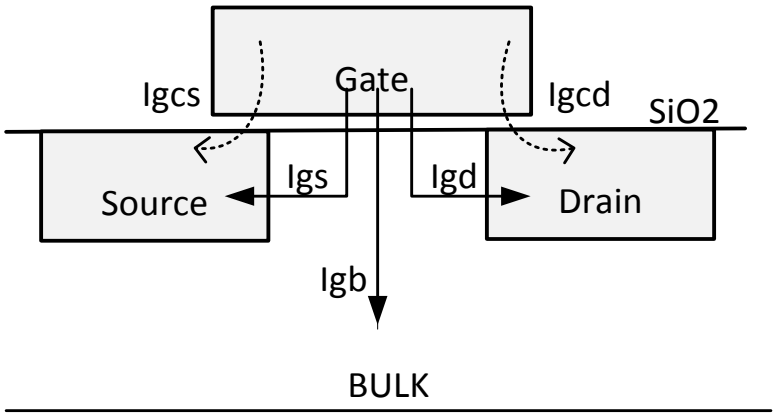


Figure 7: DT gate current components for NMOS in BISM4 [13]

2.4.2 Previous modeling of gate tunneling current in NMOS

DT current degrades the circuit's performance and increases the static power dissipation. Many researchers have been studying the DT and reporting on modeling gate tunneling for circuit simulation [12, 14, 15] .

DT gate current is a strong exponential function of tox and the potential across it with respect to the transistor dimensions. Hence DT increases exponentially as tox decrease and when the gate voltage increase [12] as shown:

$$I_{gs} = \frac{127.04 \times L_{eff} \times e^{(5.606.25 \times V_{gs} - 10.6 \times t_{ox}^{-2.5})}}{2} \quad (2.13)$$

$$I_{gd} = \frac{127.04 \times L_{eff} \times e^{(5.606.25 \times V_{gd} - 10.6 \times t_{ox}^{-2.5})}}{2} \quad (2.14)$$

Where tox and L_{eff} in nanometer

In [12], an empirical gate leakage model was incorporated in 100nm BSIM3v3 (level 49) and was suggested for circuit simulation where the DT gate leakage adjusted to fit 0.13um technology. In the model, the gate to source (Igs) and gate to drain (Igd) currents were described using voltage dependent current sources (VCCS) between gate to source and gate to drain were used as shown in Figure 8.

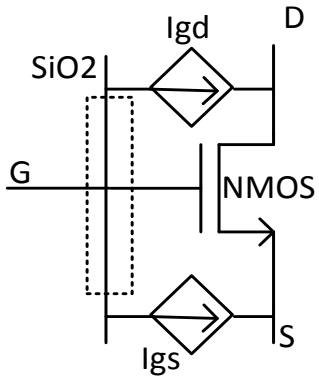


Figure 8 : DT gate current micro model proposed in [12]

In [14] a model was suggested for circuit simulation as illustrated in Figure 9 including the transistor three terminals with the parasitic capacitors Cgs, Cgd and Cgb with the gate tunneling. The gate current in the model partitioned to Igs, Igd and Ich and they were described by VCCS.

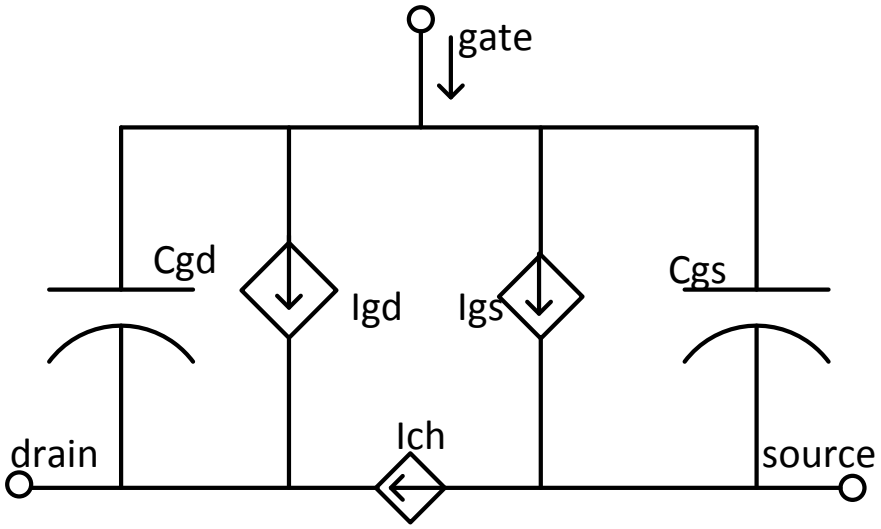


Figure 9 : micro model for gate tunneling for circuit simulation proposed in [14]

In [15] a micro model for the gate DT leakage current was proposed using voltage dependent current sources as a function of the terminal voltages and the partitioning of the channel current to Igs and Igd was represented using variable resistors as presented in Figure 10.

$$I_{gc} = I_{gs} + I_{gd} \tag{2.15}$$

$$R_{cd} = \frac{V_{cd}}{I_{cd}} \ , \ R_{cs} = \frac{V_{cs}}{I_{cs}} \tag{2.16}$$

Where: I_{cs} and I_{cd} obtained from BSIM3 parameters to fit the I-V curve from the simulation.

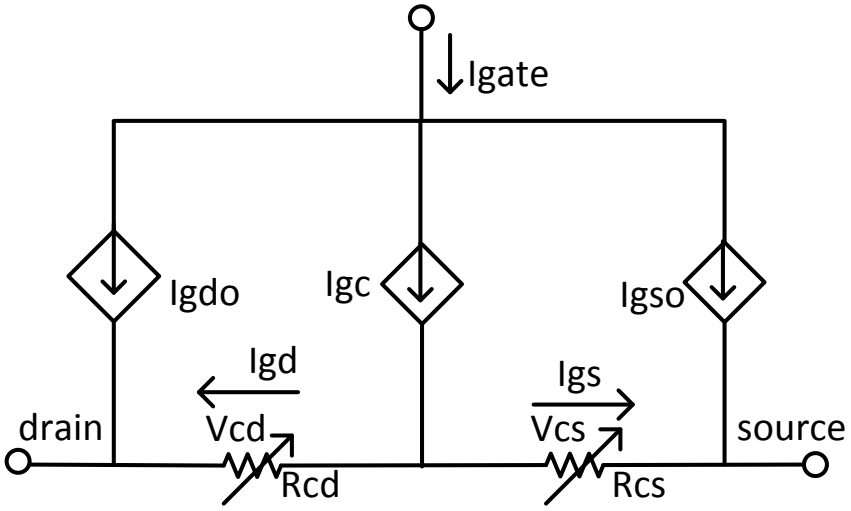


Figure 10 : gate DT model for circuit simulation suggested in [15]

2.4.3 FGMOS Simulation models

SPICE simulator needs at least one path to ground or an initial condition in each point in the circuit in order the simulator converges to a solution. Due to the nature of FGMOS there is no DC path to ground and the coupling capacitors, a DC model is needed to simulate it.

Previously, some models were suggested to solve the convergence problem. In [7] a simulation model was suggested for FGMOS by using a standard MOSFET with multiple inputs capacitively coupled to FG with a large resistor and dependant voltage source (VCVS) to provide a DC path to ground. In such a way the gain of the VCVS is equal to the coupling capacitors ratio seen at the gate for each inputs (Ci/C_T) as illustrated in figure 11.

This model is very simple to implement and has been used widely for simulating FG circuits for analog applications. The major limitation is the inability to represent the charge movement from gate leakage.

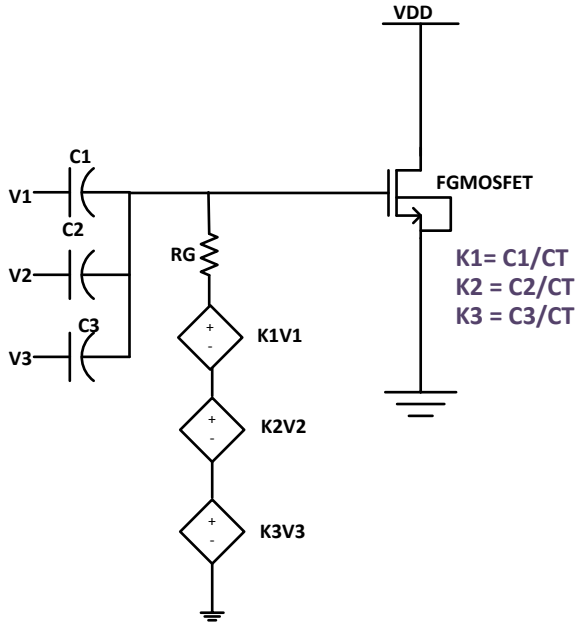


Figure 11: multiple inputs FGMOS simulation model proposed in [7]

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{gs}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T} \tag{2.17}$$

Where R_G in MΩ

$$C_T = \sum_{i=1}^{N} C_i + C_{gs} + C_{gd} \tag{2.18}$$

$$K_i = \sum_{i=1}^{N} \frac{C_i}{C_T} \tag{2.19}$$

As seen in Figure 12, a FG simulation model was proposed in [16] and it describes the coupling of the input capacitors as well as the parasitic capacitors. A resistor

connected in parallel with each input capacitor was added to the model in order to solve the convergence problem.

These resistors were selected in a way that RC product of each pair is equal. Furthermore, these resistors must be very large in order not to have any effect at AC simulation. In case there is any charge trap at the FG a voltage source can be added to the floating gate FG where $V_Q = Q / C_T$.

$$R_i = \frac{1}{K\, C_i} \tag{2.20}$$

$$G_i = \frac{1}{R_i} \tag{2.21}$$

Where i=1, 2, 3 …. n k is a constant chosen to make R very large

$$R_i C_i = R_{GD} C_{GD} = R_{GS} C_{GS} = R_{GB} C_{GB} \tag{2.22}$$

$$\boldsymbol{V_{fg}} = \frac{\boldsymbol{C_{GB}\ V_0 + C_{Gs}\ V_s + C_{Gd}\ V\ C_1\ V_1 + C_2\ V_2 + \cdots + C_n\ V_n}}{\boldsymbol{C_T}} \tag{2.23}$$

Where R_i are the input resistors, C_i are the input capacitors, V_{fg} is FG voltage and V_1, V_2 V_n , are the control input voltages. V_0 is the substrate voltage and C_{GS} and C_{GD} are the parasitic capacitors. V_S and V_D are the source and drain voltages; respectively .

The drawback in this model is the same as in Ramírez-Angulo model [7] , the

incapability to account for the gate leakage or charge movement at the gate.

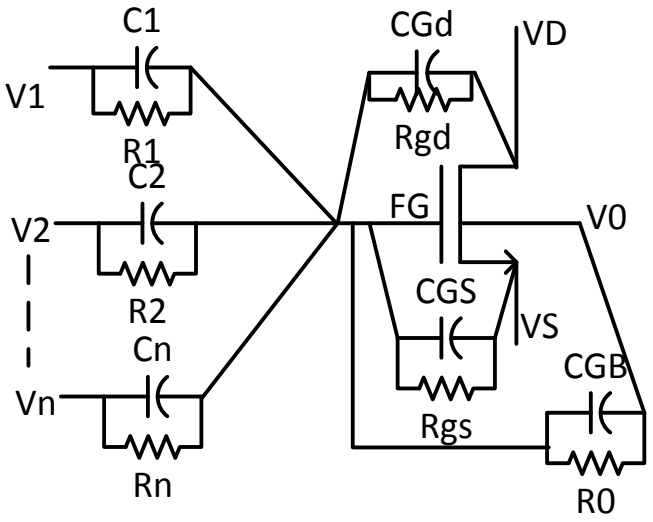


Figure 12: FGMOS simulation model in [16]

In [17], a model for FGMOS was presented using multiple inputs capacitors as shown in Figure 13. In this model, it is assumed that no parasitic capacitors connected at the gate and there was no DC path to ground in this model. Therefore to solve the convergence problem an initial voltage was added to the input capacitors. Adding a positive initial voltage to capacitor connected to FG through the negative terminal would be equivalent to remove charges from FG, while adding a negative initial voltage would be equivalent to added charges to FG.

$$V_{fg} = \frac{C_1}{C_1+C_2} V_1 \qquad (2.24)$$

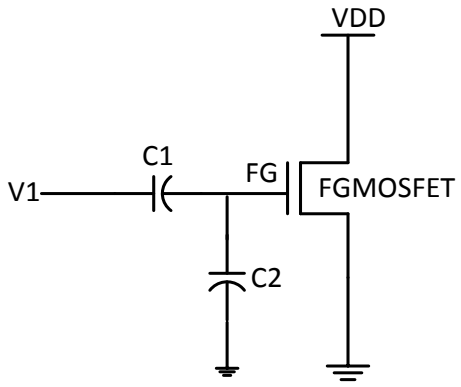


Figure 13: simulation model for FG transistor proposed in [17]

2.4.4 Summery

All the previous models for simulating FGMOS were suggested to model the functionality of FGMMOS and to solve the simulation convergence problem.

It should be noted that gate current was not described in the previous models because FGMOS was initially fabricated using double poly structure which was offered in the technologies that have tox more than 3nm and the DT gate current was negligible and did not have impact on FGMOS performance.

It is very important to model FGMOS in sub 100nm (single poly layer) technologies were tox is less than 3nm.

CHAPTER 3 LIMITATIONS IN FGMOS MODELS (CASE STUDY)

In this chapter we will present the main limitation in one of the FGMOS most promising models available in the literature the Ramirez-Angelo's FGMOS model (as a case study). A gate current impact on FGMOS behavior in FG operational amplifier (FG OP-AMP) implemented with [7] is discussed. Simulation results and comparison are also included.

3.1 FG Op-Amp

An Op-Amp is one of the main building blocks in analog design where it has two inputs, inverting and non-inverting with single or dual power supply as illustrated in Figure 14. It has very high input impedance and low output impedance. Usually the Op-Amp used in closed loop configuration to increase the precision.

In order to address the issue of the gate leakage current in nanometer technologies and its impact on FGMOS behavior, we had to evaluate a FG model available in the literature.

To do so, a FG Op-Amp implemented in TSMC 90 nm technology was simulated with P-type FG input transistors using the model suggested in [7].

The reason behind choosing this model is it's widely used in simulating FG circuits for many years and many researches relied on it in simulating FG circuits without fabricating the actual FG circuits.

This Op-Amp has eight transistors and single output. The differential FG input transistors have multiple inputs capacitively coupled to the gate and voltage sources depend on that inputs and a large resistor in order that VCVS has no effect in AC

simulation as shown in Figure 15. The single power supply equal to 1.2V, biasing current equal to 5.7μA, input capacitors ratio $C_1/C_T = 0.5$, $C_2/C_T = 0.5$ and two input voltages equal 550mV each.

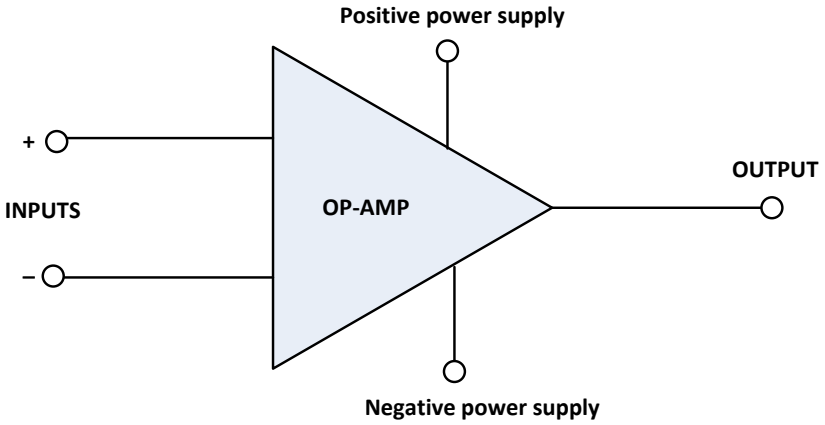


Figure 14: OP-AMP symbol

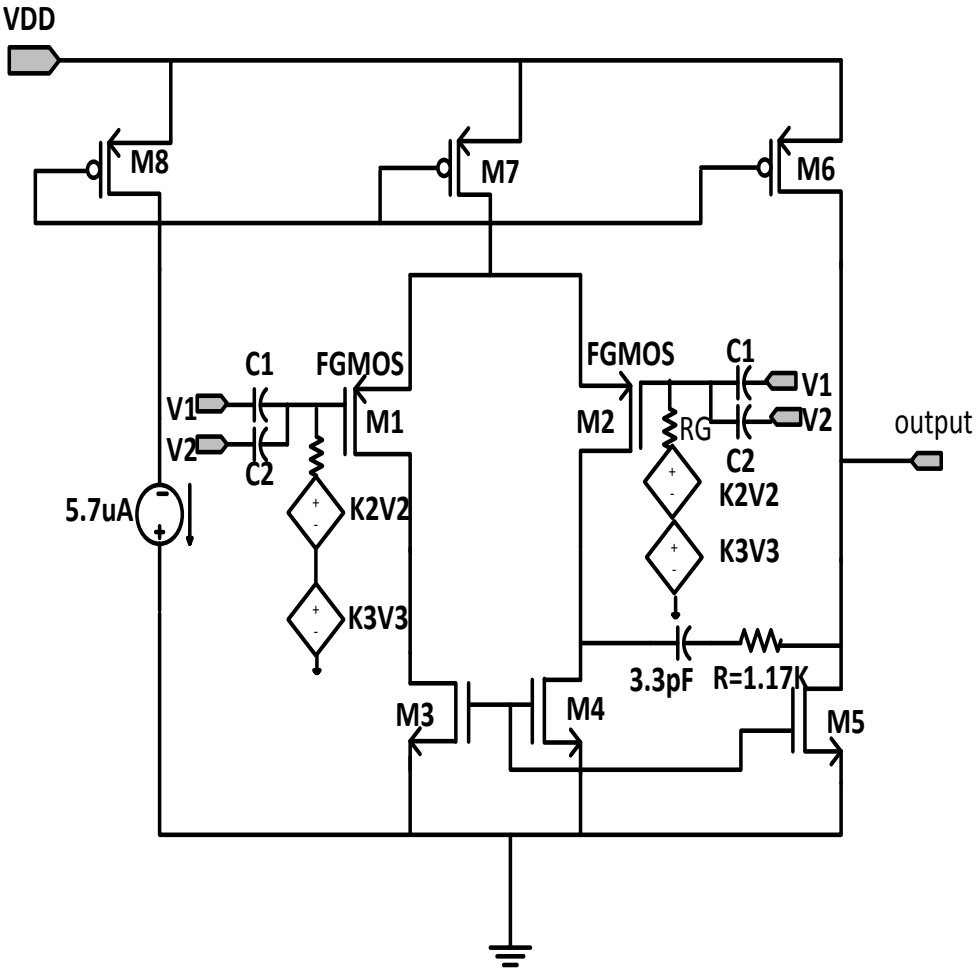


Figure 15: FG OP-AMP using simulation model in [7]

Transistor	Width (W)	Channel length (L)
M1	2.59uM	200nM
M2	2.59uM	200nM
M3	270nM	200nM
M4	270nM	200nM
M5	1.6uM	200nM
M6	5.3uM	200nM
M7	2.19uM	200nM
M8	350nM	200nM

Table 1: FG OP-AMP transistors dimensions

Gate leakage current can have different impacts on FG circuits depending on the circuit and in order to investigate that effect on FG Op-Amp a gate current represented roughly by a current source was used to describe the gate leakage in nanometer technology. A current source equal to 0.1nA was connected at the gate of the differential inputs of the amplifier circuit of FG Op-Amp as shown in Figure 16. The amplifier simulation was carried out using Cadence / Spectre to calculate the open loop AC gain as shown in Figure 17. As presented in Figure 17A, the AC gain of the amplifier is equal to 51 dB and all the transistors in saturation region as we swept the output gain versus frequencies.

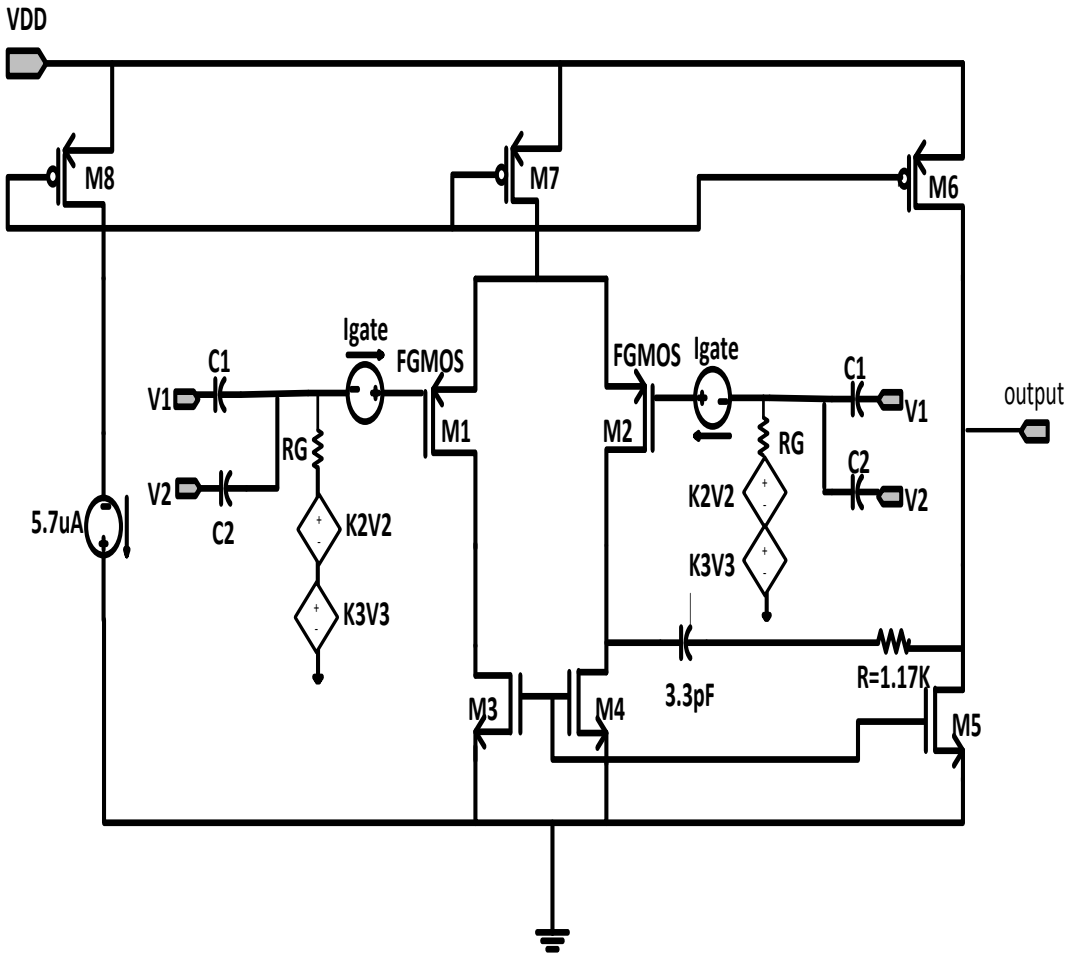


Figure 16: FG OP-AMP using FG model in [7] with a current source to describe the gate leakage current

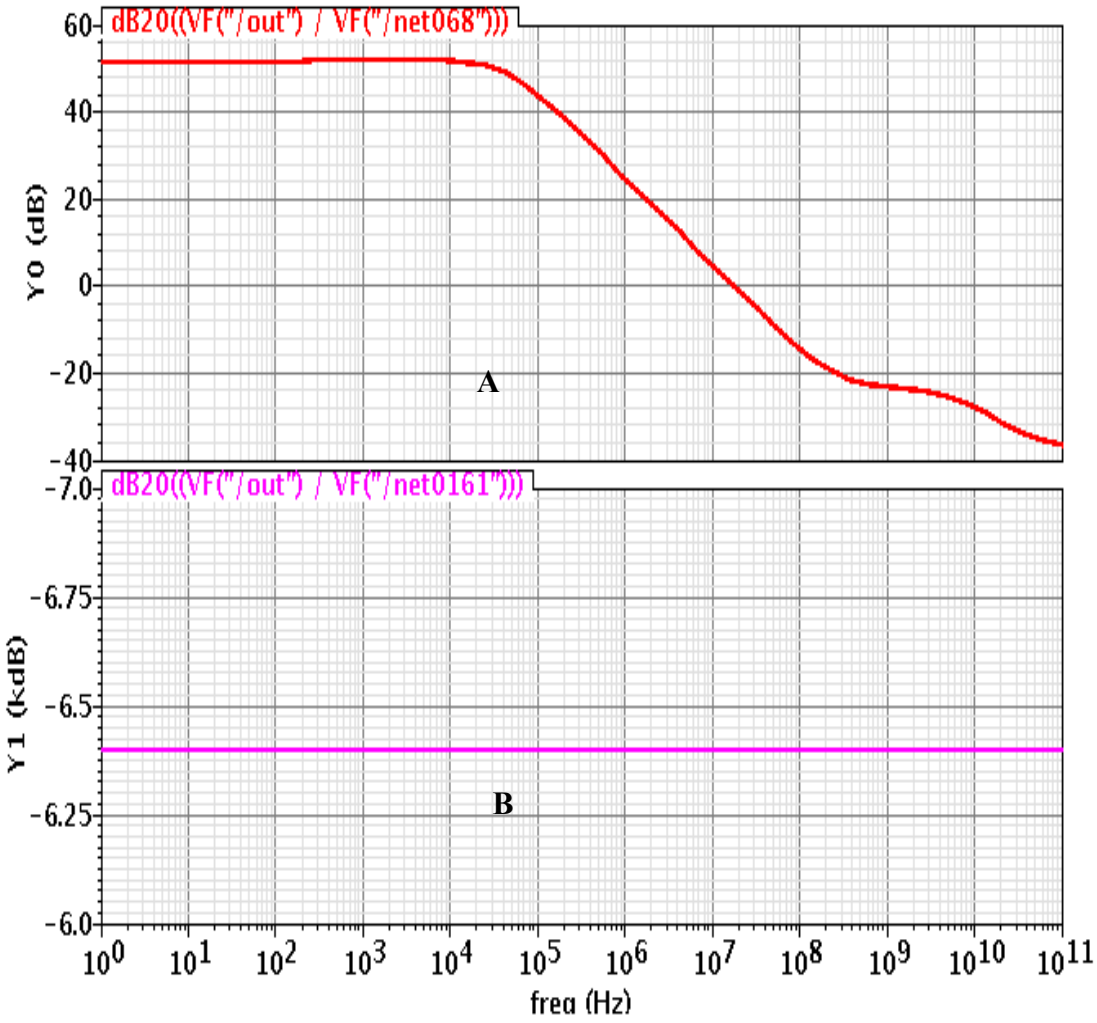


Figure 17: comparison between the gain of FG Op-Amp (in db) A: without the leakage current source B: with the gate leakage source

When a current source was added to the Op-Amp to model the leakage current the gain drops to -6.4dB because the FGMOS transistors in the Op-Amp M1 and M2 were turned off due to the reduction in the gate voltage. M1 and M2 region of operation changed from saturation to sub threshold region as a result from the gate voltage reduction.

This decreasing in gate voltage results from the charge transfer that occurred during the direct tunneling and causing an increasing in the gate-drain junction voltage and this reduces the gate-source voltage.

This is a fundamental limitation in this model due to the reduction in the gate voltage as a result of gate leakage current in nanometer technologies. Therefore, a new model for sub 100nm technologies needed to be developed.

3.2 Limitations in FGMOS simulation in [7]

In order to use the model proposed in [8] in nanometer technology (where the transistors suffer from gate leakage current), we need to examine the effect of gate leakage current on this model.

A FGMOS was implemented using coupling capacitors and VCVSs to provide the DC path [7]. A current source was added to take into consideration the gate leakage current with direction same as the charge movement direction in gate tunneling as shown in Figure 18.

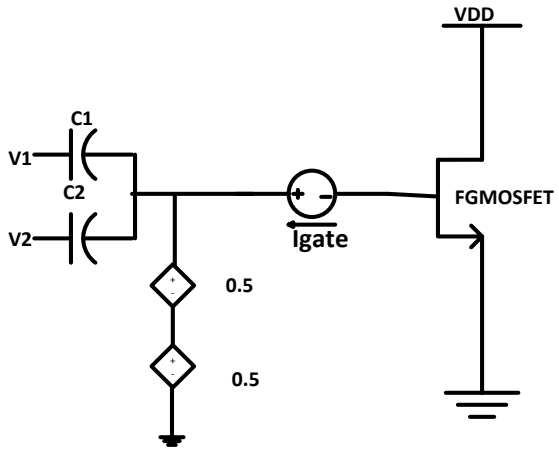


Figure 18: FG simulation model in [7] with gate current

A parametric analysis was performed for gate voltage with coupling capacitors ratio $C_1/C_T = C_2/C_T = 0.5$ for V_1=1.2V, V_2=1.2V and I_{gate} =0.1nA. Although a current source was added to this model to represent the leakage current the result was miss leading because the voltage was increasing at the gate as shown in Figure 19 instead of decreasing as we predict.

The gate voltage increased due to the gate current source instead of decreasing because the simulator calculates the total voltage at the FG node as:

$$VCVS_1+VCVS_2 + V \text{ (from the current source)}$$

The limitation in this model to respond to that current source related to the structure and the components used in it. The consequences of this constrains in this model, justifies the need of a new model for FG circuits in nanometers technology (sub100nm) that can incorporate the leakage current.

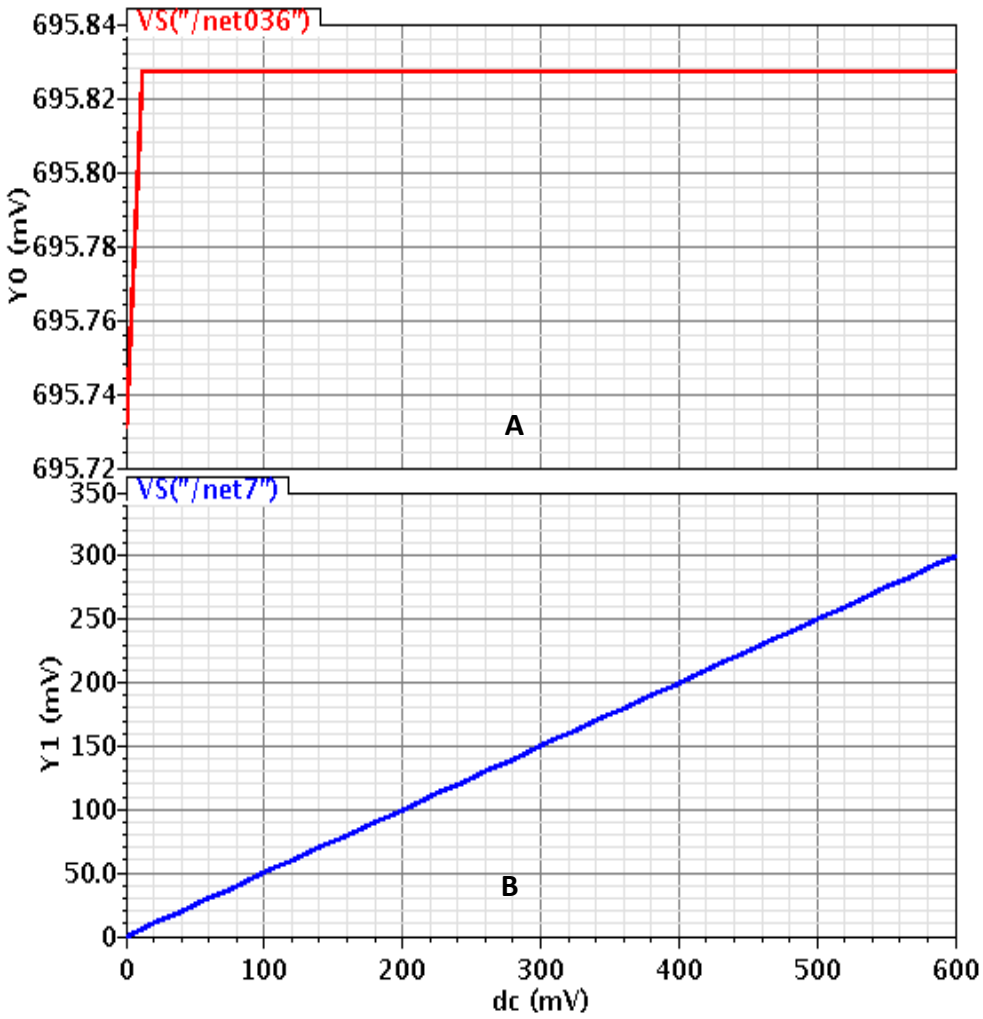


Figure 19: Floating gate voltage –input voltages A: before the gate current node B: after the gate current node

CHAPTER 4 FGMOS FABRICATION AND TESTING

In this chapter, the layout, design and fabrication issues of FG IC are described. The testing setup and equipment used are presented; furthermore the testing methodology and the procedure to conduct the FG measurement are discussed.

4.1 Research Methodology

After studying the available FGMOS simulation models and run simulations for the most widely used in analog applications as presented in chapter 3 , evaluations was carried out with respects to the challenges imposed by the technology scaling to the nanometer region.

The second step was the layout design and verifications using Cadence and Mentor graphics tools as illustrated in table 2 to check the design for any violations for the foundry rules and to confirm the identical matching between the layout and the schematic.

Next step, testing measurements were conducted using parametric test for I – V curves tracer for the gate and the drain of FG transistor using parametric analyzer (Agilent B1500A) as shown in Figure 27 assisted by other on the chip testing circuitry integrated on . The gate leakage current was monitored indirectly through the on chip testing setup.

As a last step in this research and based on a mathematical modeling and the obtained experimental results a new model was proposed for FG transistor in nanometer technologies that taking into account the gate leakage current. The

flow chart in Figure 20 explains the different steps followed in this work.

Software name	Descriptions
Virtuoso schematic editor	For circuit schematic design
Analog environment	Spector simulator
Virtuoso XL layout editor	For layout design
Calibre from Mentor	For layout physical verifications

Table 2: Cadence CAD tools used in this research

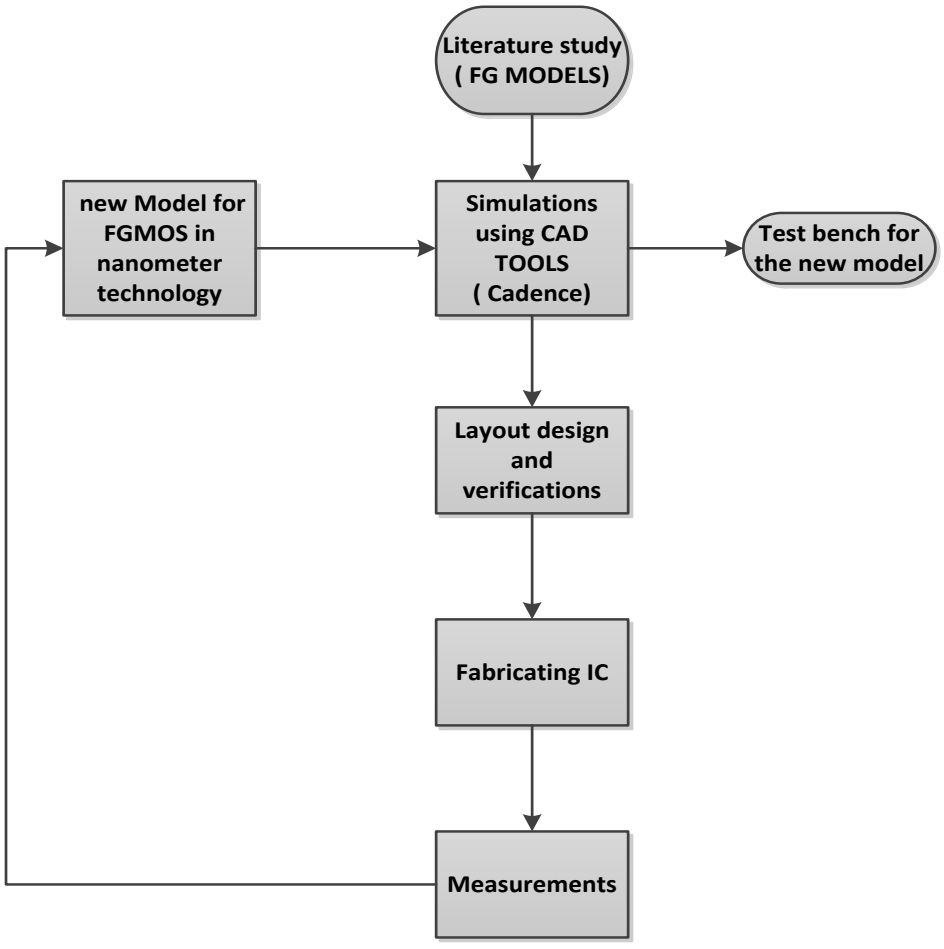


Figure 20 : research methodology flow chart

4.2 Fabricating a FGMOS experimental chip

A FGMOS experimental chip with area 1.5mm^2 was implemented using TSMC 90nm technology and single poly structure. The layout of this experimental chip is in Figure 21.

In the FG chip, there were different structures of FGMOS implemented using standard NMOS transistors with multiple inputs MIMCAP (Metal Insulator Metal capacitors) connected at the gate and on chip testing setup to measure the gate voltage.

MIM CAP are fabricated with two thin film metals that are separated by an insulator called capacitor top metal layer (CTM) and capacitor bottom plate metal layer (CBM) where it is located between M8 and M9 and with capacitance equal to 2fF/um .

Although this kind of capacitors take more area but it has small parasitic and good matching [19] and it does not need extra masking. MIM CAPs have a good capacitance density and low leakage density [20]. After the die was bonded, the IC was packaged in 40 DIP (dual in line) leads where the pads (for the inputs and outputs) where connected to the pins of the package as shown in figure 22.

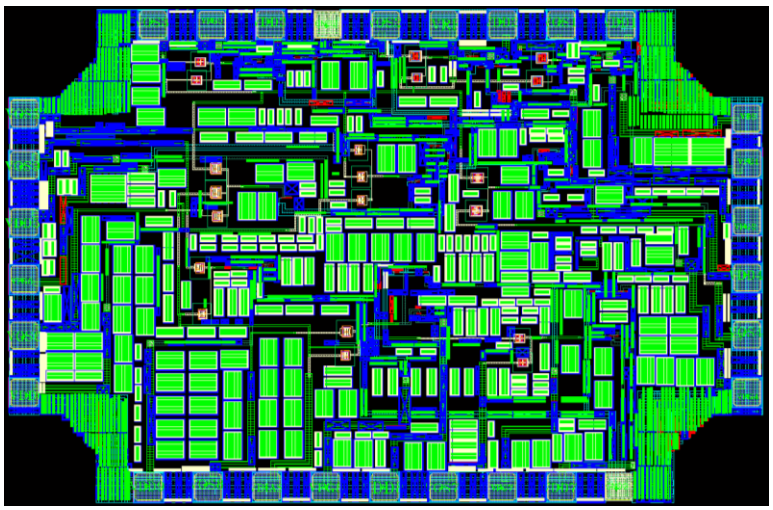


Figure 21 : FGMOS chip layout using TSMC 90nm

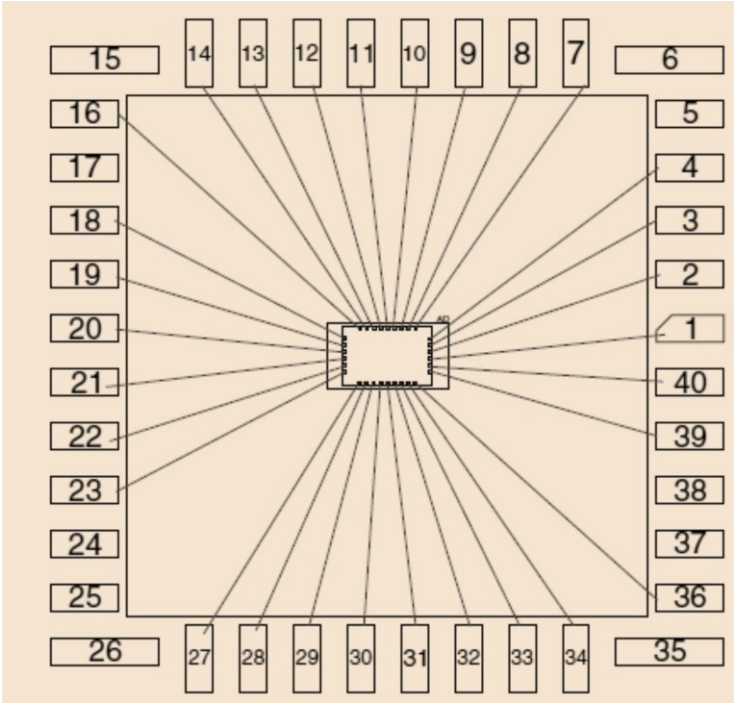


Figure 22: bonding diagram for the FGMOS IC in 40 DIP package

Parameter	FG 1	FG 2	FG 3	FG4	FG5
Width (W),µm	20	15	15	15	15
Length (L), µm	9.6	3.6	15	15	3.6
Number of inputs	2	2	3	3	2
Input capacitors size(fF)	C_1=465fF C_2=299fF	C_1=299fF C_2=299fF	C1=596.213fF C2=596.213fF C3=465.213fF	C1=350fF C2=350fF C3=350fF	C_1=465fF C_2=350fF

Table 3: FG transistors dimensions in the experimental IC

4.3 Layout verification

As the CMOS technology has been scaled down to nanometer region, IC routing facing more complexity and more constrains imposed by the manufacturer.

These constrains include the design rules such us the minimum features size and minimum spacing between wires and vias (connections between metals layers) where in the connection rules, the target is to avoid the open circuit and short circuit in the IC and in order to check the layout design, a verification tool like Mentor's Calibre [21] is needed.

The first step in the layout verification is the design rule check (DRC) for any violations. Figure 23 shows some of the geometrical terminology used for the design rules.

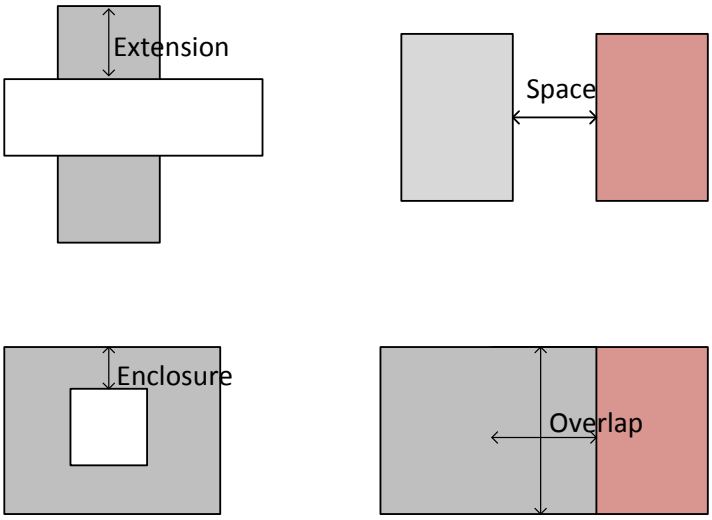


Figure 23: shows the geometrical terminology in Layout design rules

Where:

Extension: is the distance from the inside edge to outside edge

Space: is the distance between two layers

Enclosure: distance from inside edge to outside edge.

4.4 Manufacturing issues

4.4.1 Antenna effect

During the metallization process (adding metals layers) charges could be accumulated in the long wires that are connected to the poly silicon of the transistor gate.

These wires are floating before adding the top metal layer and during this, the wires will behave like antenna and collects charges. These charges can cause breakdown in the silicon oxide at the gate and lead to a permanent damage to the IC.

This effect depends on the ratio of wire to the gate area A_W/A_G [22] . This phenomenon happened when the gate area is small or when the wire area is large. Usually the manufacturer specifies this ratio and based on that the size of the wire should be chosen.

Antenna effect should be taken into consideration through the layout design to avoid any ‘floating” structure especially while using a MIM CAP.

To solve this problem there are two solutions. The first is jumper insertion by changing from one metal layer to another higher metal layer then go back to the same metal layer to break dawn a long wire. This makes the wire shorter and reduces the charge that might accumulate as shown in Figure 24. Clearly this is very effective solution to the antenna problem and it does not need any extra chip area however its time consuming and it will increase routing complexity.

The second solution is the diode insertion after routing, where a diode is added near the gate of the transistor to provide a discharge path, however, it will increase the cell area.

In the fabricated chip, jumper insertion was used to solve all MIM CAP antenna problems.

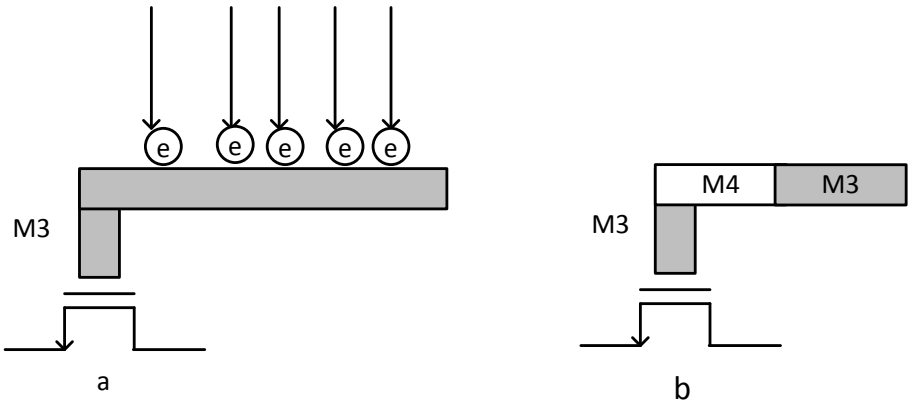


Figure 24: The antenna effects (a): routing example during the etching process
(b) Routing example after adding the jumper

4.4.2 Gate resistance

The parasitic resistance at the gate poly can increase the thermal noise and cause larger time constant; therefore, a fingered FGMOSFET was used for the large sizes transistors to reduce the total gate resistances. In such way, the transistor acts as a number of smaller transistors connected in parallel and reduce the gate resistance. For example a transistor with a channel length equal to 15um is divided it to 15 fingers with 1um per finger.

4.4.3 Charge problem

The method proposed in [11] was implemented to eliminate the charge that could be accumulated at the FG during fabrication. Dummy contacts had been added to the poly of the gate to eliminate these charges.

The contacts were not connecting the floating gate to any other parts in the circuits and it will not alter the FGMOS operation.

These contacts contains all the metal layers offered by TSMC 90nm like (M1, M2, M3 ….) to the top metal layer M9 where it is etched last as illustrated in Figure 25.

During the fabrication process, before removing the top metal layer, all the parts that has the same M9 will be connected together (which mean floating gate is not a floating node at this stage of fabrication) then when the etching process takes place, the charges will be removed from the floating gate.

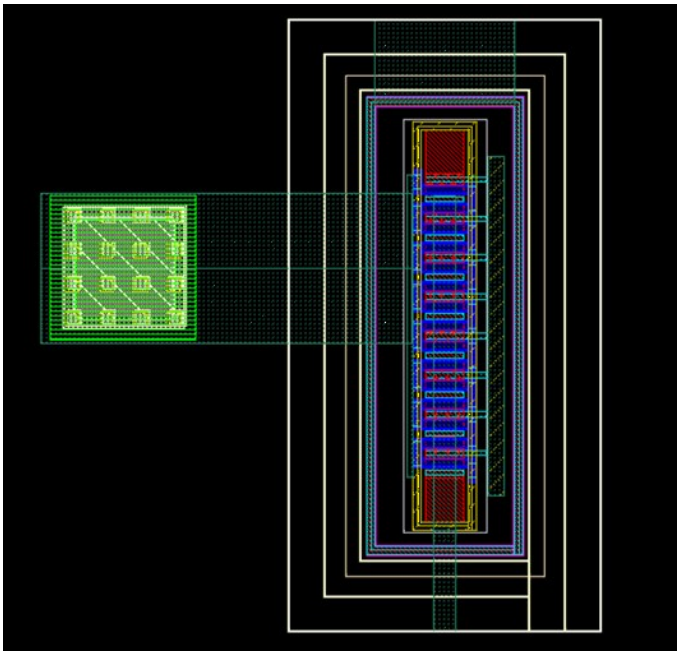


Figure 25: RFNMOS transistor with dummy contacts (from M1-M9) at the poly of the floating gate transistor to eliminate the accumulated charge

4.5 Testing setup and Equipment

Due to the nature of the floating gate structure it is not possible to connect any resistor or route the floating gate node to an output pad. In order not to disturb the floating nature of the gate, we had to come up with on chip testing setup to measure the floating gate voltage indirectly .The testing setup consists of source follower (common drain) transistor works as a buffer with its gate directly connected to the gate of FGMOS.

The FG voltage was determined by measuring the voltage across the source resistor of the source follower [23] as is shown in Figure 26.This setup also helps to calculate the gate current in the FG indirectly by monitoring for 40 hours.

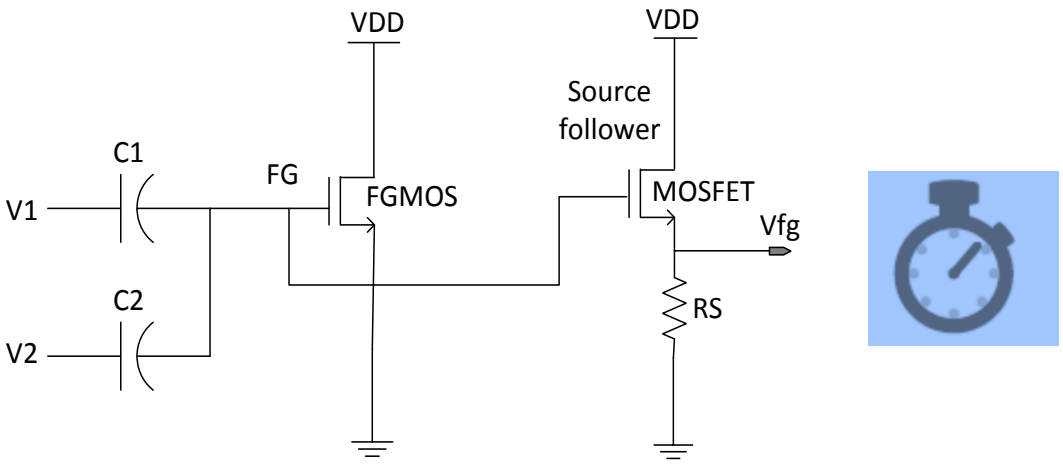


Figure 26 : The testing setup for measuring floating gate voltage

As is shown in Figure 27, a semiconductor device analyzer from Agilent (B1500A) [24] was used for I-V sweep measurements to characterize FGMOS.

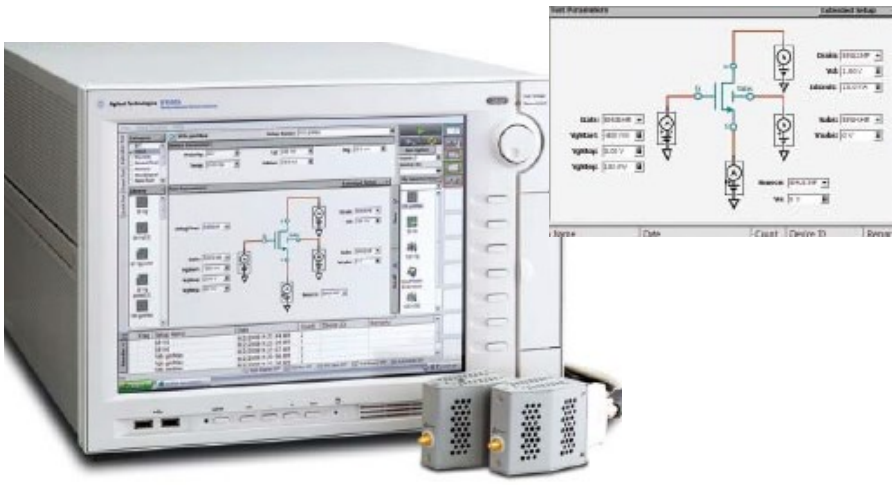
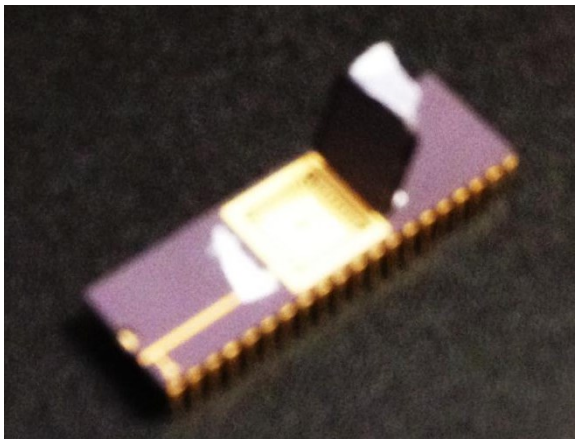


Figure 27: B1500A semiconductor analyzer from Agilent [24]

4.6 The Experiment

The FG chip testing was carried out in two stages. In the first stage, the semiconductor analyzer B1500A was used to run parametric test to extract the I-V sweep measurements for the gate and drain terminals to validate the possibility to implement FGMOS using standard MOS and MIMCAP instead of the double poly technique as used in older technologies and to examine the effects of the multiple inputs on the threshold voltage of FGMOS.

The analyzer has the Source/Measure Units (SMU's) where the measurements took place by connecting the three terminals of FGMOS (drain, gate and source) to the analyzer through three SMU's to conduct the I-V sweep measurement as shown in Figure 28.



a b

Figure 28: the testing setup to extract the I-V curve in FGMOS a: the three SMU's in Agilent B1500 analyzer b: the experimental chip showing the die inside the package

The parametric test was performed to extract the I-V curve by sweeping the drain voltage from 500mv to 1.2V and applying constant voltage to one of the terminals of the gate and sweeping the other input voltage from zero and 1.2V. The measurements were conducted from the analyzer to characterize the behaviour of FGMOS transistor.

In the second stage, we explored the impact of the gate DT current on the performance of FGMOS by monitoring the FG gate voltage for 40-50 hours using Oscilloscope and Multi meter to measure the output voltage of the follower in order to investigate the DT impact on FGMOS performance. These measurements of the FG voltage help to calculate the leakage current as shown later.

CHAPTER 5 THE EXPERMENTAL RESULTS AND DEVELOPMENT OF A NEW FGMOS MODEL

In this chapter, the measured results for the FG transistor were analysed. Also, a new simulation model is developed for FGMOS in nanometer scale technologies. The Simulation results for the new model are also included.

5.1 FGMOS characterization results

In this section we present the testing measurement for the FG chip. Figure 29 shows the I_D-V_{gs} curve for FGMOSFET with W= 20 um, L=9.6um, and two inputs at the gate with C_1=456fF, C_2=299fF and V_1 = 0.5V. The obtained V_{THFG} does not match to Eq. (2.14) for FGMOS in where for the experimental result V_{THFG} was **0.187V** while the V_{THFG} using Eq. (2.7) was **−0.377 V.** Also in Figure 30 when V_1=1.5V V_{THFG} was **0.442V** while the V_{THFG} using Eq. (2.7) was **−1.1V.**

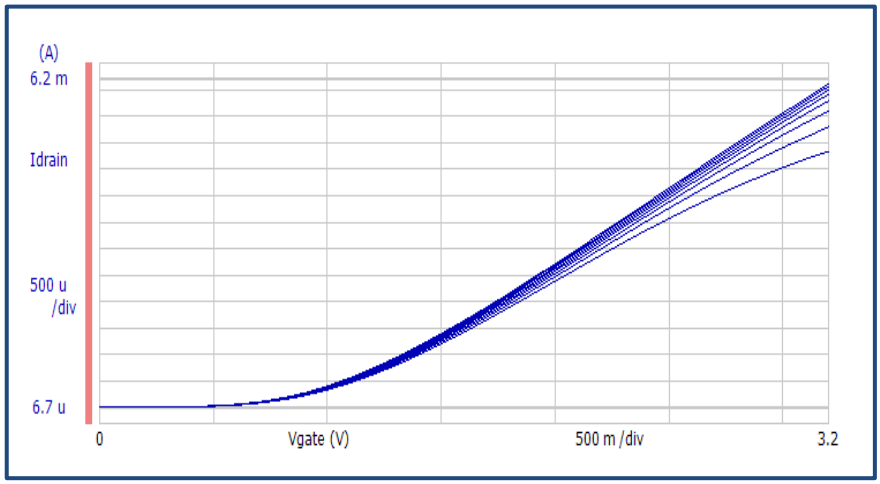


Figure 29: FGMOS experimental result for ID-Vgs with respect to Vds by sweeping V_2 and V_1=0.5 V

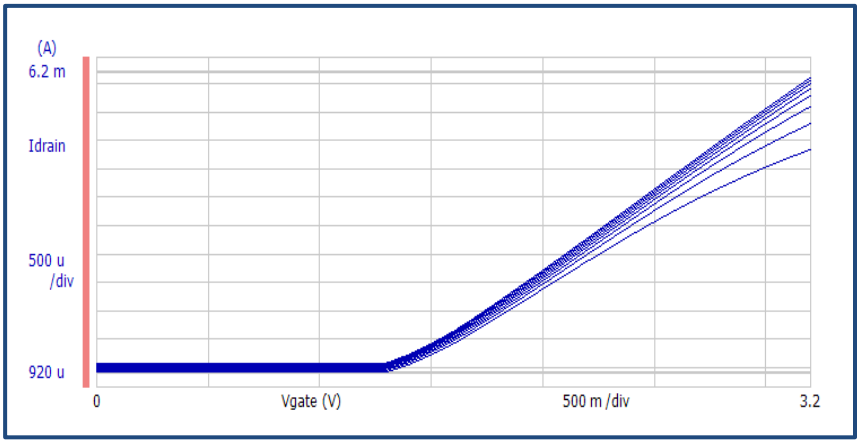


Figure 30 : FGMOS experimental result ID-Vgs with respect to Vds by seeping V_2 and V_1=1.5V

Also, there is a quite different between the experimental results shown in Figures 29, 30 and the simulation results from Cadence/ Spectre for multiple input FGMOS as illustrated in figures 31 and 32.

The threshold voltage was less than the one in standard MOS at certain input voltages and by increasing the input voltages, the threshold voltage becomes

zero. By increasing the voltage further, the drain current at zero gate-voltage becomes higher.

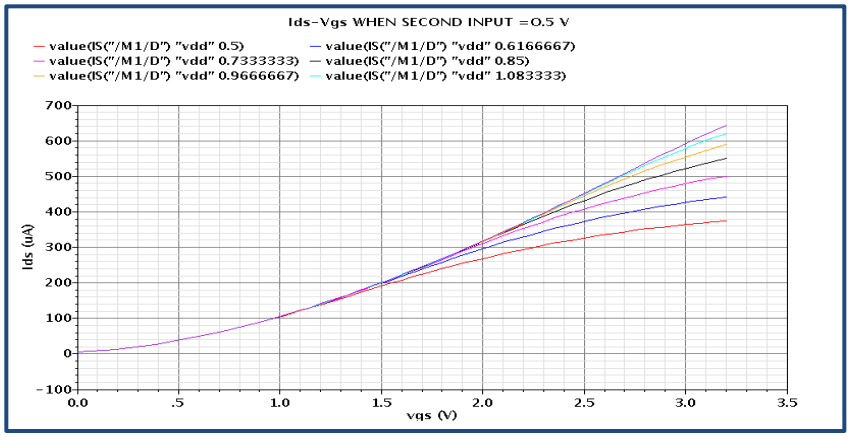


Figure 31 : FGMOS simulation result for ID-Vgs with respect to Vds by sweeping V_1 and V_2=0.5 V

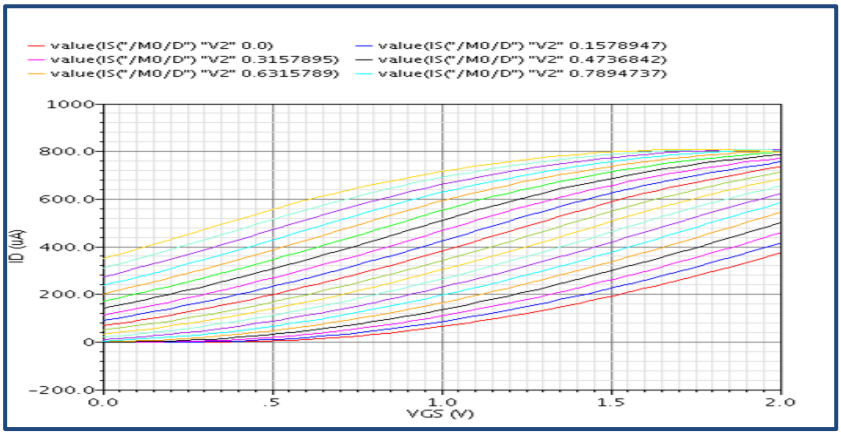


Figure 32: FGMOS simulation result for ID-Vgs with respect to Vds by sweeping V_1 and V_2=2 V

Figures 33 and 34 show that V_{THFG} versus of the second or third input voltage V2, V3 and is inversely proportional to it.

Furthermore, in the experiment the I_D-V_{DS} is almost the same as from the one obtained by the simulator as shown in Figures 35; however, there is a huge difference in the sub- threshold leakage current values as shown in Figures 36 and 37.

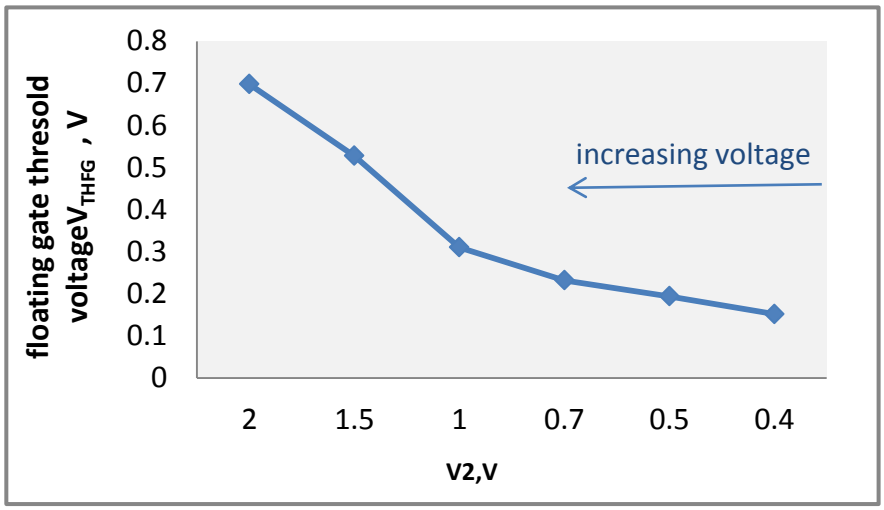


Figure 33: The experimental threshold voltage behavior of 2- inputs FGMOS with W=20um, L=9.6um, while sweeping V_1

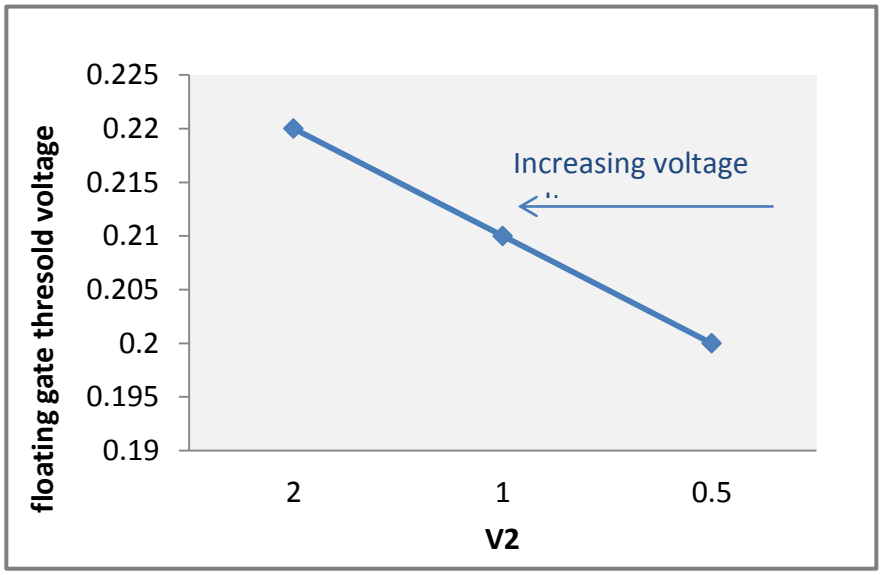


Figure 34: The experimental threshold voltage behavior of 3- inputs FGMOS with W=15um, L=15um, by sweeping V1 and setting V2=V3

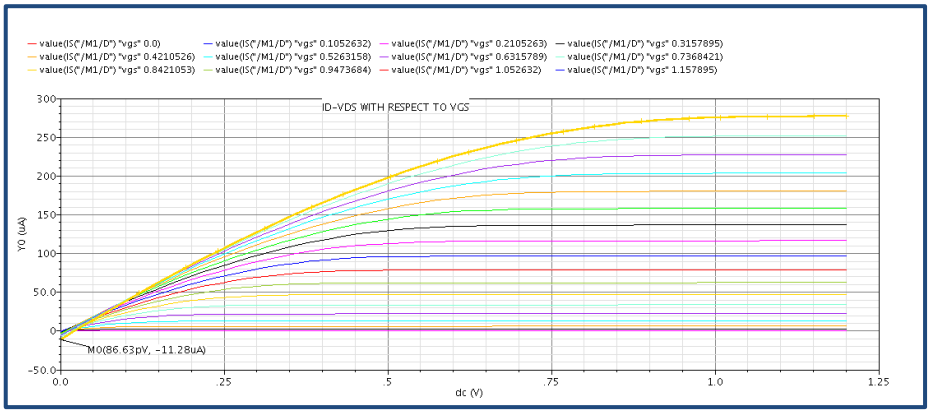


Figure 35 : Simulation result for I_D-V_{DS} with respect to Vgs of FGMOS

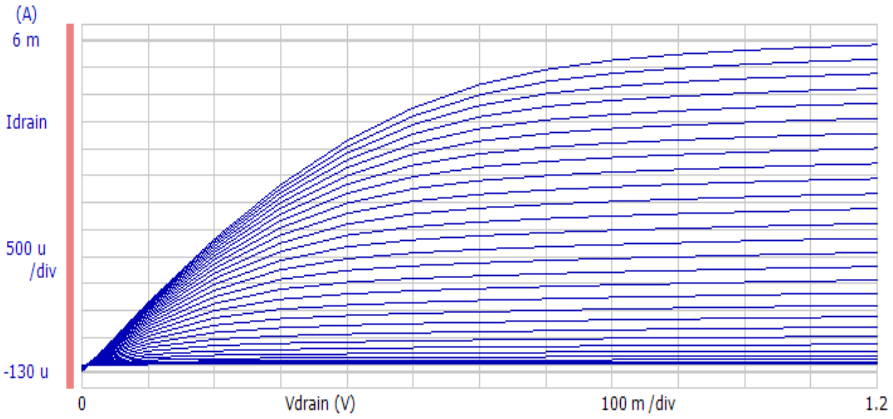


Figure 36: The experimental results for I_D - V_{DS} with respect to Vgs for W= 20 um and L=9.6um and V_1=0.5 V

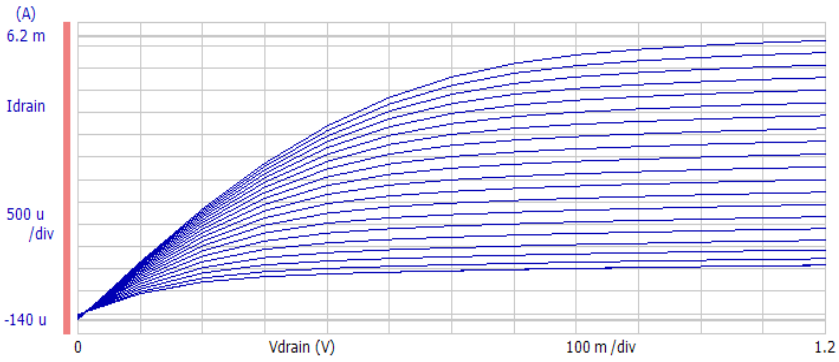


Figure 37: The experimental results for I_D - V_{DS} with respect to Vgs for W= 20 um and L=9.6um and V_1=2 V

5.2 Monitoring FG voltage

A biasing voltage was applied to the FGMOS and to the source follower from separate pads in order to sweep the power supply separately.

Gate voltages were applied to charge the floating gate and then grounded. The output of the source follower (which is directly connected to the FG) was monitored for 40 and 50 hours to investigate the impact of gate tunneling current on the FG voltage.

The FG voltage was found to be gradually decreasing as a function of time as illustrated in Figures 38 and 39.

This reduction in voltage results from the charge movement in the direct tunnelling between gate - source and gate- drain overlaps; respectively due to thin oxide layer at the gate (insulator) which is causing the DT gate current.

This decreasing in gate voltage happened slowly and gradually and it settles after 40-50 hours.

As we can see, this reduction in floating gate voltage is larger when channel length of the transistor is longer and this confirm that the leakage current depends on channel length and the biasing voltage at the gate [12].

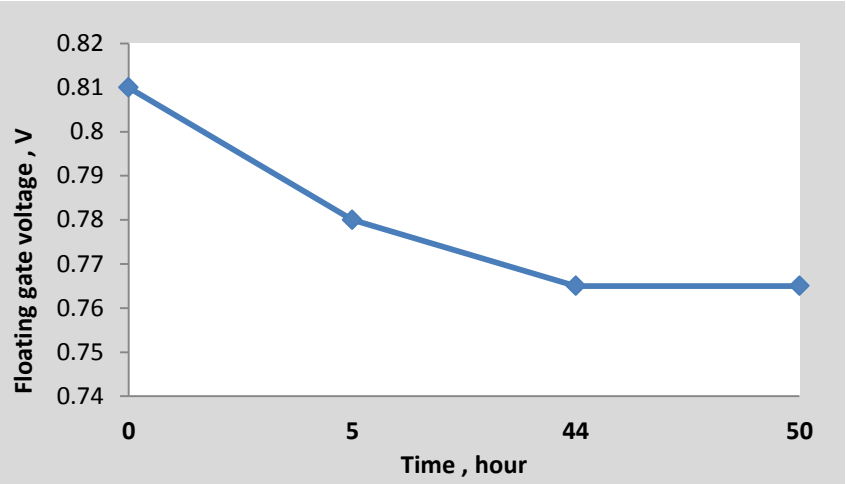


Figure 38: FG voltage decreasing with time for W= 20um, L=9.6um

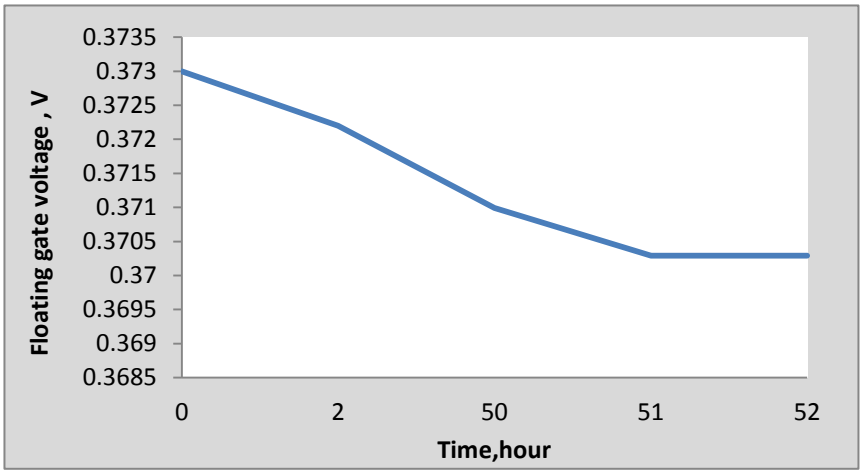


Figure 39: FG voltage decreasing with timefor W= 15um, L=3.6um

FG voltage change rate due to the leakage current is determined as:

$$\frac{dV_{fg}}{dt} = \frac{C_1}{C_T}\frac{dV_1}{dt} + \frac{C_2}{C_T}\frac{dV_2}{dt} \mp \frac{dV}{dQ}\frac{dQ}{dt} \tag{5.2}$$

$$\frac{dV_{fg}}{dt} = \frac{C_1}{C_T}\frac{dV_1}{dt} + \frac{C_2}{C_T}\frac{dV_2}{dt} + \cdots \mp \frac{1}{C_T} I_{Leakage} \tag{5.3}$$

As we can see from Eq. (5.3) it has the term $\frac{dV_{Leakage}}{dt} = \mp \frac{1}{C_T} I_{Leakage}$ which is depending on transistor type. In other words, the change rate for NMOS is negative because the electrons tunnels from the gate, while the change rate for PMOS is positive because the holes tunnels to the gate.

For DC biasing $\frac{dV_1}{dt} = \frac{dV_2}{dt} = 0$

$$\frac{dV_{fg}}{dt} = \frac{dV_{Leakage}}{dt} = \pm \frac{1}{C_T} I_G \tag{5.4}$$

$$I_G = C_T \cdot \frac{dV_{fg}}{dt} \tag{5.5}$$

The experiment shows that the gate leakage current is high enough to discharge the FG node and decrease gate voltage with time which will cause degradation in the performance of FG cells in precision circuits.

The results in Figures 37 and 38 indicate that gate voltage in FGMOS will decrease with time in a change rate $\frac{dV_{fg}}{dt}$ that is directly proportional to gate current and inversely proportional to the total input capacitance seen at the gate as seen in Eq. (5.5).

On one hand, we were unable to measure gate leakage current directly from the FG without connecting any resistive element due to the nature of FGMOS.

However, we were able to extract gate leakage current from the testing results using the formula in Eq. (5.5), the data in Figure 40 shows a comparison between the calculated gate current bases on experimental results with the simulation results.

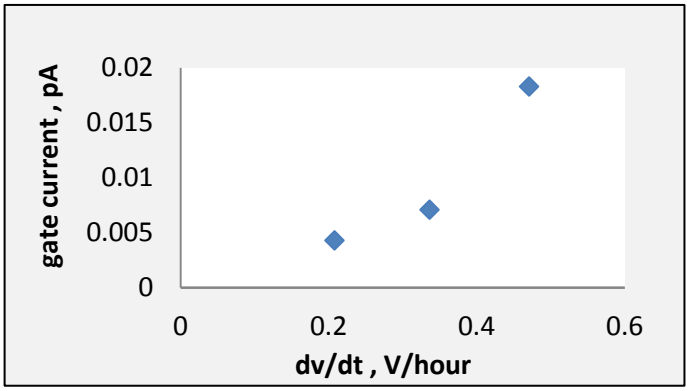


Figure 40: Gate leakage current based on measured gate voltage variation

5.3 Mathematical model for FGMOS

Based on the results of the measurements and the analytical analysis, the small signal analysis for FG transistor represented in chapter 2 is not accurate and it cannot be applied for nanometer technologies where the transistors suffer from gate leakage current due to the very thin oxide layer.

A new small signal analysis for nanometer CMOS technologies (sub 100nm) is derived. In this analysis, the gate leakage current and the way that the floating gate structure responded to it is considered.

Gate leakage current results from the charge movement at the insulator and depends on the transistor type and the polarity across the insulator, and it can be found as:

$$Q_{Leakage} = C_T\, V_{Leakage} \tag{5.6}$$

$$\frac{dQ_{leakage}}{dt} = C.\frac{dV_{leakage}}{dt} \tag{5.7}$$

$$I_{leakage} = C_T\,.\,\frac{dV_{leakage}}{dt} \tag{5.8}$$

$$\frac{dV_{leakage}}{dt} = \pm\,\frac{1}{C_T}\,.\,I_{leakage} \tag{5.9}$$

$$V_{leakage} = \frac{1}{C_T}\int I_{leakage}\; dt \tag{5.10}$$

As can be seen from Eq. (5.9) the voltage change that results from charge movement can be positive or negative quantity depends on the direction of the charge movement direction into or out from the gate . This means that FG voltage might increase or decrease as a function of time based on the leakage current and the capacitors values and can be written as:

$$\frac{dV_{FG}}{dt} = \frac{C_1}{C_T}\frac{dV_1}{dt} + \frac{C_2}{C_T}\frac{dV_2}{dt} + \cdots\frac{C_n}{C_T}\frac{dV_n}{dt} \mp \frac{1}{C_T}\,.\,I_{leakage} \tag{5.11}$$

$$\mathrm{V_{FG}} = \sum_{\mathrm{i=1}}^{\mathrm{N}}\frac{C_1}{C_T}\,V_1 + \frac{C_2}{C_T}\,V_2 + \cdots\frac{C_n}{C_T}\,V_3 \mp \mathrm{V_{leakage}} \tag{5.12}$$

And in order to keep the transistor in saturation region $V_{FG} > V_{TH,}$ and by letting V1 as the effective input, will result in:

$$\boldsymbol{V_1 > \frac{C_T}{C_1} V_T - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n \mp \frac{C_T}{C_1} V_{leakage}} \quad (5.13)$$

Which means the equivalent threshold voltage for floating gate transistor in nanometers technologies is:

$$V_{THFG} = \frac{C_T}{C_1} V_T - \frac{C_2}{C_1} V_2 - \frac{C_3}{C_1} V_3 - \cdots - \frac{C_n}{C_1} V_n \mp \frac{C_T}{C_1} V_{leakage} \quad (5.14)$$

Eq. (5.13) has a very important implication of gate leakage current because this leakage current will increase the effective threshold voltage in NMOS transistors. Also, this equation confirms the measurement results for the threshold voltage where it increased as the input voltages is increased one of as shown in Figure 33.

The threshold voltage in floating gate transistor is a function of gate DT leakage current where it is an exponential function of the voltage at the gate (VG) and technology dependent parameters A and B as shown in Eq. (5.15)

$$\boldsymbol{I_G = A . e^{B.V_G}} \quad (5.15)$$

Where B and A are the technology and biasing conditions dependent parameters extracted from fitting the simulation data in TSMC 90nm for gate current using BSIM4. These parameters will increase as the technology scaled more to 65nm, 45nm or 28nm.

The FG threshold voltage can be written as:

$$V_{THFG} = \frac{C_T}{C_i} V_T - \frac{C_2}{C_i} V_2 - \frac{C_3}{C_i} V_3 - \cdots - \frac{C_n}{C_i} V_n + \frac{1}{C_i} \int (A . e^{B.V_G})\, dt \quad (5.16)$$

5.4 A new Model for FGMOS transistor in nanometer technologies

As the CMOS technology continue scaling, tox shrinks down and this cause more gate leakage current. The importance of this model arises from the need to test FG circuit without the need to fabricate it.

A new simulation model for FGMOS that is suitable for sub 100nm is proposed in this research that takes in consideration the gate leakage current. The proposed model is compatible with simulators, such as Spectre and SPICE.

The model was built using a standard transistor from the industry (TSMC90nm) with two cells from analog hardware description language AHDL library and one block using Verilog a code to describe the gate tunnelling.

The new model consists of voltage dependant current source implemented in Verilog A code embedded under Cadence / Spectre and is described as a function of V_{gs} terminal [12, 13]. Also, there is an integrator which integrates the gate tunnelling current to generate a voltage and a subtractor as illustrated in Figure 41.

This model can be used with any technology that has SiO_2 thickness less than 3nm and suffer from gate leakage current with no changes to the model itself; however, minimal changes need to be done to the gate tunnelling cell to comply with the technology parameters where the gate tunnelling current exponentially increases as tox decreases. The model can be used for transient and DC simulations by adding initial condition to the leakage current integrator.

The floating gate voltage will be the weighted sum of all the input voltages at the gate deduced by the leakage voltage as presented in Figure 42.

In this model, the ‘Vfg node was broken to two nodes: the first node is the output of the integrator ($V_{leakage}$) where the leakage current was integrated and the other node is the weighted sum of all coupled input voltages at the gate (V_{fg}) .

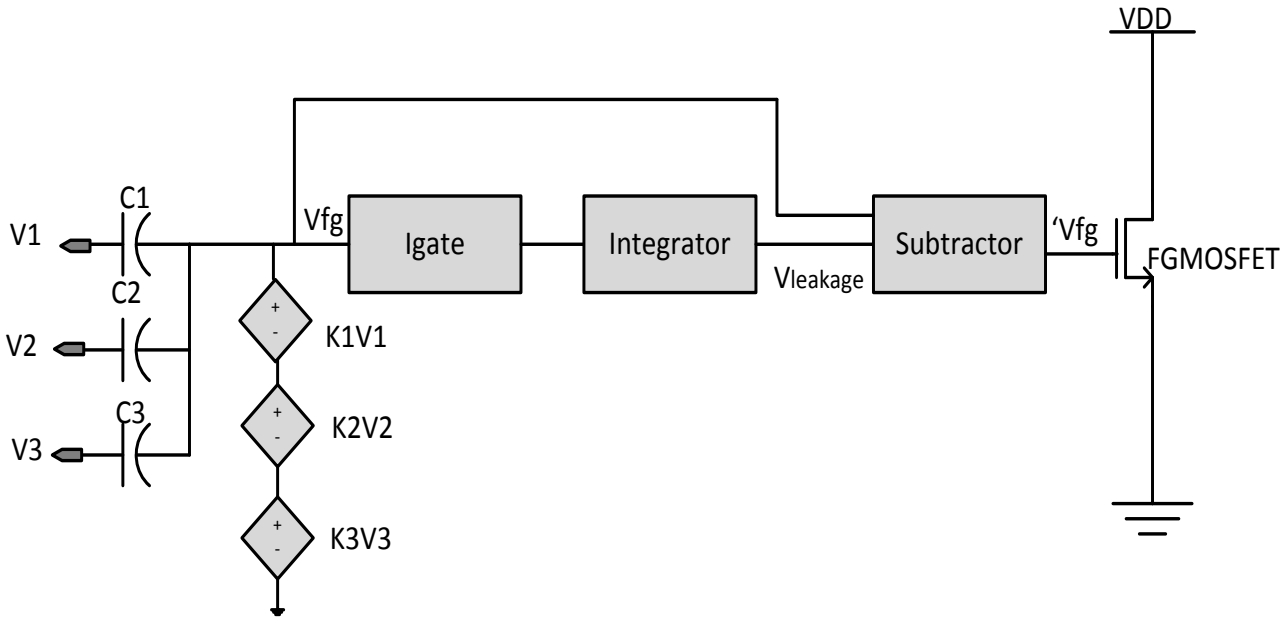


Figure 41: The structure of N-TYPE FGMOS simulation model for nanometer (sub 100nm) technologies

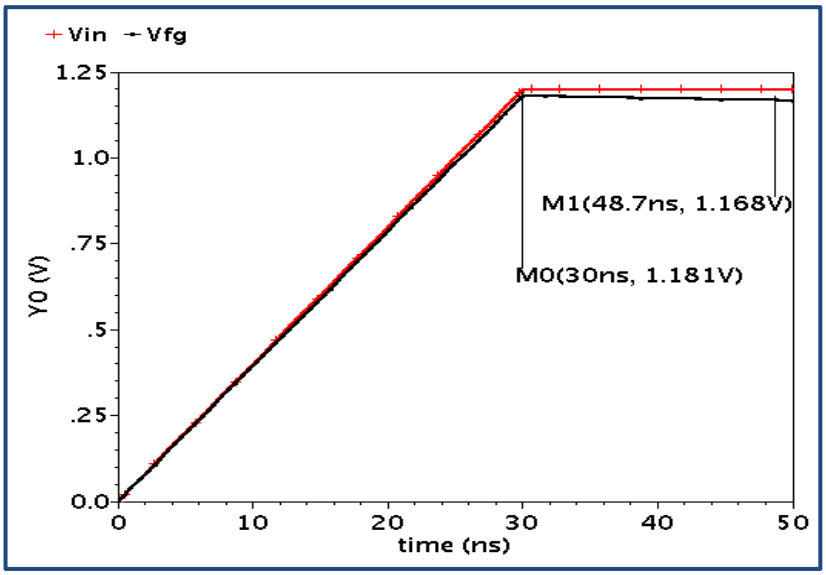


Figure 42: The N-type FG simulation model transient analysis for $'V_{fg}$

In this model, V_{fg} and $'V_{fg}$ can be determined as:

$$V_{fg} = K_1V_1 + K_2V_2 + K_3V_3 + \cdots + K_NV_N \tag{5.17}$$

$$K_i = \frac{C_i}{C_T} \text{ Where i = 1, 2, 3,….N} \tag{5.18}$$

$$'V_{fg} = V_{fg} - V_{leakage} \tag{5.19}$$

$$V_{leakage} = \frac{1}{C_T}\int_0^t (A \,.\, e^{B.V_{fg}})\, dt \tag{5.20}$$

In order to use this model in DC simulation an initial condition was needed to be added to the integrator. This initial condition can be found from Eq. (5.14). The result for the floating gate voltage is shown in Figure 43.

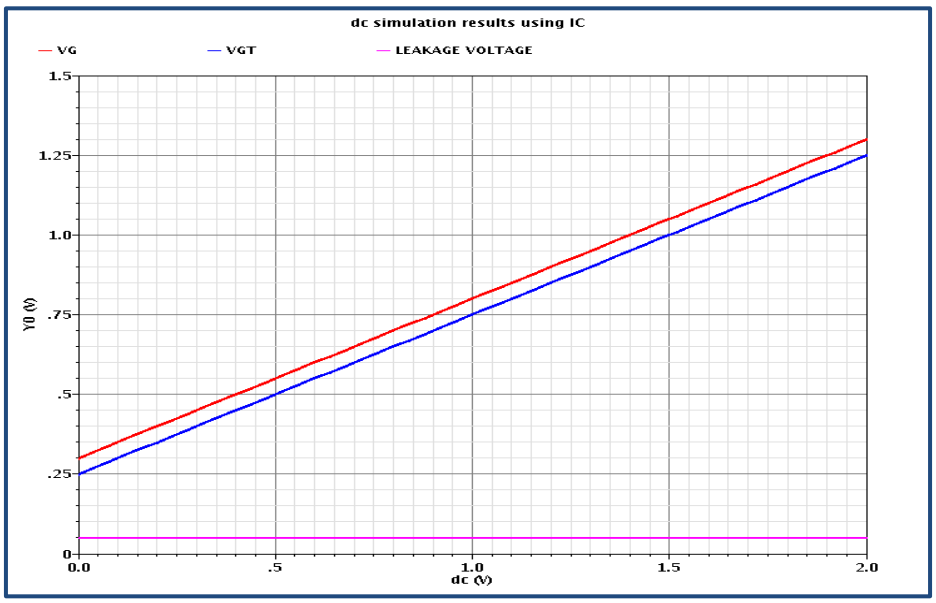


Figure 43: DC simulation for V_{fg} and 'V_{fg} using initial condition

In addition, to use PMOS FG transistor some modification should be done to the model for example the parameters A and B should be fitted to the simulated results for BSIM4 gate leakage and the subtractor should be replaced with adder to comply with Eq. (5.14).

5.5 FG Cascode current mirror using the new simulation model

Current mirror is one of the building blocks in integrated circuits and it has been used for biasing. This circuit is used to copy or multiply the input current as shown in Eq. (5.21) in which two identical transistors connected and had the same gate voltage and maintain saturation region as illustrated in Figure 44 however, mismatch between the two currents occur as a result of the channel length modulator λ as shown in Eq. (5.22) . A simple current mirror has very low output impedance and a Cascode current mirror technique was used to improve the output impedance.

$$I_{out} = K\, I_{ref} \tag{5.21}$$

$$\mathrm{k} = \frac{\mathrm{I_{out}}}{\mathrm{I_{ref}}} \frac{\mathrm{W_2/L_2}\,(1+\lambda \mathrm{V_{DS2}})}{\frac{\mathrm{W_1}}{\mathrm{L_1}}\,(1+\lambda \mathrm{V_{DS1}})} \tag{5.22}$$

Where λ is the channel length modulation and $V_{DS1,2}$ are the voltage across the drain source terminals for transistor M1, M2 respectively.

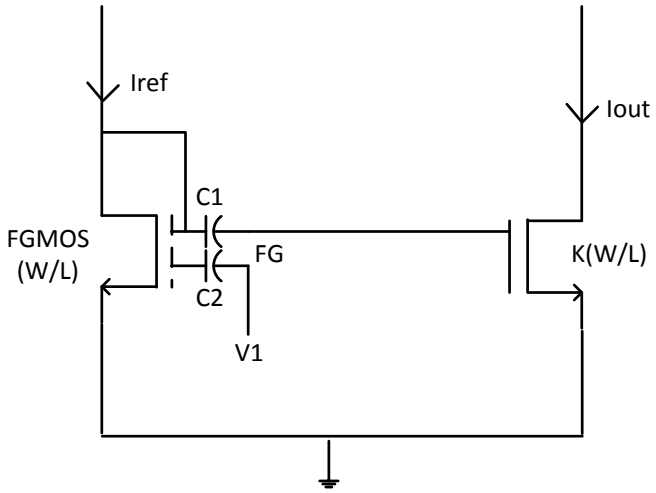


Figure 44: simple current mirror for FGMOS transistor

A FG cascode current mirror was implemented first using the model proposed in [7] as shown in Figure 45 and then were compared with the simulation results of the new model.

The simulation result for the current mirror is shown in Figure 46 and as we can see, the input voltage helped to reduce the mismatch in current mirror that results from channel length modulator and we were able to tune to get a very accurate copy of the input current.

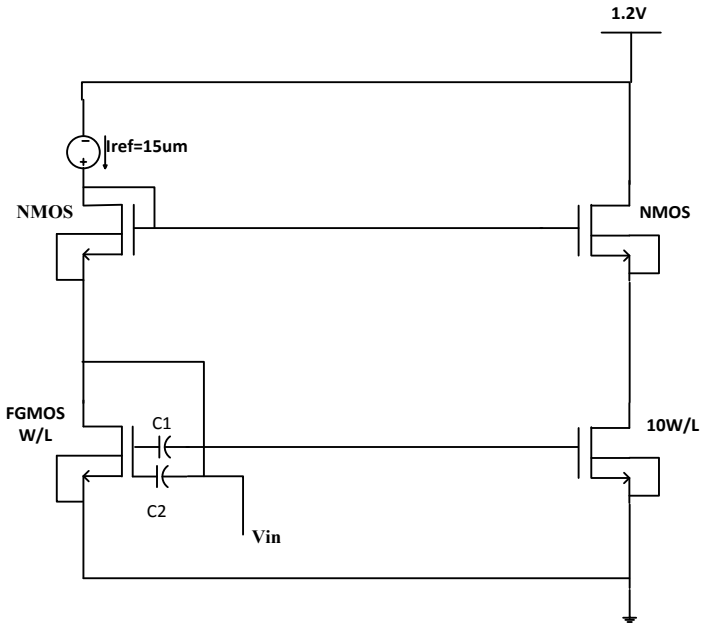


Figure 45: FG cascode current mirror implemented TSMC 90nm

V_{DD}	I_{ref}	M_1	M_2	M3	M4	I_{out}
1.2V	50uA	W=50um L=1um	W=500um L=1um	W=80um L=1um	W=80um L=1um	5mA

Table 4: FG current mirror transistors dimensions

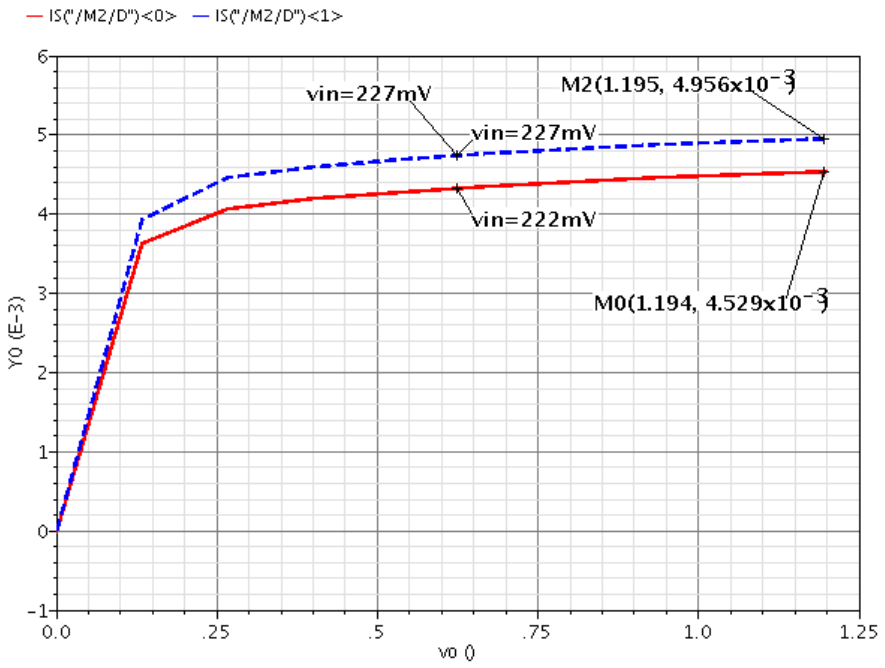


Figure 46: output current versus output voltage for FG cascode current mirror implemented with Ramirez model [7].

As presented in Figure 47 for the simulation results of cascode current mirror using the proposed model, by applying the same voltage of 227mV, the generated output current is much smaller than what obtained with the other model. In order to obtain an accurate output current the input voltage was increased to 280 mV to compensate for gate voltage reduction that results from gate current in the model. Also, the output impedance of the FG cascode current mirror implemented with the new model is shown in Figure 48.

The importance of these results arises from the need to have accurate model to simulate FGMOSFET to get realistic result without the need to fabricate.

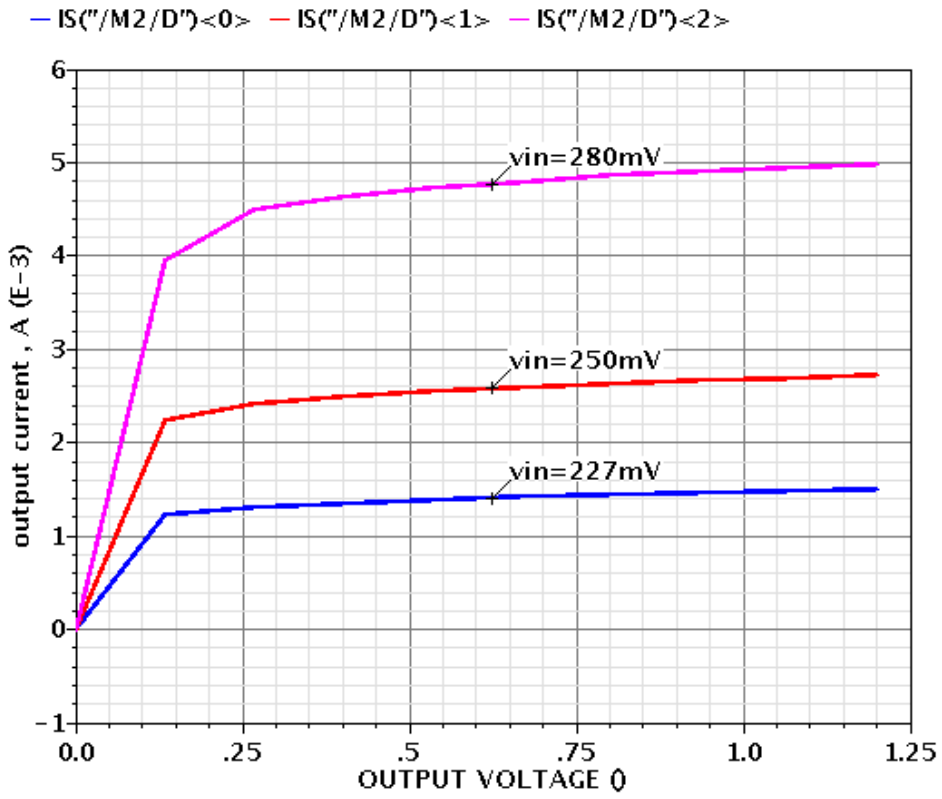


Figure 47: output current versus output voltage for FG cascode current mirror implemented with the new model.

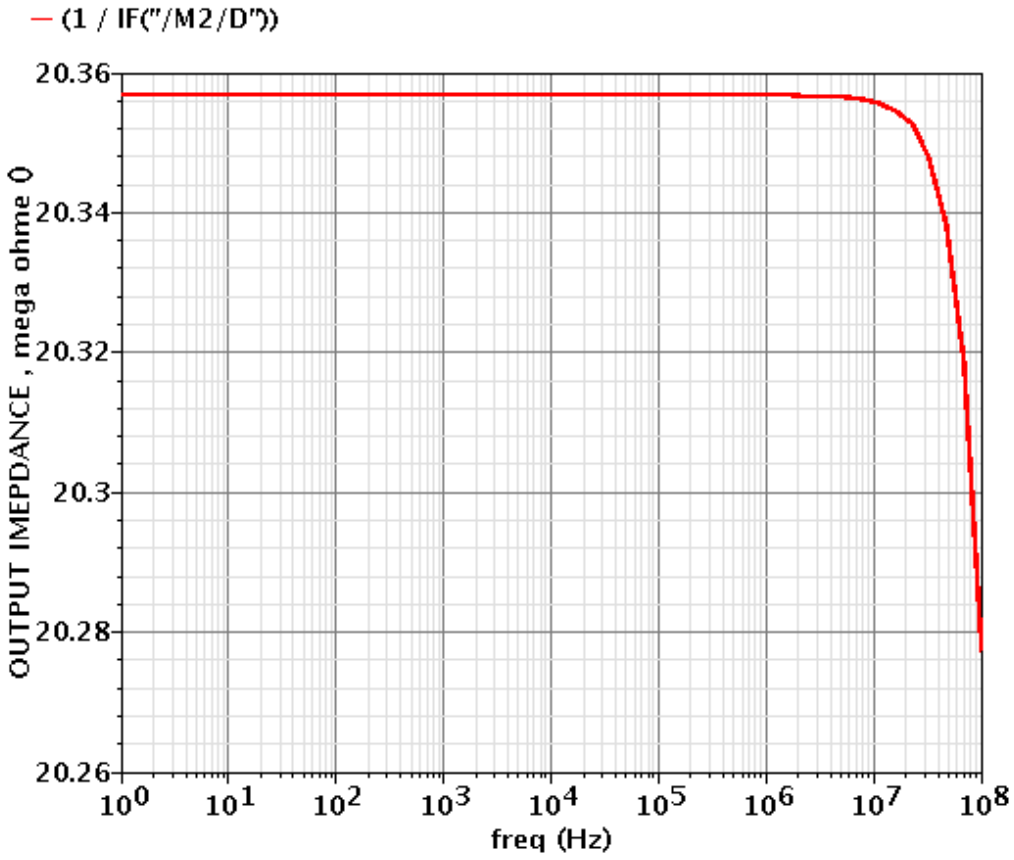


Figure 48 : The output impedance of the FG cascode current mirror implemented with the new model

CHAPTER 6 CONCLUSION AND FUTURE WORK

In this research, we developed a new simulation model for FGMOS that is suitable for sub 100nm CMOS circuits that suffer from gate leakage current. The proposed model is compatible with all industry simulators, such as Spectre by Cadence and SPICE programs.

This model can be used for Transient and DC simulation with any technology that has SiO_2 thickness less than 3nm and suffer from gate leakage current with no changes to the model itself. However minimal changes need to be done to the gate tunnelling cell to comply with the technology parameters where the gate tunnelling current exponentially increases as t_{ox} decreases.

It has been shown the DT gate leakage current has non-negligible influence on FG circuit performance .In addition; FG voltage gradually decreases as a function of time causing a change in the threshold voltage due to the charge movement in direct tunnelling.

Simulations and experimental results were presented to illustrate that problem and a new model was developed for in nano meter technologies to help the designers to simulate a realistic model for FG circuits with ultra-thin CMOS technologies.

Although this research provides a solid ground to for analogue designers, a further improvement can be applied.

For example testing setup for monitoring FG voltage can be prepared to enhance the accuracy of the measurements because it deals with very small voltage variation.

Changing the capacitor type, if possible, from metal - metal to poly - poly capacitor which means in this case changes the foundry.

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